Paper

A Comparative Study of Single- and Dual-Threshold Voltage SRAM Cells

Pragya Kushwaha and Amit Chaudhry[a]

[a] University Institute of Engineering and Technology, Panjab University, Chandigarh, India

Abstract—In this paper, a comparison has been drawn between 5 transistor (5T), 6T and 7T SRAM cells. All the cells have been designed using both single-threshold (conventional) and dual-threshold (dual-Vt) voltage techniques. Their respective delays and power consumption have been calculated at 180 nm and 65 nm CMOS technology. With technology scaling, power consumption decreases by 80% to 90%, with some increase in write time because of the utilization of high-Vt transistors in write critical path. The results show that the read delay of 7T SRAM cell is 9% lesser than 5T SRAM cell and 29% lesser than 6T SRAM cell due to the lower resistance of the read access delay path. While read power of 5T SRAM cell is reduced by 10% and 24% as compared to 7T SRAM, 6T SRAM cell respectively. The write speed, however, is degraded by 1% to 3% with the 7T and 5T SRAM cells as compared to the 6T SRAM cells due to the utilization of single ended architecture. While write power of 5T SRAM cell is reduced by up to 40% and 67% as compared to 7T SRAM, 6T SRAM cell respectively.

Keywords—5T SRAM, 65 nm CMOS technology, 6T SRAM, 7T SRAM, low power SRAM, power reduction technique.

1. Introduction

Static Random Access Memories (SRAM) are widely used in computer systems and many portable devices. As technology is scaling down, in result the threshold voltage is also scaling down along with the operating voltage. A huge amount of sub-threshold leakage current occurs due to low threshold voltage. SRAM based cache memories are best suited for system on chip applications due to its high speed and low power consumption. Due to device scaling there are several design challenges for micrometer SRAM design. Now we are working with very low threshold voltage and ultra-thin gate oxide due to which leakage energy consumption is getting increased. Besides this data stability during read and write operation is also getting affected in conventional 6T SRAM cell. In order to obtain higher noise margin along with better performance new SRAM cells like 5T and 7T SRAM cells have been introduced. In this paper a comparative analysis of 6T, 5T [1]–[5] and 7T [6]–[11] SRAM cell has been carried out. The major difference between the 5T and 7T SRAM cell is that in case of 5T SRAM cell a single bit line is used for read /write operation that saves area, bit line leakage and provides a read/write performance comparable to the 6T SRAM cell while in case of 7T SRAM cell, the storage nodes are isolated from the bit lines during a read operation, thereby enhancing the data stability as compared to the 6T SRAM cell. Table of the comparison of average power dissipation and delay time during write and read operation with the different combination of threshold voltage of NMOS and PMOS at 180 nm is summarized in Table 4. The paper is organized as follows. The 5T and 7T SRAM cell is presented in Section 2. Simulation results are shown in Section 3. Section 4 gives the conclusion.

2. SRAM Cells

A typical six transistor (6T) SRAM cell in a 65 nm technology is shown in Fig. 1. The robustness of an SRAM cell is characterized by the hold stability during read operation. In a 6T SRAM cell, the data storage nodes are directly accessed through the pass transistors connected to the bit lines. The storage nodes are disturbed due to the voltage division between the cross-coupled inverters and the access transistors during a read operation. The data is most vulnerable to external noise during a read operation due to this intrinsic disturbance produced by the direct data-read-access mechanism of a standard 6T SRAM circuit(destructive read) [12].

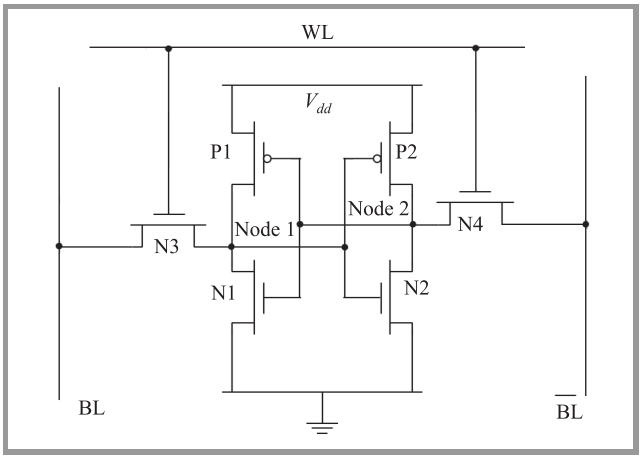


Fig. 1. Single-Vt 6T SRAM cell in a 65 nm CMOS technology: WL – word line, BL – bit line.

There are strict constraints on the sizing of transistors to be able to maintain the data stability and functionality of a standard 6T SRAM cell as shown in Table 1. The design of a 6T SRAM cell is typically characterized by the ratio (β) of the size of the pull-down transistors to the access transistors [12]–[14]. In order to maintain the read stability, N1 and N2 (Fig. 1) must be stronger as compared to

the access transistors N3 and N4. Alternatively, for write ability, N3 and N4 must be stronger as compared to P1 and P2. These requirements are satisfied with careful transistor sizing, as illustrated in Fig. 1.

Table 1
Width of transistor used for simulating 6T SRAM

Transistors	Width [nm]
N1, N2	130
N3, N4	100
P1, P2	65

In addition to the data stability issues, the increasing leakage energy consumption of the embedded memory circuits is also a growing concern. In modern high performance microprocessors, more than 40% of the total active mode energy is consumed due to leakage currents [15]–[19]. So, dual threshold voltage transistors are used for this purpose. In dual-Vt 6T SRAM cell (Fig. 2) transistors N1, N2, P1, P2 are designed as high threshold voltage (Vtn-high for NMOS, Vtp-high for PMOS) transistors because they are more appropriate to store data in memory design and access transistors N3, N4 are designed as low threshold voltage (Vtn) transistors because they can possess larger drain current. In result it reduces the access time and maintains data retention at the same time [20]–[27].

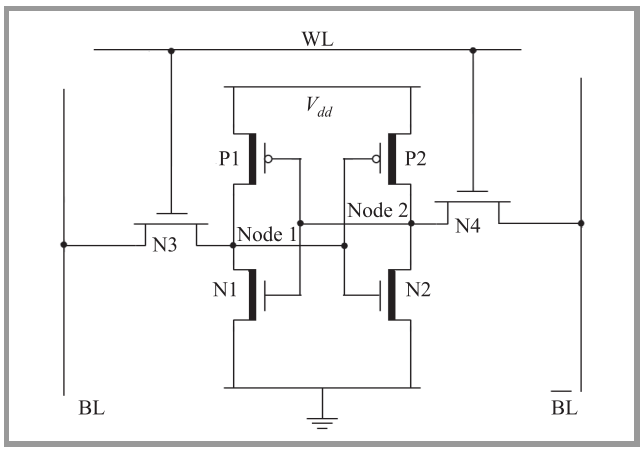


Fig. 2. Dual-Vt 6T SRAM cell in a 65 nm CMOS technology: WL – word line, BL – bit line.

2.1. The 5T SRAM Cell

The 5T cell has only one access transistor N3 and a single bit line BL. Writing of 1 or 0 into the 5T cell is performed by driving the bit line to V_{dd} (1.8 V) or V_{ss} (0 V) respectively, while the word line is asserted at V_{dd}. The write ability of the cell is ensured by a different cell sizing strategy. A sizing example in a standard 65nm CMOS is shown in Fig. 3 [1]. The trip point of the inverter N2-P2 has been decreased, while the trip-point of the inverter N1-P1 has been increased. Further, the pass-transistor N3 is sized to support both write and read operation.

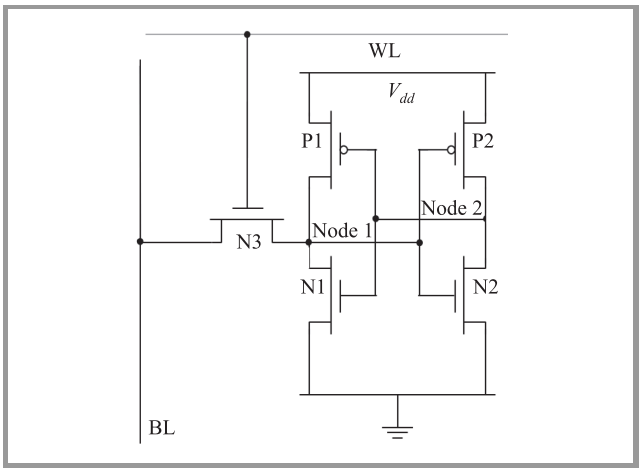


Fig. 3. Single-Vt 5T SRAM memory cell in a standard 65nm CMOS technology.

Since the 5T SRAM cell is writable at $V_{BL} = V_{WL} = V_{dd}$, a non-destructive read operation requires a bit line precharge voltage, V_{PC} ($\sim 600 - 650$ mV), where $V_{SS} < V_{PC} < V_{dd}$. This is in contrast to the conventional 6T SRAM bit lines, which are precharged at V_{dd} before a read operation.

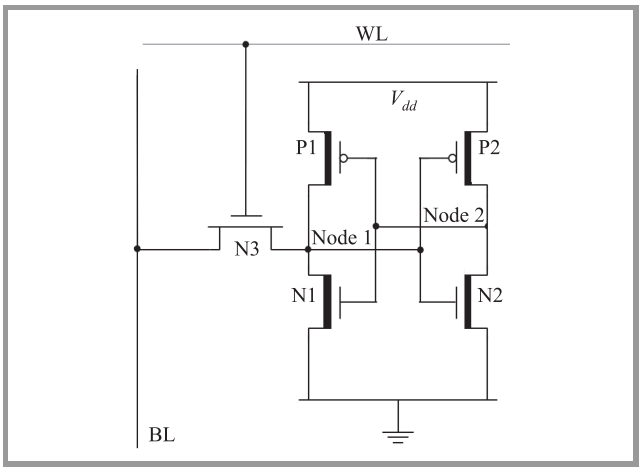


Fig. 4. Dual-Vt 5T SRAM memory cell in a standard 65 nm CMOS technology. Thick line in the channel area indicates a high-Vt transistor.

We have designed a dual-Vt 5T SRAM in this paper (Fig. 4) by high-Vt transistors P1, P2, N1, N2 and low-Vt transistor N3. And the sizes of transistors are shown in Table 2. This configuration saves leakage power dissipation in comparison to dual-Vt 6T SRAM cell.

Table 2
Width of transistor used for simulating 5T SRAM

Transistors	Width [nm]
N3	130
P1, N2	100
N1, P2	65

2.2. The 7T SRAM Cell

The schematic of the 7T dual-Vt SRAM cell [6] with transistor sized for 65 nm CMOS technology is shown in Fig. 5 and transistor's width is shown in Table 3. Prior to a read operation, the RBL is precharged to V_{dd}. To start the read operation, the read signal R transitions to V_{dd} while the write signal W is maintained at V_{ss}. If a 1 is stored at node1, RBL is discharged through the transistor stack formed by N4 and N5. Alternatively, if a 0 is stored at node1 RBL is maintained at V_{dd}. The storage nodes (node1, node2) are completely isolated from the bit lines during a read operation. The data stability is thereby significantly enhanced as compared to the conventional 6T SRAM cells. Prior to a write operation the WBL is charged (discharged) to V_{dd} (V_{ss}) to get ready to force a 1 (0) onto node1. To start the write operation, the write signal W transitions to V_{dd} while the read signal R is maintained at V_{ss}. Write 0 onto node1, the pass transistor N3 must be stronger as compared to the pull-up transistor P1.

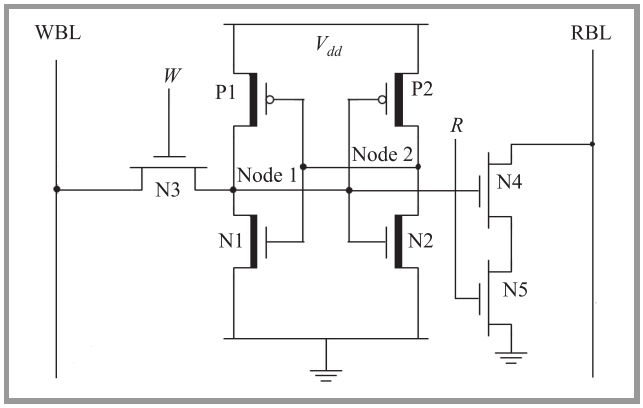


Fig. 5. The schematic of 7T dual-Vt SRAM circuit in a 65 nm CMOS technology. WBL – write bit line, RBL – read bit line, W – write control signal, R – read control signal. For data stability $\beta = 0.25$. Thick line in the channel area indicates a high-Vt transistor.

Table 3
Width of transistor used for simulating 7T SRAM

Transistors	Width [nm]
N3, N4, N5	130
P1, N2	100
N1, P2	65

Alternatively, to write 1 onto node1, the pass transistor N3 must be stronger as compared to N1.
Furthermore, since N3 transfers a degraded 1 (due to the Vt drop across the N-channel access transistor), the inverter formed by N2 and P2 is required to have a low switching threshold voltage that assists the transfer of a full 1 onto node1. Hence, these design requirements are achieved by employing dual-Vt transistors with in the cross-coupled inverters as shown in Fig. 5. As these cross-coupled inverters are not on the read-delay-path. The transistor sizing of the dual-Vt cross-coupled inverters therefore does not affect the read speed and at the same time reduces the leakage power of the cell. In this way at a time only one bit line is activated in this SRAM cell that saves bit line leakage.

3. Simulation Results

In this section comparison between conventional 5T, 7T SRAM cell has been carried out on the basis read delay, write delay, average write power and read power (Table 4).

Table 4
Comparison of average power dissipation and delay time during write and read operation with the different combination of threshold voltage of NMOS and PMOS at 180 nm

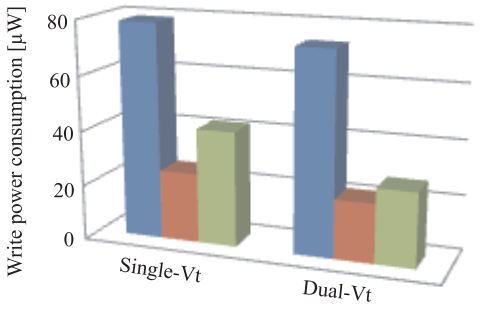
Cell	Mode	Av. write power [μW]	Write delay [ps]	Av. read power [μW]	Read delay [ps]
6T SRAM	Single-Vt	78.74	18.73	45.69	18.46
	Dual-Vt	73.4	18.68	39.42	18.48
5T SRAM	Single-Vt	25.33	18.92	34.52	14.17
	Dual-Vt	21.54	18.72	33.62	14.18
7T SRAM	Single-Vt	41.93	18.94	38.6	12.95
	Dual-Vt	27.14	18.82	35.47	12.95

3.1. Average Read/Write Power Consumption

Write power consumption of single ended structure [28]–[37] is less because the bit line capacitance is reduced as compared to 6T double bit line switching.

$$P_s = \alpha C_l V_{dd}^2 F_{cl}\,,$$

where P_s is switching power dissipation, α is activity factor, C_l is load capacitance and V_{dd} is power supply, F_{cl} is input clock frequency.
As shown in Fig. 6, the write power is significantly reduced with the proposed 5T and 7T SRAM cell as compared to the 6T SRAM cells. This reduction in the write power is due to the utilization of a single bit line for writing into the 5T and 7T SRAM cells in a memory column. For the 6T SRAM cell both bit lines in each memory column are periodically precharged to V_{dd}. After the bit line precharge is completed and once a write decision is made, one of the precharged bit lines is selectively discharged to V_{ss} (0 V) to perform a write operation. In a memory array with 6T SRAM cell, therefore, one of the bit lines needs to be fully charged and discharged during each write cycle, regardless of whether a 0 or a 1 is transferred to the cell. Alternatively, in case of writing a 1 to a memory column with the 5T SRAM, 7T SRAM cells, the write bit line (WBL) does not need to be discharged (maintained at the precharge voltage V_{dd}). The bit line dynamic switching

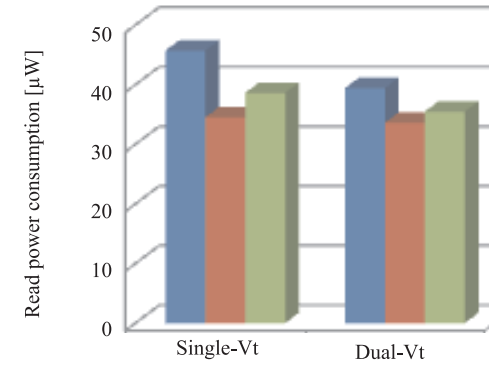


Cell	Single-Vt [µW]	Dual-Vt [µW]
6T SRAM	78.74	73.4
5T SRAM	25.33	21.54
7T SRAM	41.93	27.14

Fig. 6. Write power consumption.

power consumption is thereby significantly reduced with the 5T SRAM and 7T SRAM cells. Hence write power in 5T SRAM cell is reduced by 67% and in 7T SRAM cell it is reduced by 45% as compared to conventional 6T SRAM cell. As shown in Fig. 1, the write power of 5T SRAM cell is reduced by up to 40% as compared to 7T SRAM cell because RBL remains at V_{dd} (leakage power dissipation during write operation) in 7T SRAM cell.

During read operation, 5T SRAM precharges the single bit line to $V_{pc} = 650$ mV, which causes lower V_{ds} (drain to source voltage) over the word line pass transistor (N3 in Fig. 4). Thus read power of 5T SRAM cell is reduced by 10% and 24% as compared to 7T SRAM, 6T SRAM cell respectively (see in Fig. 7).



Cell	Single-Vt [µW]	Dual-Vt [µW]
6T SRAM	45.69	39.42
5T SRAM	34.52	33.62
7T SRAM	38.6	35.47

Fig. 7. Read power consumption.

The comparison results for power consumed during read and write operation is shown in Fig. 8. The power is higher for 7T SRAM cell due to higher parasitic capacitance.

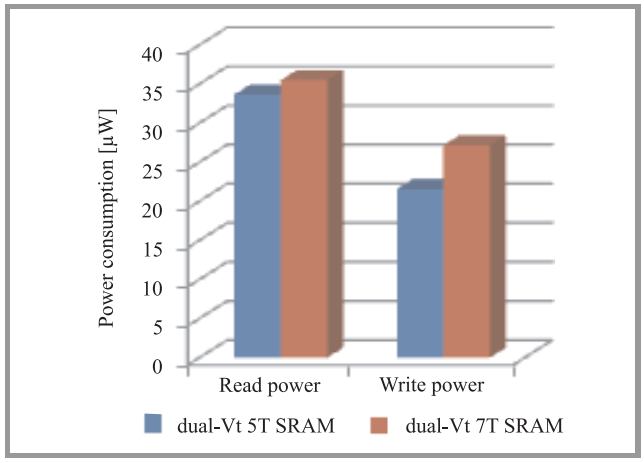


Fig. 8. Comparison between dual-Vt 5T SRAM cell and dual-Vt 7T SRAM cell on the basis of power consumption during read/write operations.

Due to the higher number of transistor used in 7T SRAM cell its leakage energy consumption increases. To reduce the leakage current in 7T SRAM dual-threshold voltage technology [20]–[27] has been used. High-threshold voltage transistors are not used for the access transistor as it increases the write delay. The threshold voltage for high-Vt and low-Vt NMOS/PMOS is shown in Table 5.

Table 5
Threshold voltage for low-Vt and high-Vt NMOS/PMOS transistors

Transistor	Low-Vt [V]	High-Vt [V]
PMOS	–0.2	–0.11
NMOS	0.47	0.76

As CMOS devices will continue to downscale into the deep nanometer range with improved device performance and lower power, it will be running into fundamental barriers of physics. Scaling below 45 nm channel length faces several fundamental limiting factors stemming from electron thermal energy and quantum mechanical tunneling. Hence in this paper we have designed SRAM at 180 nm and scaled it down to a limit of 65 nm, to study the variations occurred in power and delay factors of the memory. We can observe the effect of technology scaling on power consumption factor of SRAM memory cell in Figs. 9 and 10.

Thus technology scaling is an interesting way to lower the power consumption. Indeed, the overall parasitic capacitances (i.e., gates and interconnects) are decreased, the available active current per device is higher, and consequently, the same performance can be achieved with a lower supply voltage. It is evident from Figs. 9 and 10 that with technology scaling, power consumption decreases

by 80 to 90%, with some increase in write time (see in Fig. 11) because of the utilization of high-Vt transistors in write critical path.

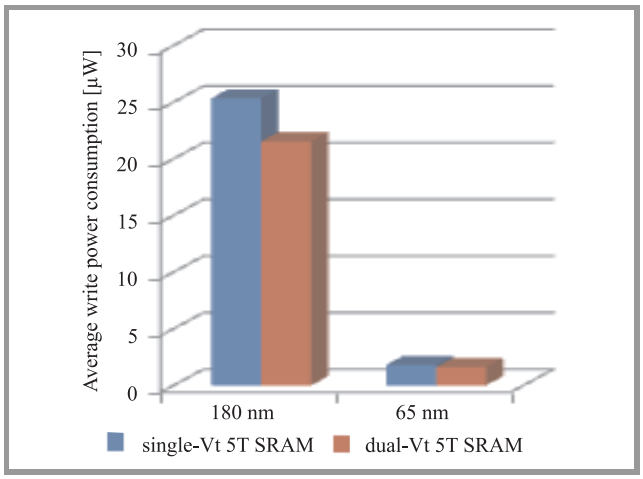


Fig. 9. Power reduction with the technology scaling in 5T SRAM cell.

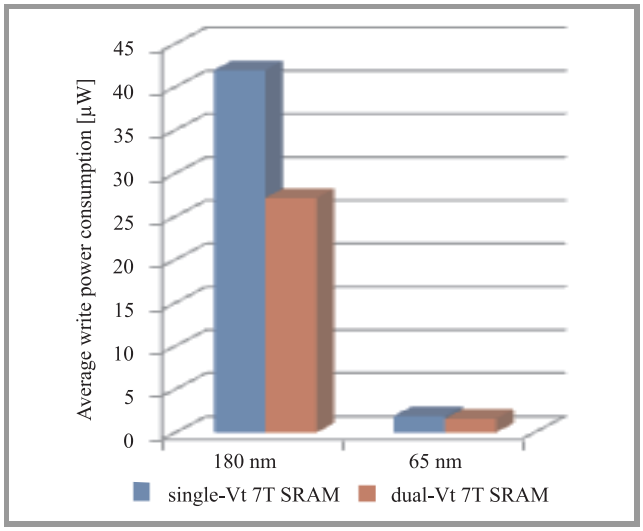


Fig. 10. Power reduction with the technology scaling in 7T SRAM cell.

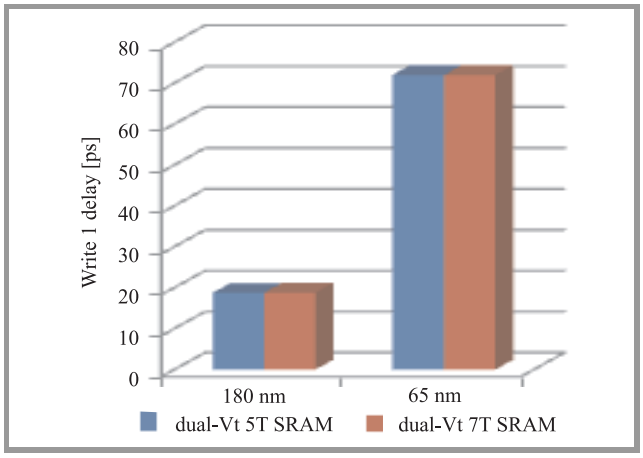


Fig. 11. Increase in write 1 delay as technology is scaled down.

3.2. Read/Write Delay Time

As shown in Fig. 12, 7T SRAM cell is not only robust but also is faster as compared to the 5T and 6T SRAM cells during a read operation. The read critical path is composed of two series transistors (N4 and N5) each sized twice a minimum sized transistor in 7T SRAM cell (see in Fig. 5).

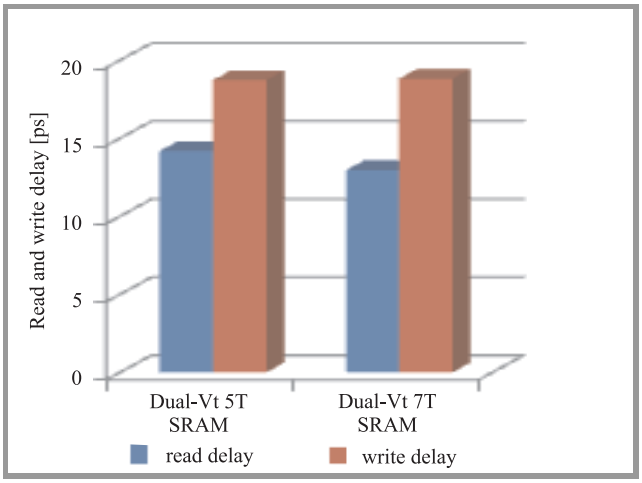


Fig. 12. Read and write delay comparison.

Alternatively, with the 5T SRAM cells, the read critical path are composed of series transistors (N3 and N1) with the access transistors (N3) sized stronger than driver transistor (N1) to maintain cell's read speed as shown in Fig. 4. The driving capability of the high-Vt transistor (N1) is lesser than any low-Vt transistor hence read delay of 5T SRAM increases. The read speed of 7T SRAM cell is 9% higher than 5T SRAM cell and 29% higher than 6T SRAM cell due to the lower resistance of the read access delay path.

The write speed, however, is degraded by 1 to 3% with the 7T and 5T SRAM cells as compared to the 6T SRAM cells due to the utilization of only a single bit line for writing into the cells with the proposed technique. This result is proving the fact that the write operation of single ended bit line SRAM cell is difficult because of strongly coupled inverters. Write 1 speed is slow because of NMOS pass transistor (N3 in Figs. 4 and 5) as it will pass weak 1 to the storage node (node1 in Figs. 4 and 5), so switching time of the memory cell get increased, as a result of this effect write 1 delay of 5T SRAM cell and 7T SRAM cell increased in comparison to 6T SRAM cell.

4. Conclusions

The 5T SRAM and 7T SRAM have been compared with respect to 6T SRAM. Read delay of 7T SRAM cell is 9% lesser than 5T SRAM cell because of the lower resistance of the read access delay path. Write delay of 5T SRAM and 7T SRAM is 1 to 2% higher than conven-

tional 6T SRAM cell due to single ended bit line architecture. Read power consumption of 5T SRAM is 10% lesser than 7T SRAM cell due to advantage of low voltage of bit line during read operation. 7T SRAM has 65% higher write power consumption as compared to 5T SRAM cell because RBL is at supply voltage during write operation which causes leakage power consumption. In this way we observe that 7T SRAM cell has high read speed with the loss of power. On the other hand 5T SRAM cell has benefit of low power consumption with the loss of read speed.

Acknowledgment

The authors thank the Director, UIET, Panjab University (Chandigarh), India for allowing to the work. The authors would like to thank to Panjab University, Chandigarh, India for providing excellent research environment to complete this work. The authors wish to thank all individuals who have contributed directly or indirectly in completing this research work.

References

[1] I. Carlson, S. Andersson, S. Natarajan, and A. Alvandpour, "A high density, low leakage, 5T SRAM for embedded caches", in *Proc. 30th Eur. Solid State Circ. Conf. ESSCIRC 2004*, Leuven, Belgium, 2004, pp. 215–218.

[2] M. Margala and M. Wieckowski, "A novel five-transistor (5T) SRAM cell for high performance cache", in *Proc. IEEE Int. SOC Conf. SOCC 2005*, Herndon, VA, USA, 2005, pp. 101–102.

[3] S. Cosemans, W. Dehaene, and F. Catthoor, "A low power embedded SRAM for wireless applications", in *Proc. IEEE 32nd Conf. Solid State Circuit*, Montreu, Switzerland, 2006.

[4] S. Cosemans, W. Dehaene, and F. Catthoor "A Low-Power Embedded SRAM for Wireless Applications", *IEEE J. Solid State Circuits*, vol. 42, no. 7, 2007.

[5] R. F. Hobson and H. Jarollahi, "Power and area efficient 5T-SRAM with improved performance for low-power SoC in 65 nm CMOS", in *IEEE 53rd Int. Midwest Symp. Circ. Sys. MWSCAS 2010*, Seatle, WA, USA, 2010, pp. 121–124.

[6] S. A. Tawfik and V. Kursun, "Low power and roubst 7T dual-Vt SRAM circuit", in *Proc. IEEE Int. Symp. Circ. Sys., ISCAS 2008*, Seatle, WA, USA, 2008, pp. 1452–1455.

[7] R. E. Aly, M. I. Faisal, and M. A. Bayoumi, "Novel 7T sram cell for low power cache design", in *Proc. IEEE Int. SOC Conf. SOCC 2005*, Herndon, VA, USA, 2005.

[8] R. E. Aly and M. A. Bayoumi, "Low-power cache design using 7T SRAM cell", *IEEE Trans. Circ. Sys.*, vol. 54, no. 4, 2007.

[9] J. Singh, J. Mathew, and K. D. Pradhan, "A subthreshold single ended I/O SRAM cell design for nanometer CMOS technologies", in *Proc. IEEE Int. SOC Conf. SOCC 2008*, Belfast, UK, 2008, pp. 243–246.

[10] M.-T. Chang, P.-T. Huang, and W. Hwang, "A robust ultra-low power asynchronous FIFO memory with self-adaptive power control", in *Proc. IEEE Int. SOC Conf. SOCC 2008*, Belfast, UK, 2008.

[11] T. Azam and B. Cheng, "Variability resilient low-power 7T-SRAM design for nano-scaled technologies", in *Proc. IEEE 11th Int. Symp. Quality Electron. Design*, San Jose, CA, USA, 2010.

[12] Z. Liu and V. Kursun, "High read stability and low leakage cache memory cell", in *Proc. IEEE Int. Symp. Circ. Sys.*, Cancun, Mexico, 2007, pp. 2774–2777.

[13] L. Chang *et al.*, "Stable SRAM cell design for the 32 nm node and beyond", in *Proc. IEEE Symp. VLSI Technol.*, Hsinchu, Taiwan, 2005, pp. 128–129.

[14] P. Athe and S. Dasgupta, "A comparative study of 6T, 8T and 9T decanano SRAM cell", in *Proc. IEEE Symp. Industrial Electron. Appl. ISIEA 2009*, Kuala Lumpur, Malaysia, 2009.

[15] G. Sery *et al.*, "Life is CMOS: Why chase life after?", in *Proc. IEEE Design Automation Conf.*, New Orleans, LA, USA, 2002, pp. 78–83.

[16] R. Keerthi and C. Chen, "Stability and static noise margin analysis of low-power SRAM", in *Proc. IEEE Int. Conf. Instrument. Measur. Technol.*, Victoria, BC, Canada, 2008.

[17] S. S. Rathod, S. Dasgupta, and A. K. Saxena, "Investigation of stack as a low power design technique for 6-T SRAM cell", in *Proc. IEEE Region 10th Conf. TENCON 2008*, Hyderabad, India, 2008.

[18] D. Hentrich, E. Oruklu, and J. Saniie, "Performance evaluation of SRAM cells in 22nm predictive CMOS technology", in *Proc. IEEE Int. Conf. Electro/Inform. Technol.*, Windsor, Ontario, Canada, 2009.

[19] S. Birla, N. Kr. Shukla, D. Mukherjee, and R. K. Singh, "Leakage Current reduction in 6T single cell SRAM at 90nm technology", in *Proc. IEEE Int. Conf. Advances Comput. Engin.*, Bangalore, Karnataka, India, 2010.

[20] C.-C. Wang, P.-M. Lee, and K.-L. Chen, "An SRAM design using dual threshold voltage transistors and low-power quenchers", *IEEE J. Solid State Circ.*, pp. 1712–1720, vol. 38, no. 10, 2003.

[21] B. Amelifard, M. Pedram, and F. Farzan, "Reducing the subthreshold and gate-tunneling leakage of SRAM cells using dual-Vt and dual-tox assignment", in *Proc. IEEE Conf. Design, Automation and Testing in Europe*, Munich, Germany, 2006, vol. 1, p. 1.

[22] F. Moradi, D. T. Wisland, H. Mahmoodi, Y. Berg, and T. V. Cao, "New SRAM design using body-bias techniques for ultra low power applications", in *Proc. IEEE 11th Int. Symp. Quality Electron. Design*, San Jose, CA, USA, 2010, p. 468.

[23] C. H. Kim and K. Roy, "Dynamic Vt SRAM: A leakage tolerant cache memory for low voltage microprocessors", in *Proc. Int. Symp. Low Power Electr. Design ISLPED'02*, Monterey, CA, USA, 2002, pp. 251–254.

[24] C. H. Kim and J.-J. Kim, "A forward body-biased low leakage SRAM cache: Device and architecture considerations", in *Proc. Int. Symp. Low Power Electr. Design ISLPED'03*, Seoul, Korea, 2003, pp. 6–9.

[25] B. Amelifard, F. Fallah, and M. Pedram, "Leakage minimization of SRAM cells in a dual-Vt and dual-tox technology", *IEEE Trans. on Very Large Scale Integra. Sys.*, vol. 16, no. 7, 2008.

[26] J. T. Kao and A. P. Chandrakasan, "Dual-threshold voltage techniques for low-power digital circuits", *IEEE J. Solid State Circ.*, vol. 35, no. 7, 2000.

[27] S. Panda, N. M. Kumar, and C. K. Sarkar, "Power, delay and noise optimization of a SRAM cell using a different threshold voltages and high performance output noise reduction circuit", in *Proc. Int. Conf. Comput. Devices for Commun. CODEC 2009*, Kolkata, India, 2009.

[28] K. W. Mai, T. Mori, and B. S. Amrutur, "Low-power SRAM design using half-swing pulse-mode techniques", *IEEE J. Solid State Circ.*, vol. 33, no. 11, 1998.

[29] E. J. Stine and H. Choday, "Single-ended half-swing low-power SRAM design", in *Proc. IEEE 42nd Conf. Signals, Sys. Comput.*, Pacific Grove, CA, USA, 2008, p. 2108.

[30] J. Singh, J. Mathew, and P. S. Mohanty, "Single ended static random access memory for low-vdd, high-speed embedded systems", in *Proc. IEEE 22nd Int. Conf. VLSI Design*, New Delhi, India, 2009.

Pragya Kushwaha is a final year student of M.Tech Microelectronics University Institute of Engineering and Technology, Panjab University, Chandigarh, India. She obtained her Bachelor Degree in Engineering (Electronics and Communication) from Raj Kumar Goel Institute of Technology, Ghaziabad, India, in 2009. Her area of research includes designing of low power memories at micrometer regime. Currently, she is working towards her thesis under the esteemed guidance of Dr. Amit Chaudhry.
E-mail: pragya189@gmail.com

Amit Chaudhry completed his Ph.D. in Microelectronics in 2010 from Panjab University, Chandigarh, India. He joined Panjab University, University Centre for Instrumentation and Microelectronics in October, 2002. He was responsible for teaching and research in VLSI and microelectronics to post graduate students. His research areas include device modeling for sub 100 nm MOSFETS. He is a life member of various societies in the area of microelectronics. Currently he is Senior Assistant Professor, University Institute of Engineering and Technology, Panjab University, Chandigarh. He has more than 35 publications in international journals/conference proceedings. He is a principle investigator in the Department of Information Technology (DIT) project on nanoscale and low temperature MOSFET modeling. He is a reviewer and member of editorial board of several peer reviewed international journals and highly reputed international conferences.
E-mail: amit_chaudhry01@yahoo.com
University Institute of Engineering and Technology
Panjab University
Chandigarh, India