# Silicon-germanium for ULSI

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**Abstract** — The paper describes recent progress for the introduction of silicon-germanium, bipolar and field effect heterostructure transistors into mainstream integrated circuit application. Basic underlying concepts and device architectures which give rise to the desired performance advantages are described together with the latest state-of-the-art results for HBT and MOSFET devices. The integration of such devices into viable HBT, BiCMOS and CMOS is reviewed. Other contributions that SiGe can make to enhance the performance of ULSI circuits are mentioned also.

*Keywords — silicon-germanium, HBT, SiGe-CMOS.*

## 1. Introduction

Pioneering work by Kasper et al at AEG (now Daimler-Chrysler) in the mid 1970s [1] and Bean et al at Bell Laboratories in the 1980's [2] gave rise to a new materials system for device engineers to employ. The associated heterojunction or band-gap engineering concept had been foreseen by both Shockley [3] and Kroemer [4] on a theoretical basis, in the earliest days of bipolar transistor technology. Seminal papers by Kroemer [5] in the 1980s have been inspirational to a generation of bipolar transistor device engineers resulting in the realisation of very high performance SiGe HBT devices with application to circuits which can operate in the lucrative $0.9 \div 5.8$ GHz mobile phone and wireless LANS markets. The potential for the use of SiGe alloy in MOSFET devices for CMOS and particularly BiCMOS application has been recognised by the major companies. In fact, a number of companies are now offering products aimed mainly at the mobile communications and satellite markets and a good set of links to these is maintained by Douglas Paul at Cambridge University UK [6]. The SiGe technology is developing very rapidly and is driven by the large corporations. Production level CVD batch systems have been developed by IBM [7] who also offer most of the parts to realise SiGe HBT, r.f. solutions (see „Whitepaper" on IBM web-site). The most mature SiGe device is the heterojunction bipolar transistor and many companies have viable production process with $f_T >> 50$ GHz, in many cases compatible with their BiCMOS process. The performance and integratability of the HBT device into CMOS manufacturing are key requirements for immediate markets. The high performance HBT has the potential to replace the III/V components in mobile products allowing an all-Si solution.

In this paper, the basic concepts, development and most recent state-of-the art device and technology results will be presented in the context of mainstream application. The contributions by some of the UK University community will be a particular focus. Section 2 contains an account of SiGe HBT which offers the easiest incorporation of the new material into relatively standard production processes. Some ideas for low voltage logic circuits based on concepts closer to Kroemer's vision are contained within this section also. Section 3 describes oxidation of SiGe. The production of good dielectrics, together with the abundance of Si constitute the two key reasons for the success of Si in the market place compared to other semiconductors. Section 4 reviews recent progress towards the realisation of SiGe CMOS and the final sections contain comments on SOI-SiGe, other applications of SiGe and conclusions.

## 2. Heterojunction bipolar transistor

The inclusion of SiGe alloy into the base of a bipolar transistor produces a narrow band gap base region, whereby most of the band discontinuity appears in the valence band edge. This is extremely fortuitous as the associated potential barrier effectively serves to inhibit the reverse injection of holes into the emitter. Hole transport into the emitter constitutes the dominant base current mechanism so the result is a large increase in the current gain, $\beta$. In the context of SiGe HBTs it is more appropriate to say that the base current remains the same as an equivalent all-Si device, but the collector current is enhanced by the presence of SiGe in the base which implies increased minority carrier injection. The result is the same and the very high gain can be traded by pushing up the base doping level to reduce base resistance. The heavily doped base can also be made very thin for reduced base transit, taking care to maintain an adequate Early voltage $V_A$, especially for the case of analogue devices. Lower doped emitters can be used to reduce base-emitter capacitance also. Thus devices can be designed with very high $f_T, f_{max}$ and also reduced base noise level. The Ge profile can be optimised for either digital (high $f_T$) or analogue (high $\beta V_A$) application as indicated in Fig. 1. A full account of physics and design issues together with details of process integration for 0.25 μm BiCMOS has been reported by IBM [8, 9]. The SiGe base is produced by epitaxy for optimal performance and is relatively easy to introduce into a manufacturing process with only marginal cost penalty.

The schematic diagram of Fig. 2 illustrates the IBM BiCMOS process. Extremely impressive performance has been reported for SiGe HBT's, with values of $f_T$ and $f_{max}$ of 130 [10] and 160 GHz [11] respectively and gate delays of 11 ps [12]. An 0.2 μm, near to BiCMOS compatible SiGe HBT technology was recently reported by Hitachi, with 107 GHz $f_{max}$ and 6.7 ps ECL ring oscillator delay [13]. The HBT showed 47 GHz $f_T$ at a lower current of 0.1 mA showing the potential for low power operation.
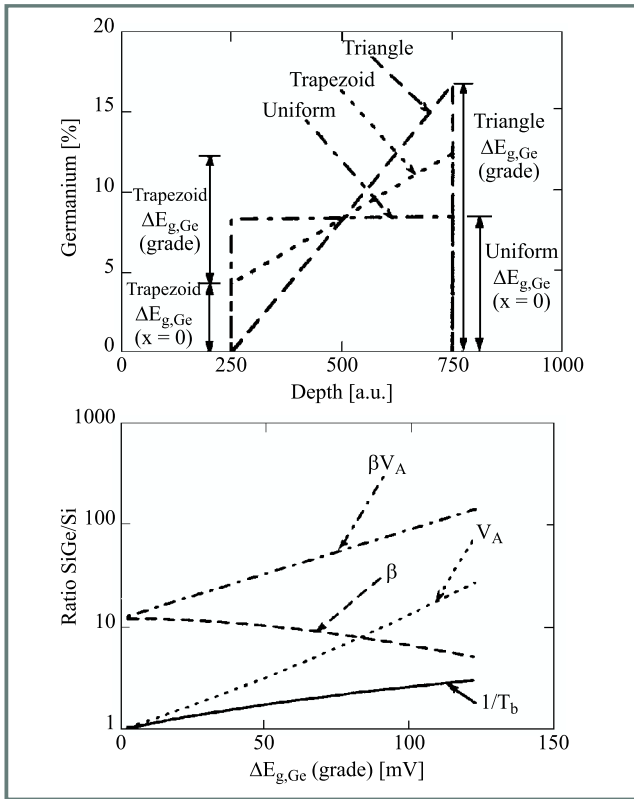
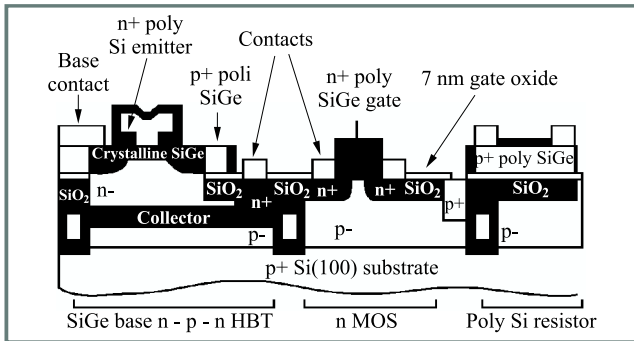**Fig. 1.** Optimisation of base Ge profile for different applications (*reproduced from [8]*).



**Fig. 2.** Schematic diagram of IBM SiGE HBT BiCMOS process [8] (*diagram reproduced from [27]*).



**Fig. 3.** State-of the-art SiGe HBT: selective SiGe epitaxial base, self-aligned stacked metal/in-situ doped poly-Si (SMI) electrodes, trench isolation [13].

As illustrated in Fig. 3, these devices are highly optimised in both the vertical and lateral dimensions, for high $f_T$ and $f_{max}$ respectively. Full integration of 55/90 $f_T/f_{max}$ SiGe:C HBTs into a 0.25 μm BiCMOS process has been reported [14]. Note that carbon is incorporated to suppress B out-diffusion of the base. This out-diffusion is a particular problem of SiGe HBT technology because of the very highly doped base bounded by relatively lightly doped collector and emitter regions. The propensity for B out-diffusion is exacerbated by Si interstitial injection following extrinsic base implants: so-called transient enhanced diffusion. The out-diffusion causes parasitic barriers to be formed in the conduction band edge, reducing collector current and hence $f_T$. Thin, undoped SiGe spacer layers can help to allevi-
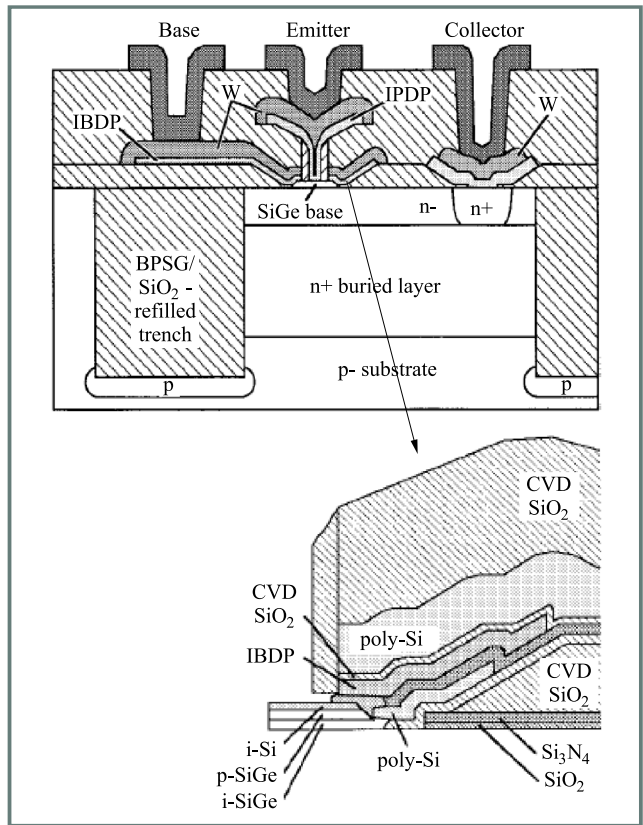
ate the problem. Parasitic barriers can also form at high injection levels: the „modified Kirk effect".

The initial approach by industry was to introduce the heterojunction into their standard poly-Si emitter processes and this does not bring the full benefits of the band-gap engineering concept. The primary motivation was the reduction of noise and perhaps most importantly, an early introduction of products into the market place. A further possible quick route to production is offered by forming the SiGe by Ge implantation [15] and this may be particularly useful for improving the performance of the p-n-p device for analogue application. There are considerable materials problems to overcome although the use of subsequent Si amorphisation and regrowth (EPIFAB process) pushes end of range defects deep into the substrate and can improve material quality [16].

The optimum route to achieve a truly optimised HBT involves selective and non-selective epitaxial growth and this strategy has been used in the state-of-the-art results achieved so far. The concept is illustrated in the architecture shown in Fig. 4 which shows a collector region grown with selective epitaxial growth (SEG) in an oxide window followed by a non-selectively grown (NSEG) base region and low doped emitter. A poly-Si emitter contact can be used to further increase gain. Such an approach allows full exploitation of the heterostructure principle although prob-
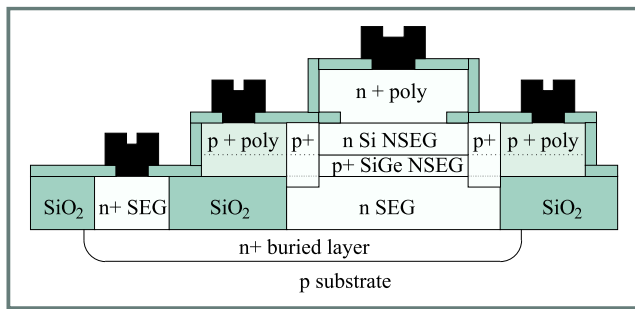
**Fig. 4.** Schematic diagram of SiGe HBT produced using selective epitaxy [17].

lems can exist with excess leakage currents at the collector periphery [17].

An advantage of HBT's is the reduced charge storage and this has initiated a re-appraisal of saturated logic families which can operate at very low voltages. Such a logic family is integrated injection logic ($I^2L$) which comprises of n-p-n switching transistors operating in inverse mode with integrated p-n-p [18] or resistive loads [19]. Gate delays down to 60 ps have been suggested by simulation; performance which is considerably slower than that of HBT-ECL. Nevertheless, the very low voltage effect supply voltage ($\sim 0.8$ V), low power-delay product and high packing density looks attractive for mobile, mixed signal environments. The use of resistive loads rather the (poor) lateral p-n-p load can reduce $I^2L$ gate delay further [19]. The SEG/NSEG approach allows self-aligned gate architectures closer to Kroemer's original vision whereby arrays of transistor operating in both normal and inverse modes can be realised in oxide windows to produce very compact low voltage circuits, as illustrated schematically in Fig. 5. The
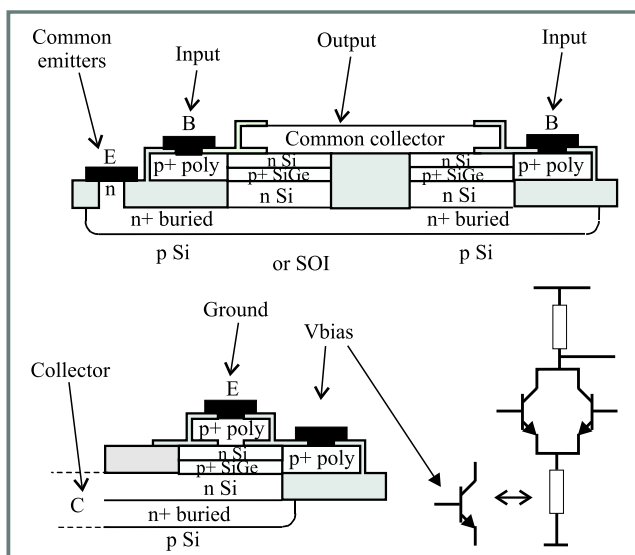


**Fig. 5.** Concept for high packing density, low voltage SiGe HBT logic. Top schematic shows emitter-down switches forming NOR logic; bottom diagram illustrates integration of an active bias (emitter-up) which could replace bottom resistor.

inherent symmetry of SiGe-HBT's is particularly suitable for collector up mode of operation and such HBTs with $f_{max} = 33$ GHz have been reported recently [20].

# 3. Oxidation of SiGe

The ability to realise a high quality dielectric and interface with semiconductor is a key factor in the success of Si technology. It is important that the incorporation of SiGe into the process flow does not compromise dielectric integrity. Growth rate enhancement (GRE) is apparent for wet thermal oxidation of SiGe but not for dry oxidation [21]. Our own experiments on low temperature plasma anodisation, using the system shown in Fig. 6, also show GRE but no Ge snow-plough [22, 23]. It has been suggested that oxida-
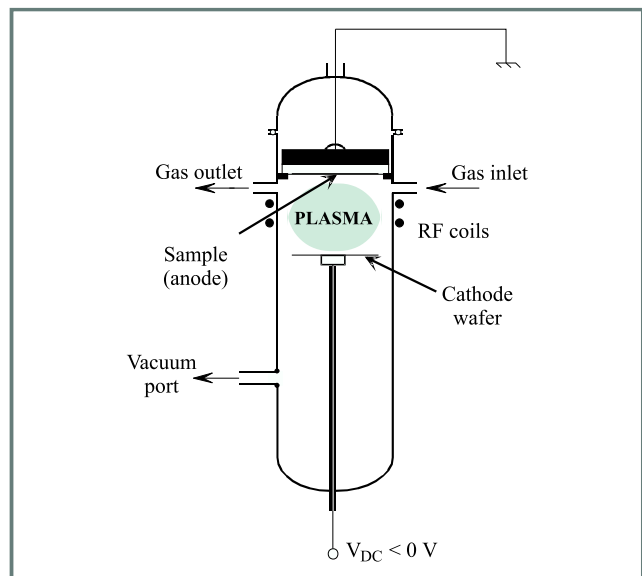


**Fig. 6.** Low temperature plasma anodisation system which allows growth of oxides at room temperature.

tion regimes that are surface reaction rate limited tend to lead to snow-ploughing of Ge from the growing film [22]. This produces a Ge-rich interface with high fast state density which is unsuitable with regard to both gate oxide and passivation application. Oxidation regimes that are mass transport limited tend to preclude snow ploughing of Ge and the surface can be inverted to allow transistor action [24] but the presence of unoxidised Ge in the oxide constitutes electron traps which compromise reliability [23]. It is unlikely that such effects can be overcome and the conclusion must be that direct oxidation of SiGe should be avoided. For this reason, the use of sacrificial Si capping layers that are partly consumed by gate oxidation is usual in SiGe MOS processes. Implanted Ge HBT processes can experience problems with poly-Si emitter/base engineering, associated with oxide growth rate enhancement. Reliability problems associated with SiGe HBTs as a result of SiGe oxidation are as yet unclear although it is likely that SiGe layers can be kept away from interfaces with dielectric by design. A further issue concerns the thermal budget for

the incorporation of strained layers into IC processes and the use of low temperature oxidation processes may be of interest in this regard in the future (see [22] for a review).

# 4. SiGe MOSTs and H-CMOS

The incorporation of SiGe into CMOS technology is far more problematic than that of SiGe HBTs into bipolar or even BiCMOS process flows. The motivation for incorporating SiGe is firstly that hole mobility can be enhanced allowing better matching of the p-channel and n-channel devices and there is also the potential for higher mobilities ($\mu$) for both carrier types. This will increase drive capability which is the critical factor for both sub-micron (device length, $L$) technologies where the „$\mu/L^2$" rule applies and very deep sub-micron technologies where interconnect capacitance becomes dominant. The key issue is that the added complexity of the SiGe CMOS process must bring sufficient benefit to be commercially viable. There are essentially two classes of device and both are constructed from successive layers of epitaxial material. The first is the modulation doped FET (MODFET), shown schematically in Fig. 7, which employs the so-called modulation doping concept whereby the channel is formed in undoped material with carriers provided by an adjacent doped layer. A conducting sheet of charge typically of the order low
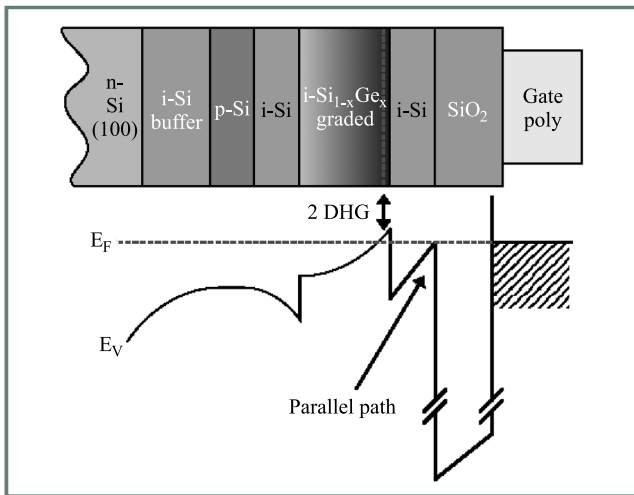


Fig. 8. Epitaxial layer structure illustrating the heterojunction MOS concept [34] (*diagram reproduced from [27]*).



Fig. 7. Epitaxial layer structure illustrating the modulation doping concept [25] (*diagram reproduced from [27]*).

$10^{12}$ cm$^{-2}$ thus exists prior to application of the gate voltage. Alternatively, a heterostructure device without doping can be produced with carriers induced purely by gating, as outlined in Fig. 8.

As discussed in the previous section, there is a need to avoid the direct oxidation of SiGe and so a Si capping layer, upon which the gate oxide is formed, is included on top of the SiGe channel layer. The channel is thus buried and the transport is away from the comparitively rough Si/SiO$_2$ interface providing a further source of mobility improvement. Simple devices incorporating a so-called pseudo-
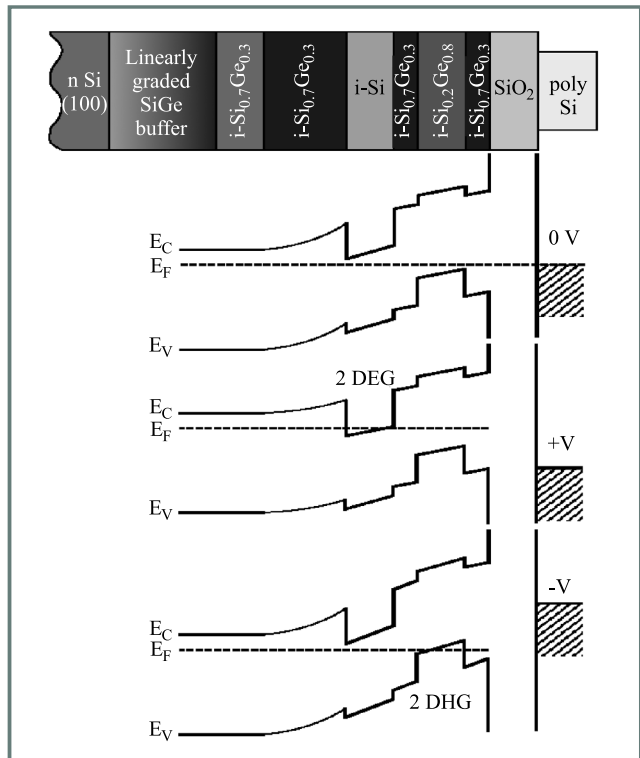
morphic SiGe layer has the band gap discontinuity in the valence band edge providing confinement of holes to form a buried channel. This means the device is suitable for p-MOST realisation but not for n-MOST. In terms of CMOS, this means that SiGe is incorporated into the p-channel device only; the n-MOST can be a conventional surface channel device. An important early study [25] produced a MODFET with best hole mobility of 220 cm$^2$ V$^{-1}$s$^{-1}$ which is probably too low to justify the added complexity of incorporating the SiGe layer. Most recently, a high performance p-MODFET with a mobility of 930 cm$^2$ V$^{-1}$s$^{-1}$ has been reported [26]. A preliminary study using low temperature grown gate oxides has produced both p- and n-channel devices with SiGe surface channels [24]. The device concept features surface channels of intrinsic SiGe and employs a sacrificial Si capping layer which is consumed by the plasma oxidation. The concept relies on the planarisation effect of PO whereby any surface roughness leads to field intensification.

More encouraging results have been obtained for devices built on so-called virtual substrates comprising of a linearly graded SiGe epitaxial buffer layer on a Si substrate. The grading serves to direct defects downwards away from the surface and in principle, very low defect density surfaces can be produced by this means. A further layer is grown and depending on the Ge concentration, band-edge discontinuities in either conduction or valence band can be realised so that both p- and n-channel buried channels can be formed. This approach may offer the best route to CMOS although there are considerable materials prob-

lems to overcome to realise reliably, low defect density virtual substrates, as reviewed in [27]. Record mobilities of 2830 cm$^2$ V$^{-1}$s$^{-1}$ and 1300 cm$^2$ V$^{-1}$s$^{-1}$ have been reported for n-MODFETs [28] and p-MODFETs respectively [29]. Fig. 9 shows relative performance of field effect devices [27] whereby SiGe n-MODFETs exhibit $f_T$ comparable to III/V MODFETs and p-MODFETs show record performance.
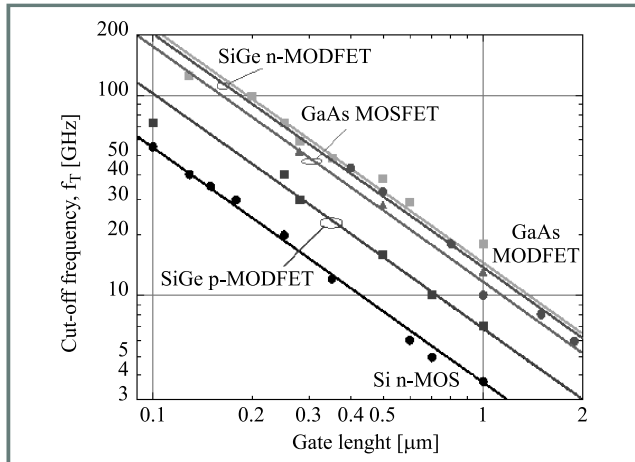


**Fig. 9.** Relative performance of high frequency field effect devices [27].

The conclusion from the individual device studies is that best results are obtained for a strained Si channel n-FET and strained SiGe (or Ge) channel p-FET [30]. The former devices have comparable speed performance to III/V devices and p-MODFETs have exhibited order of magnitude mobility improvements over conventional p-MOSFETs. Silicon based MODFETs have further advantages to III/V counterparts as a result of the better thermal conduction properties of Si although further work is required to ascertain noise performance. To implement these devices into CMOS production introduces a fresh set of problems. Progress into CMOS realisation has been reviewed by Maiti et al [31] and Schäffler [32]. The aim is to realise both n- and p-channel devices in a single set of epitaxial layers, without the requirement to return the wafers to the growth chamber. Designs have been reported based on modulation doping and more conventional MOSFET action. The devices have employed either Schottky or MOS gating. An early implementation [33] of CMOS employed a mesa isolation strategy similar to that of III/Vs. A n-MODFET was formed on a strain relaxed SiGe buffer. These layers were etched away locally to allow formation of a lower-level pseudo-morphic SiGe channel p-MODFET. Schottky gates were used. Downward penetrating defects from the buffer layer made the p-channel device unacceptably poor however. A somewhat similar concept also employing (Pt) Schottky gates was suggested by Ishmail [30]. For commercial processes, MOS gates are preferred to Schottky gates for reasons of leakage, reproducibility and reliability. The aim also is to produce both device types on the same strain-adjusting layer thus avoiding the need for local removal of

layers and maintaining planarity. Note that compromises are required in the individual device design as it is not feasible to produce separate virtual substrate layers individually for p- and n-channel devices. The planar CMOS concept of Ishmail [30], later reported by Sadek et al [34] and illustrated in Fig. 10, uses a 30% Ge, SiGe virtual substrate with a strained Si channel n-MOSFET and a subsequent SiGe (> 70% Ge) channel for the p-MOSFET. Common
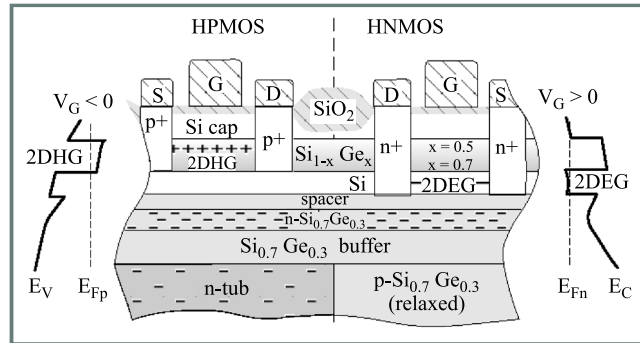


**Fig. 10.** Complementary HMOSFET with a Si channel for the n-type and an SiGe channel for the p-type device. A common relaxed buffer is used for both transistors [34] (*diagram reproduced from [32]*).

gate material of p+ poly-Si can be used if layer dopings are adjusted appropriately, to produce quite low threshold voltage (< 0.4 V) required for low power operation. Full CMOS with a SiGe p-MODFET and conventional surface channel n-MOSFET has been realised with hole mobility of over 320 cm$^2$ V$^{-1}$s$^{-1}$ [35], using LTO deposited and plasma anodic gate oxides. Finally, large electron and hole mobilities (> 2000 cm$^2$ V$^{-1}$s$^{-1}$) have been predicted for strained Si channels [36]. The ability to use strained Si for both channels suggests a simpler CMOS process.

# 5. Other applications of SiGe

Silicon germanium has been used in a number of other ways in IC processes. Vertical MOSFETs can benefit from a SiGe source region: a reverse heterojunction effect whereby the gain of the parasitic bipolar transistor formed by source/body/drain is reduced considerably giving higher breakdown voltage for the MOST [37]. Poly-SiGe (50% Ge) looks attractive as an alternative gate electrode material for reduced threshold voltages and common gate material in CMOS application [38], where the work function can be tailored by the Ge concentration. Gate poly depletion effects are ameliorated also by the enhanced dopant activation at low temperatures. Implanted Ge in the drain region of MOSFETs can alleviate hot electron effects due to the reduced ionisation threshold arising from the lower band gap [39]. SiGe can also be used as an etch-stop in bonded wafer SOI technology. The temperature coefficient of resistance can be controlled in polycrystalline SiGe resistors for better thermal performance. Finally, thin film poly SiGe transistors offer higher carrier mobility for large area

electronics whereby pixel addressing driver circuitry can be realised on the flat panel displays for a cheaper solution.

# 6. SiGe-on-insulator

Introduction of silicon-on-insulator substrates brings additional benefits to the fabrication of SiGe MOSFETs as well as the inherent advantages of SOI technology in its own right. For MOS application, the elasticity of the buried insulator can help reduce the defect density of SiGe layers and also provide a simplified CMOS process to aid integration of SiGe into the process flow. SOI brings its own benefits including ease of isolation, reduced drain/source and bulk capacitances and increased packing density [40]. A recent result from Toshiba [41] demonstrates hole mobilities greater than the universal mobility of Si for non-optimised layer structure. For HBT's, SOI substrates offer reduced collector to substrate capacitance as well as ease of isolation. A 60 GHz $f_T$ super self-aligned HBT on SOI has been realised by NEC fabricated on SOI substrate and its application to 20 Gbit/s optical transmitter IC's demonstrated [42]. An advanced technology for r.f. application has been proposed whereby an SOI-SiGe HBT has been realised using bonded wafer technology and is illustrated schematically in Fig. 11. The buried ground plane produces
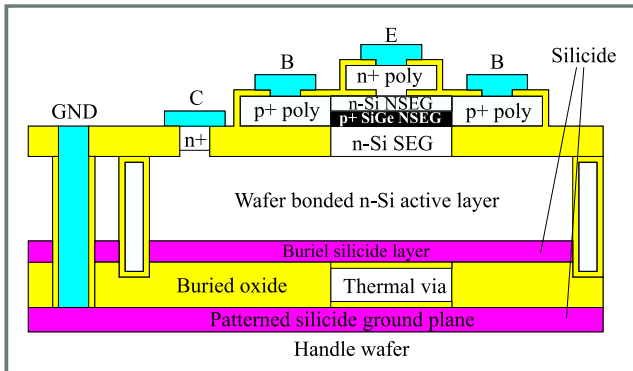


**Fig. 11.** Schematic of the „ultimate" r.f. transistor featuring SEG/NSEG epitaxial growth, trench isolation, SOI substrate with thermal vias. Low resistance silicide layer for low collector resistance and buried ground plane under the buried oxide, for cross-talk suppression. (*By kind permission Prof. P. Ashburn, Southampton University, UK, Prof. H. S. Gamble, Queen's University Belfast, UK*).

effective screening of analogue and digital circuits on the same substrate (mixed signal). This buried ground plane concept has been demonstrated to achieve nearly −90 dB suppression of substrate cross-talk [43]. The technology also features thermal vias to allow the heat to escape – a significant problem with SOI technology particularly for analogue application. Heating can cause thermal run-away in HBT's and reduction of drive capability due to mobility degradation in MOSFET devices.

# 7. Conclusions

SiGe can be used to further improve Si bipolar and MOSFET device performance in quite a wide variety of ways. SiGe BiCMOS is undoubtedly the main driver for the industry in the short term, because of the benefits it can bring to wireless markets. A number of products are also available in SiGe HBT where the low noise and high frequency of operation are particularly noteworthy. Some doubt remains as to whether full SiGe CMOS will make it to the market place due to the high costs of new fabrication plants and the need to comply with the SIA roadmap. In any event, it may be that other technologies such as SOI can provide the improved performance in a more cost-effective way. It is conceivable that both SOI and SiGe CMOS will be used for a „last generation" of CMOS when existing scaling strategies run out of steam. However, it is almost certain that SiGe material will find a place in mainstream ULSI CMOS in some capacity and a likely contender is its use as gate material for low power application.

# Acknowledgements

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