Invited paper

Roadmap for SiC power devices

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Abstract — Silicon carbide (SiC) power devices offer significant benefits of improved efficiency, dynamic performance and reliability of electronic and electric systems. The challenges and prospects of SiC power device development are reviewed considering different device types. A close correlation between an exponential increase of current handling capability during recent five years and improvement in substrate quality is demonstrated. The voltage range of silicon and SiC unipolar and bipolar power devices with respect to the on-state voltage is determined based on device simulation. 4H-SiC unipolar devices are potentially superior to all silicon devices up to 10 kV. 4H-SiC unipolar devices are superior to all SiC bipolar devices up to 8÷9 kV. The low end of SiC unipolar devices is determined to be around 200 V provided substrate resistance is reduced by thinning the substrate down to 100 μm. The influence of reduced channel mobility on the specific on-state resistance of 4H-SiC DMOSFETs and UMOSFETs is shown. It has been demonstrated that 6H-SiC DMOSFETs could be a better choice compared to 4H-SiC MOSFETs in the voltage range below 600 V utilising better channel mobility obtainable so far on 6H-SiC polytype. An impact of super junction (SJ) concept on silicon and SiC MOSFET specific on-resistance limits is demonstrated.

Keywords — SiC power devices, roadmap for, status, development trends, unipolar and bipolar SiC devices, super junction devices, applications, system benefits, current handling capability, simulations.

1. Introduction

Silicon carbide is an example of a so-called wide band gap semiconductor, a material whose electronic and physical properties promise a major qualitative leap in semiconductor device performance. Intense research and development has been going on throughout the last decade in many centres over the world. In particular, activities in Sweden have been at the forefront of development. The beginning of the new century represents the threshold for commercialisation of SiC based devices. A number of companies are announcing the release of products and the number of material producers has multiplied four-fold.

2. Applications of power devices

Emerging WBG (wide band gap) semiconductor devices, of which silicon carbide is currently the most mature, face a well-established market of power electronics practically totally dominated by silicon devices. Silicon carbide power devices have high potential of finding its way into the mainstream applications and of capturing important parts of the market thanks to the specific material properties of SiC that translate into high value added for electronic power systems. Specifically high electric field breakdown in combination with reasonably high electron mobility and high thermal conductivity translate into improved efficiency, dynamic performance and reliability of electronic and electric systems. It is relatively straightforward to envision savings on cooling requirements connected with increased working temperature of the devices well above 125°C typical of silicon power devices as well as reduced noise, size and weight of systems due to greatly increased operating frequency. To overcome both limitations has long been desired in especially high voltage applications above 1 kV where bipolar silicon devices must be used. Such devices are necessarily slow and suffer from high switching losses due to substantial recovery charge that makes them the limiting component in terms of performance of many systems.

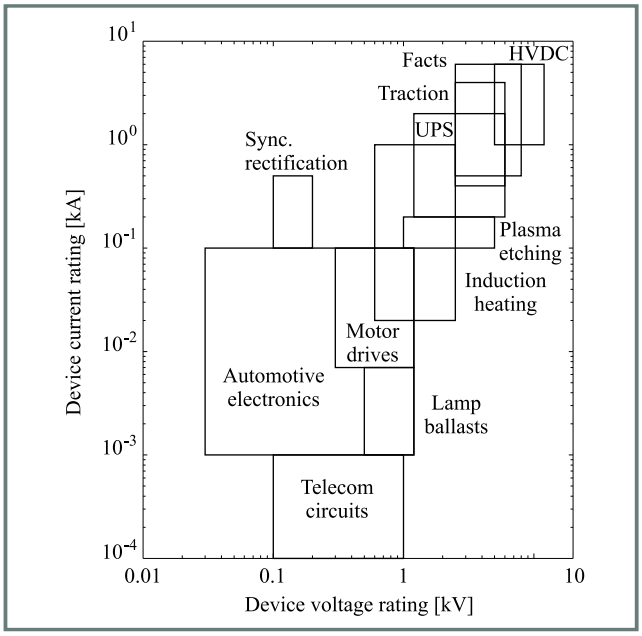

Fig. 1. Current and voltage ratings of power devices used in different applications.

In Fig. 1 applications for power devices are summarised in relation to required current and voltage ratings. In Fig. 2 the same applications are summarised in relation to required device power ratings and operating frequency. Types of silicon power devices used in different applications are shown in the graph.

3. System benefits of WBG semiconductors

In general SiC power devices have compared to Si power devices the advantages of lower on-state voltage drop for

Table 1
System benefits of WBG semiconductors

Device properties	System benefits	Driver
Low on-state voltage Low recovery charge Fast turn-off and turn-on High blocking voltage Higher junction temperature High power density	Higher efficiency Higher frequency Reduced noise Smaller size and weight – reduced value of reactive components – fewer devices stacked in series – smaller size of heat-sink – natural convection – saving costs of forced convection and fans	Power distribution and conditioning HVDC FACTS Motor drives UPS

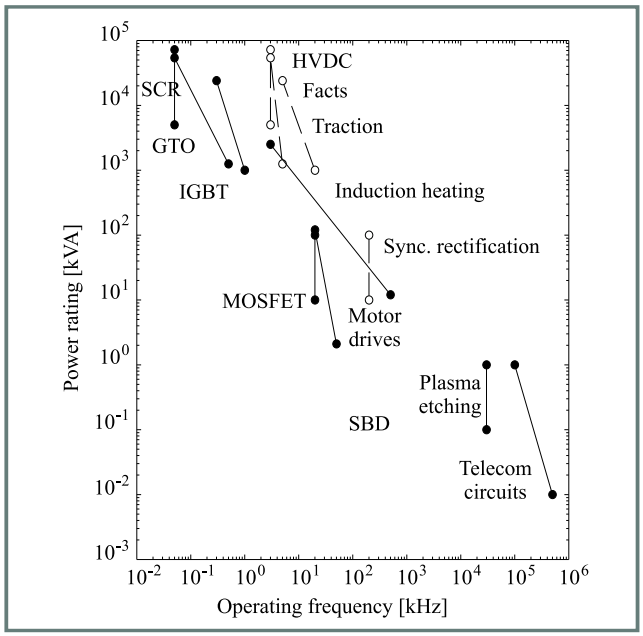

Fig. 2. Device power rating and operation frequency for different applications. The desired operation frequency is shown by empty symbols and dashed lines. The type of silicon power devices used today in different power and frequency ranges is shown as well.

unipolar devices (lower specific on-resistance) as well as excellent dynamic characteristics, high switching speed and low losses for both unipolar and bipolar devices due to extremely low recovery currents. Furthermore, they have theoretical potential of handling 100 times higher power density making possible higher packing density of device chips and reduction of the size of power devices [1–4].

In short SiC devices are an obvious choice in all applications where low R_{on} (alt. low conduction losses), high frequency (alt. low switching losses) and working temperature above 150°C (alt. reduced cooling requirements) lead to significant system benefits.

The predicted benefits of introducing SiC power devices in the electronic power systems are summarised in Table 1.

4. Silicon carbide device development trends

Development of SiC devices in terms of voltage handling capability has been remarkably fast ever since the first commercial material from Cree Research Inc. became available in 1993. High voltage capability has been demonstrated in almost all types of SiC power devices. The progress in terms of voltage blocking capability has been controlled by the availability of low doped thick epitaxial layers. The evolution of blocking voltages follows closely the constant improvements in CVD epitaxial growth of low doped n-type layers and their commercial availability. Schottky barrier diodes have been demonstrated with blocking voltages of 1.75 kV and 3.0 kV (1996 and 1998, Kyoto University and Linköping University, respectively) [5, 6] and 4.9 kV (1999, Purdue University) [7]. PiN diodes were made blocking voltages of 2.0 kV (1993, NASA Lewis Research) [8], 4.5 kV (1995, ACREO (IMC)) [9], 6.2 kV (1999, Cree Research/Kansai Electric Power) [10] and 8.6 kV (1999, Cree Research) [11]. PiN diodes blocking over 4.5 kV have been repeatedly done within ABB/KTH facilities in Kista. JBS diodes blocking 1.8 kV (1998, ABB/ACREO (IMC)/Daimler-Benz) [3] and 3.6 kV (1999, Cree Research/Kansai Electric Power) [12] and 3.7 kV (2000, Hitachi/Kansai Electric Power) [13] have been demonstrated. High voltage MOSFET devices have been made, like 1.4 kV trench UMOSFET (1997, Northrope-Grumman) [14], lateral 2.6 kV implanted DMOSFET (1997, Purdue University) [15] and recently 1.4 kV UMOSFET (1998, Cree Research/Kansai Electric Power) [16] and 1.8 kV DMOSFET (1999, Siemens) [17]. Other unipolar switches include high voltage 1.8 kV vertical JFET (1998 and 2000, respectively, Siemens) [18, 19] and 2.0÷4.5 kV vertical JFETs (2000, Cree Research/Kansai Electric Power) [20]. Also bipolar devices like GTO thyristors with blocking voltage of 1.0 kV (1997, Northrope-Grumman) [21] and 2.6 kV (1999, Cree Research) [22] were demonstrated.

However development of current handling capability has been slow up to now and limited by the quality of the

material and more specifically by the size of the defect free areas on the SiC wafers.

4.1. Material development

The increase in substrate size has been dramatic over the last three years, motivated by the prospect for SiC technology to enter production phase (see Fig. 3). Today both 50 and 75 mm wafers can be purchased and 100 mm wafers

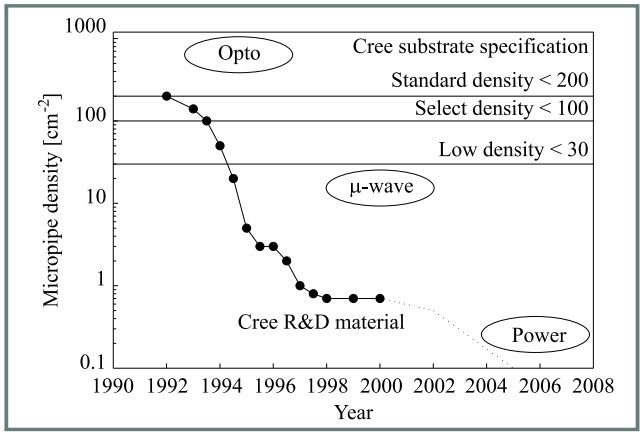

Fig. 3. The evolution of SiC wafer size from Cree Research [24].

have been demonstrated. It is likely that 100 mm wafers will be offered for sale within three years and that even larger substrates are demonstrated during the same period. The introduction of 100 mm or 4 inch substrates can be the turning point for SiC device production since much of the equipment used for processing Si can also be used for SiC. Market introduction of the SiC technology requires in addition to the reasonable wafer size an adequate quality of the semiconductor material. All the SiC power devices require at least one epitaxial layer with controlled doping and thickness to be grown on top of the highly doped substrates. The major limiting factor for the quality of SiC epitaxial films is the substrate material itself. Even if the development of SiC substrates has been successful during the last five to ten years the quality is still extremely poor compared to the substrates of other commercially available semiconductor materials.

Epitaxial layers typically contain a high density of detrimental defects like dislocations (10^5 cm^{-2}), micropipes (100 cm^{-2}) and polytype inclusions (10%), the majority of which propagate from the bulk of the substrate into the epi-layers. In addition, other defects that are generated during epitaxial growth include different growth pits ($10^2 \div 10^4$ cm^{-2}) most likely caused by substrate surface damage introduced during cutting and polishing. Since the defect free areas of the substrates today are relatively small, market factors dictate that only small area devices, like μ-wave frequency MESFETs, are economically feasible to produce. Production of large area power devices requires further significant increase of at least the micropipe free areas on the substrates (see Fig. 4). For this reason

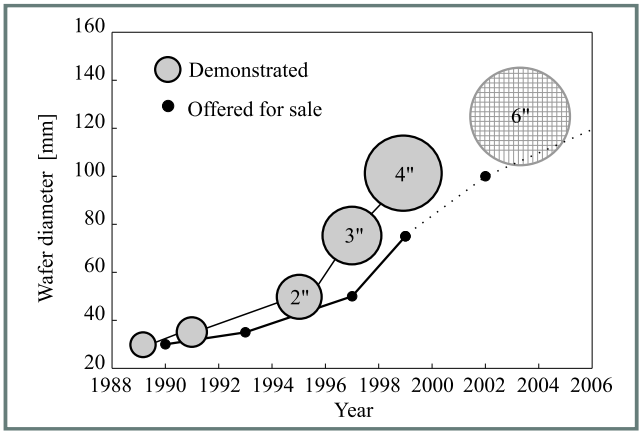

Fig. 4. The evolution of micropipe density in best R & D wafers from Cree Research [24].

multi-chip press-pack and wire-bonded module solutions are being developed and tested [16, 23].

4.2. Current handling capability

All available data point to a close correlation between the yield (measured in terms of static blocking capability) and micropipe density in the substrates. This is demonstrated in Figs. 5 and 6. In Fig. 5 development of the maximum chip

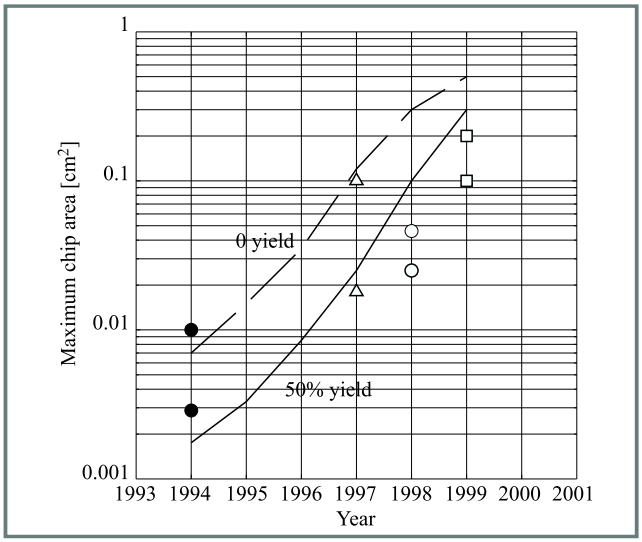

Fig. 5. Evolution of maximum chip area for estimated yield of 50% (solid line) and 0% (dashed line) based on PiN diode data (lines). Also there are shown estimated maximum areas based on SBD data from Purdue University (△) [25], and Siemens (◯) [26], on JBS data from DaimlerChrysler (□) [27], and on JFET data from NASA Lewis Research Center (•) [28].

size in time is shown as determined from the available yield data for PiN rectifiers (lines) and Schottky (SBD) rectifiers (empty symbols). The data by others are used to verify our own data. The lower line (and symbol) corresponds to a yield of 50% and upper line (and symbol) to a 0% yield as determined applying Poisson distribution model to the yield data measured on diodes of different size processed on the same wafers. In Fig. 6 the defect density extracted

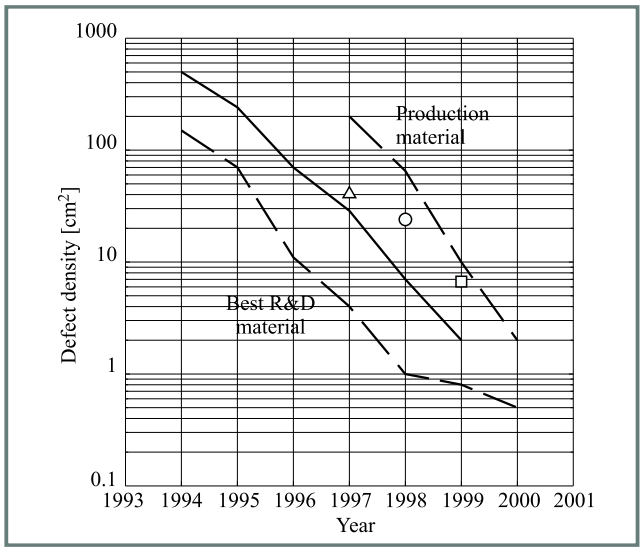

Fig. 6. Defect density extracted from yield data using Poisson model as illustrated in Fig. 7 and micropipe density in Cree Research substrates after ref. [24]. The time scale is that of publication (one year has been added to the wafer manufacturing date).

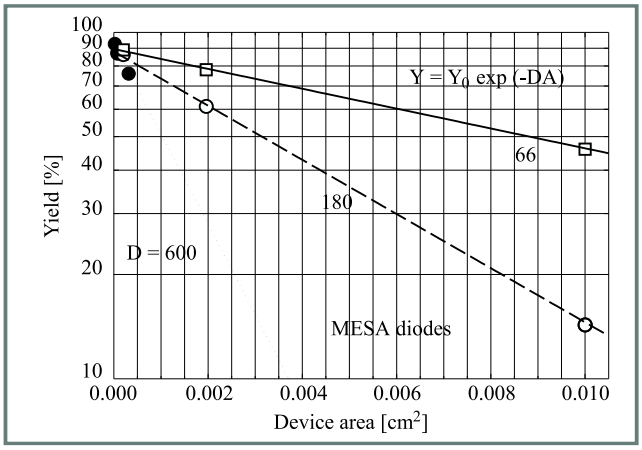

Fig. 7. Extraction of defect density and maximum chip area for a given yield for three different wafers each containing diodes with three different diameters. The Poisson yield model is used as shown in the figure. The diodes were processed 1994, 1995 and 1996, respectively.

using Poisson model from PiN diode data (solid line) and SBD data (empty symbols) is plotted together with micropipe density data published by Cree Research for their best material (lower dashed line) and standard production grade material (upper dashed line) [24]. The time axis for the substrate data was shifted one year forward to account for the fact that it takes about one year from the time the material is made to the time the devices are measured and data presented at a conference. The correlation between the defect density obtained from Poisson model and those from micropipe defect density in substrate material is astonishing. An example of extraction procedure is shown in Fig. 7 where static blocking voltage yield data are plotted for PiN diodes of different size from the same wafer processed 1994, 1995 and 1996 (SiC substrates from Cree Research were produced 1993, 1994 and 1995, respectively). Latest PiN data are based on reference [23]. The data are fitted with a function $Y = Y_0 \exp(-D \cdot A)$ where D is defect density and A is device area. The value (100%-Y_0) is a measure of „dead" area. Usually the area close to the edge of the wafer has much higher concentration of defects than the rest of the wafer. Devices in this area have not been excluded beforehand when calculating the yield. The percentages of dead area and the fatal defect densities for the wafers in Fig. 7 are 7% and 600 cm^{-2}, 12% and 180 cm^{-2} and 10% and 66 cm^{-2}, respectively. All the devices were processed on the Cree Research substrates. The epitaxial layers were grown at different sites. At Linköping University (PiNs), at Siemens (Siemens SBDs), at Nasa Lewis (NASA Lewis JFETs) and at Cree Research (Purdue Universities SBDs and DaimlerChrysler JBS diodes).

Micropipes appear to be the dominant single type of defect when it comes to yield based on the static blocking capability. As the quality of the material and density of the micropipes decreases it becomes easier to observe and distinguish the influence of other types of defects on the electrical performance of the devices. The influence of the defects and lateral non-uniformities normally increases with the increasing area of the device. The awareness of the role played by other types of defects and imperfections increases as more and larger size devices are made and is reflected in the rapidly increasing number of papers on reliability related issues [29–36].

Recently, other defects present in SiC material like screw dislocations have also been given extra attention [37, 38]. These defects are suspected to influence dynamic performance of the devices and were shown to be responsible for soft breakdown phenomena in device characteristics. The role of these defects is, however, not clear as yet. Their effect on the device performance is clearly not as detrimental as that of micropipes. The final judgement has to wait since long time stability data under both static (DC) and switching conditions (frequency tests) are still missing. A lot of the fundamental questions related to stability and reliability of SiC devices remain at present unanswered. These issues related to material bulk and surface properties and to surface passivation and gate insulation in MOSFETs will be crucial during the coming years for the success of wide band gap semiconductor materials and high temperature electronics. Issues of passivation and insulation are also starting to attract more and more attention [39, 40]. It is a rapidly expanding field of research. Oxide/nitride/oxide stacks and also oxides subjected to nitridation have been shown to have improved dielectric strength [41, 42] however oxide is still a base of this gate dielectric system determining interface properties. Also monocrystalline AlN was suggested and tried [43, 44] but its deposition or MBE growth requires high temperatures (> 1000°C). Reliability issues are expected to dominate the research field of SiC (and later also of GaN) at the present stage of technology and device development and for many years to come.

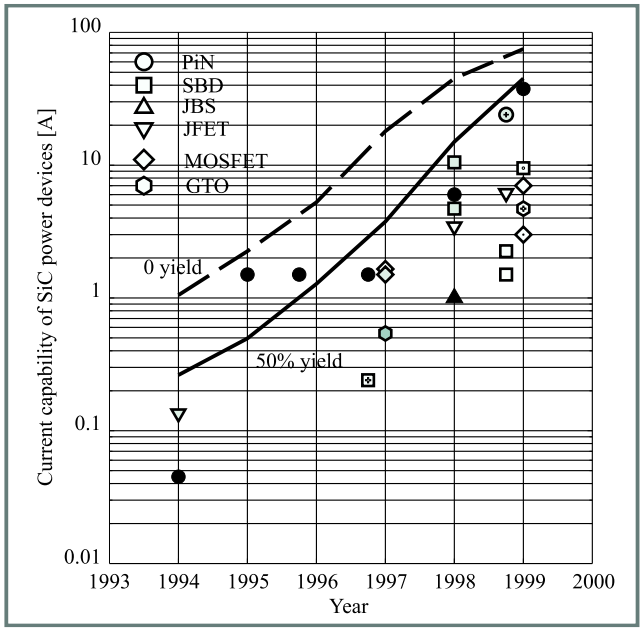

Fig. 8. Evolution of current handling capability in SiC power devices. The best published data from different manufacturers are summarised in the figure according to publication date.

In Fig. 8 most of the published results from different device types are summarised in terms of current handling capability assuming a current density of 150 A/cm^2 for all the devices. The line of 50% yield and 0% yield is based on the data from HV PiN diode development using a Poisson yield distribution fit to experimental data over the years. All other data are from other manufacturers. Data show a dramatic (exponential) progress in current handling capability taking place in the most recent couple of years. This means that we can expect current handling capability to reach levels adequate for most practical applications in a few years.

4.3. Status of SiC power devices

A summary of the status of development of SiC power devices is given below by listing devices in the order of decreasing maturity and specifying optimal voltage range for each device.

1. Schottky barrier rectifiers (SBDs), voltage range 0.2 to 2.5 kV, higher leakage current compared to PiN and JBS at higher temperatures. SBDs with blocking voltages up to 4.9 kV have been demonstrated.

2. PiN rectifiers, voltage range above 4.5 kV, high on-state voltage due to WBG, voltages in excess of 10 kV require significant improvement of carrier lifetime. PiN rectifiers with blocking voltages up to 8.6 kV have been demonstrated.

3. JBS diodes, voltage range 0.2 to 10 kV, a device of choice for working temperatures above 150°C, due to lower leakage current compared to SBDs. JBS rectifiers with blocking voltages up to 3.9 kV have been demonstrated.

4. Vertical JFETs, voltage range 0.2 to 10 kV, normally-on devices, can be used in cascode configurations with low voltage Si MOSFET to obtain insulated gate control and normally-off function. Vertical JFETs with blocking voltages up to 1.8 kV have been demonstrated.

5. GTO thyristors, voltage range 8 to 40 kV, robust devices for high temperature, high radiation environments, can be operated in cascade configuration with low voltage Si/SiC MOSFET for insulated gate control. GTOs with blocking voltages up to 2.6 kV have been demonstrated.

6. MOSFETs, voltage range 0.2 to 8 kV. SiC MOSFETs suffer from low channel mobility values. However even though this lowers their performance compared to the ideal material limit they are already today superior in performance compared to Si devices for voltages over 0.5 kV. MOSFETs with blocking voltages up to 2.6 kV have been demonstrated. The trend of continuous improvements in channel mobility and device performance by technology development and by novel designs is continuing.

5. Power devices. Choices and prospects

5.1. Unipolar versus bipolar Si and SiC devices

Introduction of SiC power devices will change with time the scene of preferred semiconductor devices used in different applications. It is important for the system designer and semiconductor device engineer alike to be able to understand the potential and limitations of different devices as well predict the pace of their development. In Fig. 9 the ideal performance limits of unipolar and bipolar Si and SiC power devices are shown in the domain of on-state voltage and blocking voltage. In the Si case the on-state voltage curves based on the actual device data are shown for fast PiN rectifiers, MOSFETs, IGBTs and GTO thyristors together with an ideal limit equal to the resistivity of the uniformly doped drift region of unipolar device only. In the SiC case the on-state voltage curves based on device simulations are shown for DMOS and UMOS transistors, vertical JFETs, Schottky barrier rectifiers, PiN rectifiers and IGBTs. The SiC device data represent the ideal limit for different types of devices. The device lateral design uses high-density layout with small cell pitch equal to 3 μm, 5 μm and 10 μm for UMOSFET, VJFET and DMOSFET, respectively. The ideal bulk mobility is assumed for all the devices in both the channel and the drift region. The contribution from substrate resistance is included and minimised assuming only 100 μm thick substrate with a doping of $1 \cdot 10^{19}$ cm^{-3}. The ideal limit for 4H-SiC based on the resistivity of the uniformly doped unipolar device drift region only is shown including the influence of the substrate

Table 2
Challenges in development of SiC PiN rectifiers

		Primary	Secondary	Driver
Improvement	Continuous	Increase current handling capability	Reduce on-state voltage Reduce contact resistance Reduce substrate resistivity	Power distribution HV applications
	Breakthrough	Improve stability Improve performance at high current densities Adequate passivation High carrier lifetime material $(2 \div 10\,\mu s)$	Substrate thinning	Low V_{on} Reliability

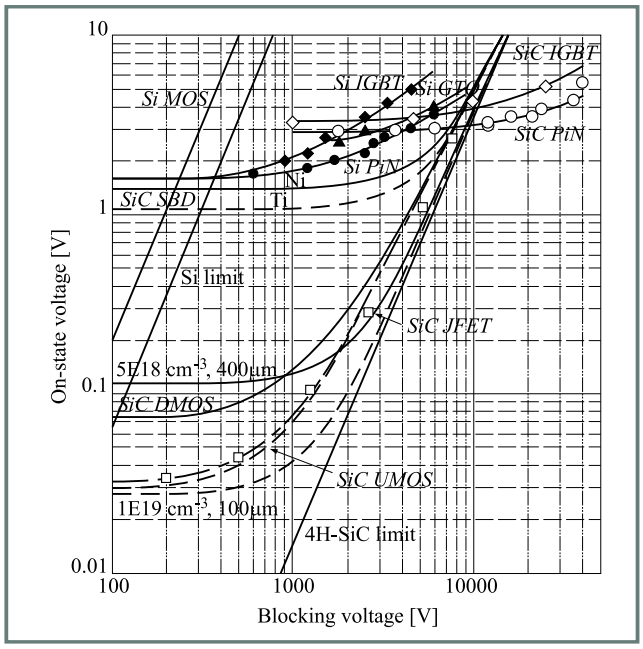

Fig. 9. On-state voltage of Si (actual) and SiC (simulated) power devices as a function of blocking voltage.

resistance in the case of thick and low doped and thin and higher doped substrate. The 400 μm thick substrate with a doping of $5 \cdot 10^{18}$ cm^{-3} represents substrates available today and the 100 μm thick substrate with a doping of $1 \cdot 10^{19}$ cm^{-3} illustrates the improvement possible by using thinner and higher doped substrates. In the case of very high voltage SiC bipolar devices the single most important parameter is free carrier lifetime. The curves for SiC PiN rectifiers and SiC IGBTs shown in the diagram are based on simulations using carrier lifetime of 5 μs in the range from 1 kV to 40 kV. A carrier lifetime of 2 μs results in on-state values not much worse than shown up to the blocking voltage of about 6 kV and 15 kV for IGBTs and PiN rectifiers, respectively. On the other hand, IGBT and PiN devices with blocking voltage in excess of 25 kV and 30 kV, respectively, require a lifetime of 10 μs in order not to deviate more than 0.5 V from the drawn curves.

Several important conclusions can be drawn from the data presented in Fig. 9. First of all the application area of unipolar devices is greatly expanded. The SiC unipolar devices are superior to silicon power devices with respect to the on-state voltage in the voltage range up to at least 10 kV. Considering superiority of unipolar devices over bipolar in terms of dynamic behaviour and switching losses it means that SiC unipolar devices have the potential of replacing silicon bipolar devices in all their present applications (assuming the same current and voltage ratings). Secondly, the application area of SiC bipolar devices starts above blocking voltage of 8–10 kV which is above the Si power devices with highest ratings available today. The SiC bipolar devices are superior to the Si bipolar devices with respect to the switching losses due to the low plasma level and low accumulated charge in the device during conduction. This is caused by 10 times smaller thickness of the n-base and to the lower minimum lifetime required for efficient conductivity modulation. It can also be seen that above 4.5 kV SiC PiN rectifiers are superior to Si PiN rectifiers also with respect to the on-state voltage. The same applies to the SiC IGBTs with voltage rating above 2.5 kV as compared to the Si IGBTs. In the case of Schottky barrier devices there is hardly any gain other than the cost of the epitaxy to differentiate between different voltage designs for voltages lower than about 1 kV. Finally it can also be seen that in order to use fully potential of SiC unipolar devices also at the low voltage end it is necessary to lower the resistance contribution of the substrate material. With standard substrate material available today the practical lower limit of the design voltage is around 1 kV. Thinning of the SiC substrate would expand that limit down to about 200 V. The idealised evolution in time between different power devices and materials with respect to the voltage range is pictured in Fig. 10; assuming constant continued improvement in material quality and disregarding cost.

Table 2 summarises challenges in the area of SiC PiN rectifiers.

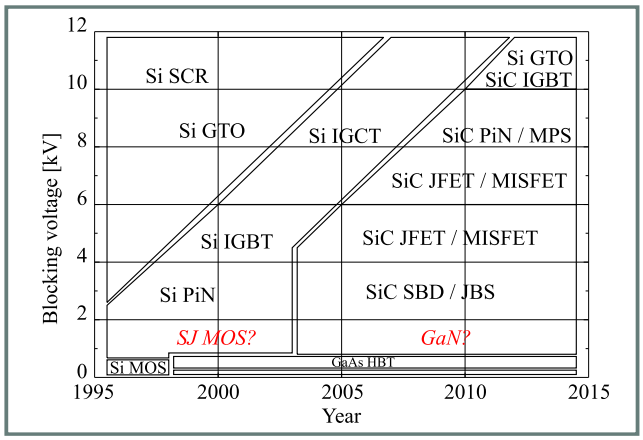

Fig. 10. Preferred device type and semiconductor material based on the data in Fig. 9.

5.2. Unipolar devices

In Fig. 11 a summary of the best published specific on-resistance values from different unipolar devices is given to substantiate what was said before. Also shown in the diagram is the theoretical material limit for on-resistance in Si and SiC. The newest development in the field of MOSFET on-resistance so called Cool MOS (Siemens) is shown. The principle for the breakthrough in reducing on-resistance in MOSFETs is called Super Junction design. It means that the drift region is divided into alternating narrow layers of n- and p-type parallel to the current flow. The doping of the n- and p-type layers must be controlled in such a way that the n- and p-type regions are depleted under blocking condition and that the charge in n- and p-type layers due to doping is equal. The donator and acceptor charges neutralise each other. In this way the doping of the n-type layers constituting new channels for current during conduction can be increased without influencing negatively the blocking voltage. The higher is n-type doping the larger is the reduction of the on resistance. However that means that n-type regions must be made smaller and smaller in order to be depleted under blocking conditions. If not the increase in electric field will cause the premature breakdown. The SJ principle removes the limitation of having to lower drift region doping with increase in blocking voltage and the resulting quadratic dependence of the on-resistance on the design voltage. The impact of SJ design with different width of super junction regions on both Si and SiC MOSFET performance is shown by the stretched lines (simulated). The technology for realisation of the depicted benefits is not easy or cheap. Today's Cool MOS technology is rather coarse and could be depicted as 10–20 μm [45–47]. The point is that similar concept can be realised in the case of SiC devices. Another point is that SiC MOSFETs with today's poor channel mobility values are already superior to the best silicon devices.

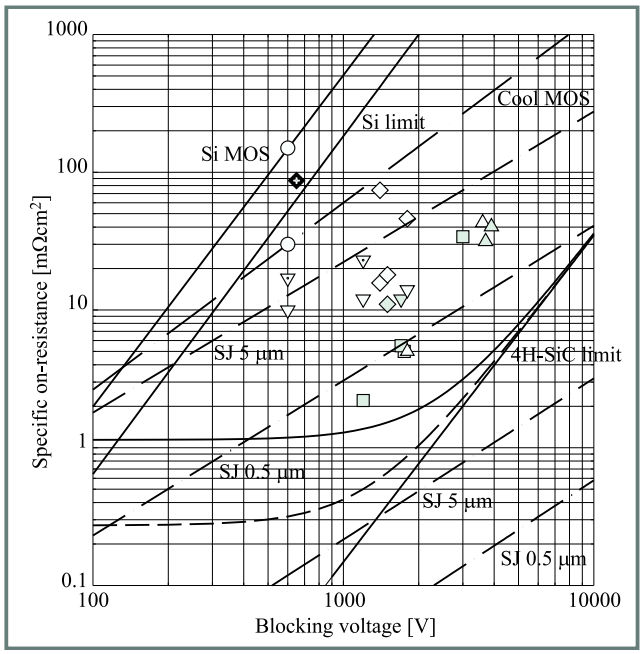

Fig. 11. Specific on-resistance of unipolar Si and SiC devices. The meaning of symbols is like in Fig. 8. The diamond with cross is a lateral MOSFET. The lines for SJ devices are shown for 5 μm and 0.5 μm wide regions (10 μm and 1 μm pitch, respectively).

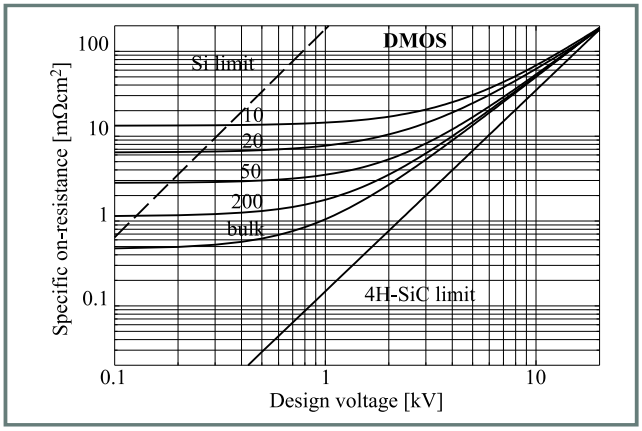

Fig. 12. Influence of the channel mobility on specific on-resistance of 4H-SiC DMOSFETs.

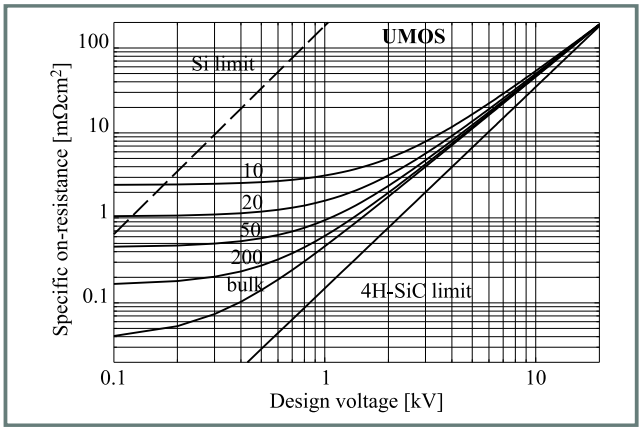

Fig. 13. Influence of the channel mobility on specific on-resistance of 4H-SiC UMOSFETs.

In Figs. 12 and 13 the influence of the channel resistance on the specific resistance of the 4H-SiC DMOSFETs and UMOSFETs is shown, respectively, in the voltage range from 100 V to 20 kV. The simulated structures are those used in Fig. 9 with cell pitch of 10 μm and 3 μm for DMOSFET and UMOSFET, respectively. The channel length is about 1 μm. The voltage design of structures is adjusted by varying resistivity and thickness of the drift region except for the structures for voltages lower than 1 kV. In those structures also the doping in the p-base was reduced improving the channel resistance for the structures with bulk channel mobility. The value of the channel mobility in the case of the DMOSFET is the average mobility due to the gaussian p-well doping distribution used in the simulations. It can be seen from simulations that channel mobility of $100 \div 200$ cm^2/Vsec can be regarded as target channel mobility for acceptable devices provided it is not coupled to interface conditions giving rise to operational instabilities in threshold voltage and sub-threshold characteristics.

The SiC/SiO_2 interface properties on 4H SiC material are much poorer compared to 6H SiC polytype [48, 49]. These is a reason for much better channel mobility values reported for MOSFETs made on 6H-SiC compared to 4H-SiC. The 6H-SiC material may then be a better choice for reasonably low voltage MOSFETs compared to the 4H-SiC alternative regardless of much poorer bulk mobility value of 6H-SiC influencing the contribution of the drift region. The results of simulations performed on 4H-SiC and 6H-SiC DMOSFET and UMOSFET structures in order to define the voltage limit for such an approach are summarised in Figs. 14 and 15. The simulated structures are the same as those used to obtain data in Figs. 12 and 13. As can be seen from the presented data, it may be advantageous to use the 6H-SiC material for devices below about 0.6 kV. At design voltage of 1 kV, however, the specific resistance of 6H-SiC devices becomes higher than the specific resistance of 4H-SiC devices regardless of the value of channel mobility. This is due to the fact that drift region contribution to the specific resistance is dominating for devices with design voltages larger than about 600 V [50].

Challenges in development of SiC MOSFETs are summarised in Table 3 and challenges related to development of SiC Schottky rectifiers (SBD, JBS and MPS (merged Schottky and PiN rectifiers)) are summarised in Table 4.

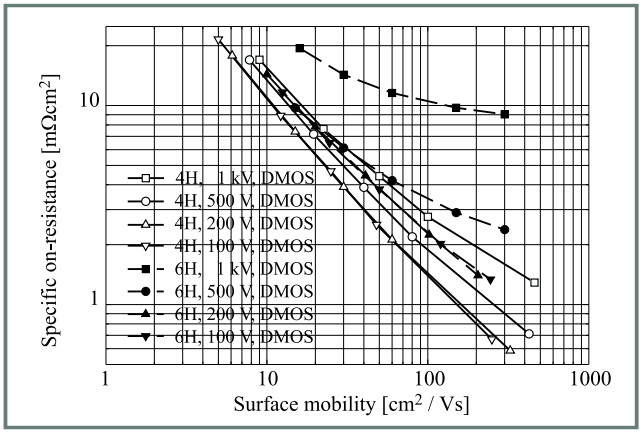

Fig. 14. Specific on-resistance of 4H-SiC and 6H-SiC DMOSFETs as a function of the channel mobility.

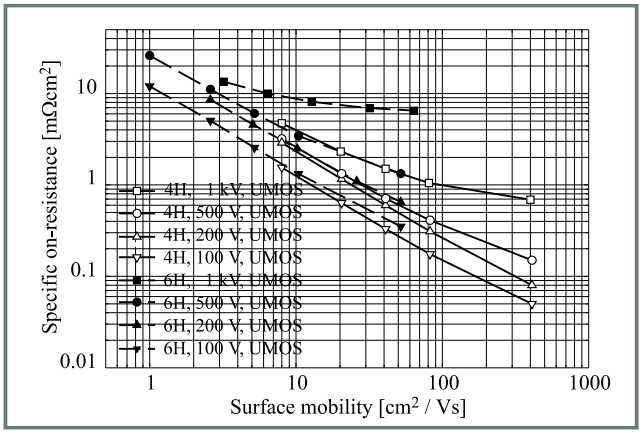

Fig. 15. Specific on-resistance of 4H-SiC and 6H-SiC UMOSFETs as a function of the channel mobility.

6. Silicon carbide electronics

6.1. Device perspective

Challenges in SiC electronics from the device perspective are summarised in Table 5.

6.2. Total system perspective

The appearance of the SiC power devices on the market will bring about and accelerate new developments in the areas of packaging, passive components (capacitors), circuit and system design as well as improvements in construction and operation of electric motors. It will not be in general most effective just to substitute SiC devices for silicon ones in existing circuits. It will be necessary to adopt new solutions in order to utilize full potential of increased operational frequency, working temperature and reduced size of active devices. Advent of SiC power devices will enforce thinking in terms of the total power system including electrical, mechanical and electromechanical components. This will provide incentive towards increased integration of electronics and electromagnetic and mechanical parts of the system. Also electrical motors will have to be developed in order to facilitate integration and utilisation of the benefits of high frequency operation.

The necessity of new solutions is most apparent and urgent in the area of packaging. Especially considering that the modular solution utilising parallel connection of small chips as opposed to large area single devices will be the most efficient way to increase current handling capability for a long time. This actualises necessity of high temperature, high frequency and high packing density module technology. Challenges in packaging are summarised in Table 6.

Table 3
Challenges in development of SiC MOSFETs

		Primary	Secondary	Driver
Improvement	Continuous	Improve channel mobility Improve interface quality Increase current handling capability	Reduce contact resistance Reduce resistivity of implanted layers Reduce substrate resistivity	Low R_{on} Feasibility
	Breakthrough	New gate dielectrics Channel engineering – crystallographic orientation (ex. a-plane) – polytype (ex. 15R) – buried channel etc. (depletion type)	Substrate thinning	Low R_{on} Reliability

Table 4
Challenges in development of SiC Schottky (SBD, JBS and MPS) rectifiers

		Primary	Secondary	Driver
Improvement	Continuous	Low leakage junction termination Increase current handling capability	Reduce on-state voltage Reduce contact resistance Reduce substrate resistivity	Low R_{on} Low leakage currents
	Breakthrough	High barrier materials for $T > 150^{\circ}$ C Adequate passivation	Substrate thinning	Reliability

Table 5
Challenges in SiC electronics

		Primary	Secondary	Driver
Improvement	Continuous	Wafer quality and size MISFET technology – improve channel mobility – improve interface quality Niche application Increase current handling capability	Contact resistance Resistivity of implanted layers Substrate resistivity	Material supply
	Breakthrough	New gate dielectrics Adequate passivation Novel structures Implantation damage Packaging for HT New material suppliers	Carrier lifetime	Speed Losses High T_j System benefits

Table 6
Challenges in packaging for SiC devices

		Primary	Secondary	Driver
Improvement	Continuous	Lower R & L	High reliability die attach High reliability bonding Low stress compounds	Surface mount Automotive
	Breakthrough	Reduce pkg/chip footprint Better voltage isolation Better CTE matching Diamond heat spreaders Flip-chip mounting EMI immunity	High T_g plastics	Surface mount Reliability

7. Conclusions

Commercialisation of SiC power devices is facing a lot of extremely difficult challenges. Especially, reliability issues constitute the biggest challenge in the coming years.
It is however, difficult to see anything that could prevent SiC power devices from entering the electronic market in the first decade of this century considering:

a) the tremendous benefits offered to the electronic systems,

b) the momentum gained by the development activities involving many people in different countries,

c) the spectacular results in device performance obtained so far,

d) the dramatic increase in the ratings of test devices during the recent years.

This last point is a reassuring indication of the continued positive development.

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