Invited paper

Direct extraction techniques of microwave small-signal model and technological parameters for sub-quarter micron SOI MOSFETs

Michël Goffioul, Danielle Vanhoenacker, and Jean-Pierre Raskin

Abstract — Original extraction techniques of microwave small-signal model and technological parameters for SOI MOSFETs are presented. The characterization method combines careful design of probing and calibration structures, rigorous in situ calibration and a powerful direct extraction method. The proposed characterization procedure is directly based on the physical meaning of each small-signal model element. Knowing the qualitative small-signal behavior of each model parameter versus bias conditions, the high frequency equivalent circuit can be simplified for extraction purposes. Biasing MOSFETs under depletion, strong inversion and saturation conditions, certain technological parameters and microwave small-signal elements can be extracted directly from the measured S-parameters. These new extraction techniques allow us to understand deeply the behavior of the sub-quarter micron SOI MOSFETs in microwave domain and to control their fabrication process.

Keywords — microelectronics, microwave devices, SOI MOSFET.

1. Introduction

The boom of mobile communications leads an increasing request of low cost and low power mixed mode integrated circuits. Maturity of silicon-based technology and recent progresses of MOSFET's microwave performances [1–4], explain silicon success as compared to III-V technologies. Silicon-on-insulator-based MOSFETs are very promising devices for multigigahertz applications. Thin-film SOI MOSFETs offer indeed interesting low-voltage performances, higher speed and increased integration density, all with simpler processing than bulk silicon MOSFETs of comparable size [5]. Many recent realizations of logic circuits, memories, and RF circuits [6] have confirmed both the advantages and the viability of thin-film SOI circuits, even in the case of very large systems. To support the development of thin-film SOI circuits, adequate device models and characterization techniques must be available concurrently with the maturation of fabrication processes. In the present paper, we describe direct extraction techniques to accurately characterize sub-quarter micron SOI MOSFETs in the microwave domain. The characterization method combines careful design of probing and calibration structures, rigorous in situ calibration and a powerful direct extraction method. The proposed characterization procedure is directly based on the physical meaning of each small-signal model element. That makes it very useful for controlling the sensitive fabrication steps such as the silicidation process of the gate, source and drain regions. Moreover, due to the physical meaning attributed to each model element through the characterization process, the extracted equivalent circuit is scalable. This last point is crucial for circuits simulation and optimization purposes.

2. Fabrication process

200 nm UNIBOND® wafers with a 400 nm buried oxide were used as the starting material. The silicon thickness was thinned down to 40 nm or 30 nm by a recessed-channel process in the case of the fully depleted (FD) transistors. Gate oxide (4.5 nm) was grown after a LOCOS isolation. A field implant is used to eliminate sidewall leakage. A 200 nm thick polysilicon layer is deposited and patterned by DUV lithography. Source/drain extension implant is followed by formation of a 80 nm spacer oxide after which the source-drain regions are implanted and activated with a 950°C/15 s RTA afterwards. A titanium silicide process is used to reduce the sheet and contact resistances of gate fingers and the elevated 80 nm thick source-drain regions. After the silicide process a gate sheet resistance of about 10 $\Omega/\square$, instead of 100 $\Omega/\square$ for a classical doped polysilicon gate, is obtained for a 0.25 μm gate channel length MOSFET. The total S/D series resistance were about 700 $\Omega\mu$m and 1300 $\Omega\mu$m for n- and p-MOSFETs, respectively. The back-end processing includes a three level metal process with tungsten plugs and planarization of intermetal oxides by chemical and mechanical polishing (CMP). SOI MOSFETs composed of 12 gate fingers connected in parallel with various channel lengths (L = 0.25, 0.35, 0.5 and 1 μm) and widths (W = 1, 2, 3.4, 6.6, 9, 15 and 25 μm) were built and measured.

3. Microwave small-signal model

The direct extraction methods developed in the present paper are based on the good knowledge of the measured transistors 3D structure and the physical meaning attributed

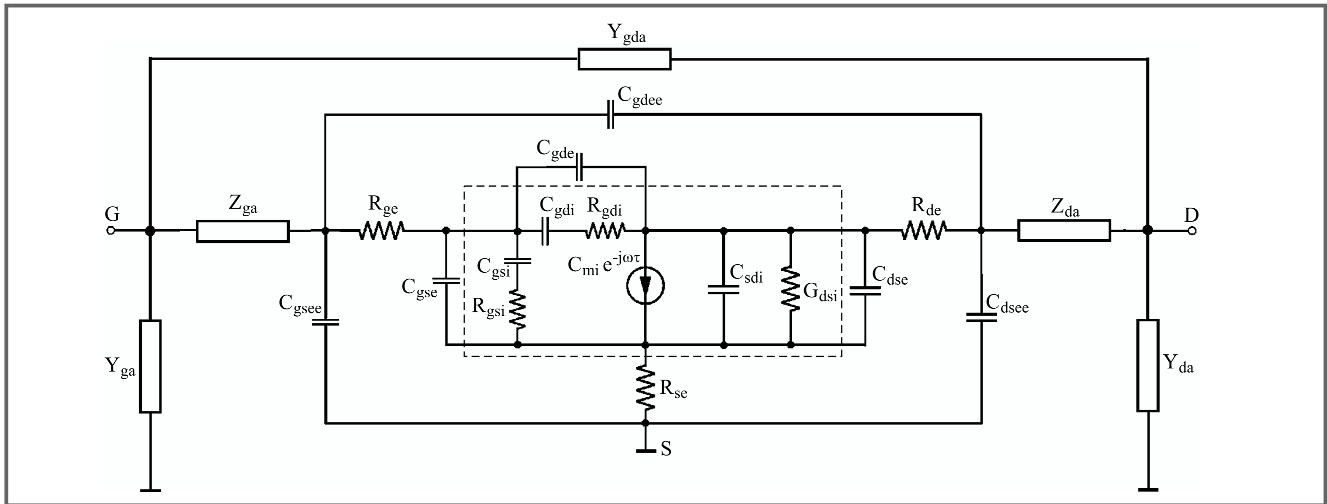

Fig. 1. Small-signal model of a common-source SOI MOSFET.

to the various lumped elements of transistors small-signal equivalent circuit. Figure 1 shows the model used for the common-source SOI MOSFET. According to the physical meaning attributed to the elements, the circuit can be split into three parts:

- Index i denotes the intrinsic elements which model the core of the transistor, and are thus dependent on the bias conditions and on the size of the active zone.
- Index e denotes the extrinsic elements, which are supposed to be independent of bias, but scale with the active zone.
- Index a denotes the shunt and series access parameters caused by the metal connections just outside of (adjacent to) the active zone. The frequency behavior of the series impedances (Z_{ga} and Z_{da}) and shunt admittances (Y_{ga} and Y_{da}) is determined by the propagation characteristics of a coplanar waveguide transmission line (CPW) on SOI substrate. They are constant under normal biasing conditions, and not dependent on the width of the active zone.

Under certain bias conditions, some small-signal elements vanish and then the equivalent circuit presented in Fig. 1 can be simplified. These assumptions can only be done if the physical meaning of each small-signal lumped element of the transistor structure is correctly considered. In the next section, the extraction procedure of technological parameters and microwave small-signal elements based on transistor S-parameters measured under depletion, strong inversion and saturation conditions is explained.

4. Extraction procedure

The main steps of the small-signal model extraction are: the extraction of the CPW feed transmission lines parameters, the determination of the extrinsic parasitic capacitances, the extraction of the extrinsic resistances, and finally, the determination of all intrinsic elements for a given bias point. Following the same philosophy, it has been shown that certain technological parameters such as the effective channel length, the gate, source and drain silicide resistivities and the effective gate oxide thickness can be directly extracted from the measured high frequency S-parameters.

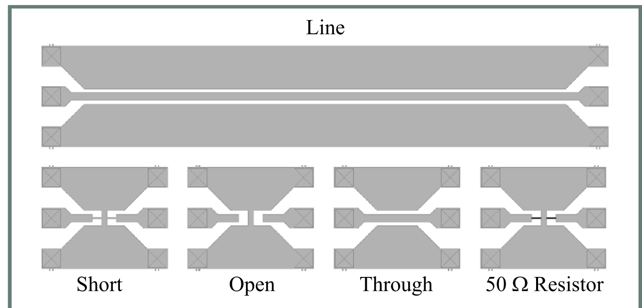

Fig. 2. Calibration kit allowing to perform a TRL calibration and to determine the reference impedance.

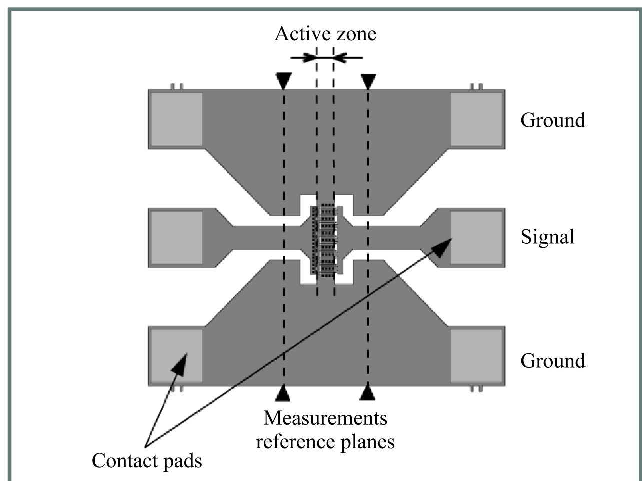

Fig. 3. Top view of on-wafer MOSFET test structure showing the measurements reference planes and the active zone.

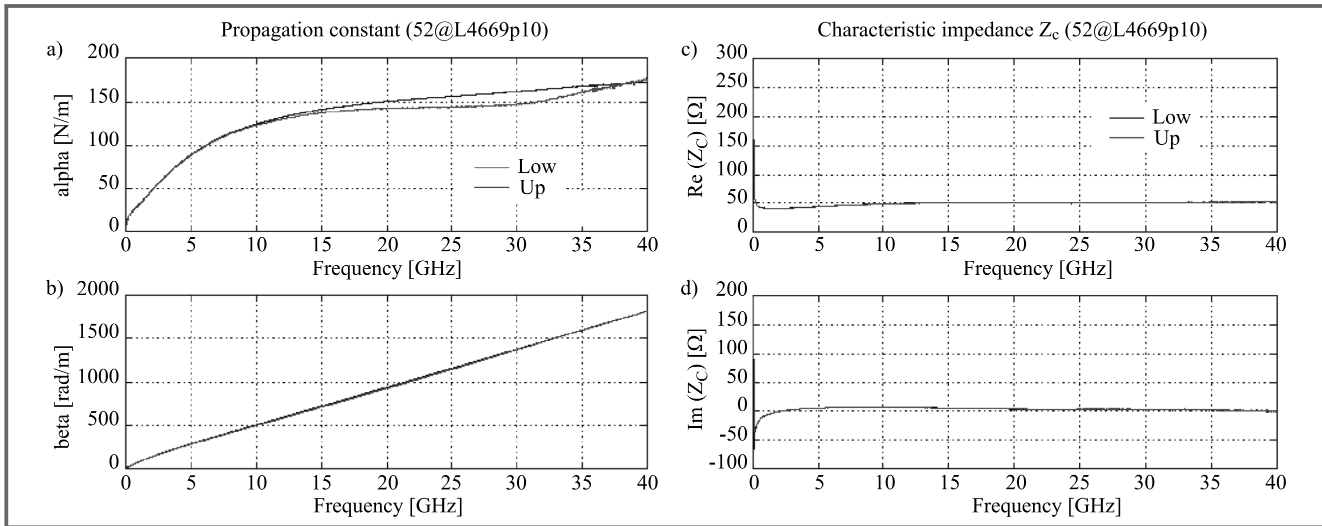

Fig. 4. Extracted complex propagation coefficient ($\gamma = \alpha + j\beta$) (a), (b) and complex characteristic impedance (Z_c) (c), (d) by considering the measured S-parameters of the short line (Up, called „through" in Fig. 2) and the long line (Low, called „line" in Fig. 2) in the calibration procedure.

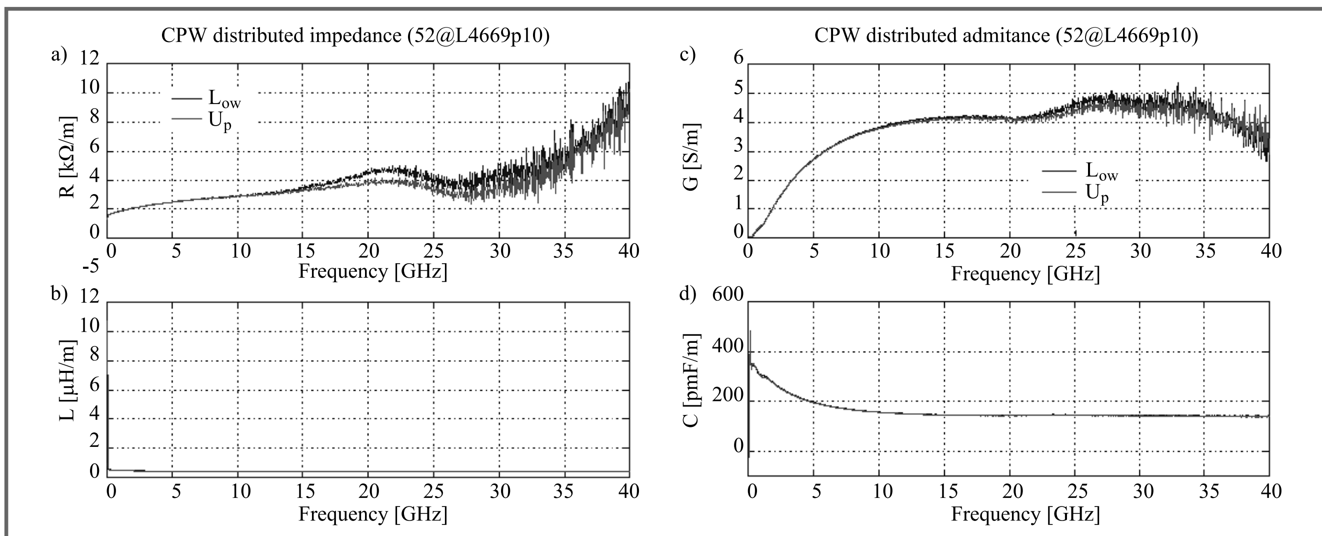

Fig. 5. Extracted series (*R* and *L*) (a), (b) and shunt (*G* and *C*) (c), (d) equivalent parameters per unit length for a CPW line on standard SOI substrate (20 Ωcm).

4.1. Extraction of the CPW feed lines parameters

Using standards implemented on the SOI wafer (Fig. 2), a through-reflect-line (TRL) calibration is performed as described in [7] for defining the S-parameters reference planes close to the input and output of measured transistors. Figure 3 shows the position of the measurements reference planes after calibration. It appears that there is a short residual length of CPW metallic line (approximately 50 μm) at the transistor input and output between the measurements reference planes and the beginning of the transistor active zone. After the extraction of the transmission line characteristics Z_c and γ (Fig. 4) from the measured calibration kit (Fig. 2) built on SOI substrate, the series and shunt parameters per unit length of the line are obtained. Figure 5 presents the extracted impedance and admittance values per unit length for a CPW line implemented on standard SOI substrate (20 Ωcm). Knowing the exact distance between the measurements reference planes and the beginning of the transistor active zone (l_{ga} and l_{da}, the CPW line access lengths at the input and output of the transistor, respectively) the residual access lines can be then estimated by:
Series impedances:

$$Z_{ga} = l_{ga}(R + j\omega L)\,, \tag{1}$$

$$Z_{da} = l_{da}(R + j\omega L)\,. \tag{2}$$

Shunt admittances:

$$Y_{ga} = l_{ga}(G + j\omega C)\,, \tag{3}$$

$$Y_{da} = l_{da}(G + j\omega C)\,. \tag{4}$$

The parasitic admittance Y_{gda} represents mainly the parasitic coupling between gate and drain metallic interconnec-

tions outside the active zone. As explained in [8], Y_{gda} can be extracted from the measured S-parameters for the transistor biased in depletion. It is obtained by the intercept at the origin of the linear regression on measured data points plotted in a two dimensional plane defined by $[W,Y_{12}]$ or $[W,Y_{21}]$, with W being the transistor total width and Y_{ij} the Y-matrix elements of the transistor measured under depletion bias condition $(V_{gs} << V_{th})$ and V_{ds} = 0 V. It is important to note that due to the design of the metallic access CPW lines (high frequency interconnections) this parasitic element is mainly capacitive and has a very small value (around 1 fF).
Using the extracted values $(Z_{ga}, Z_{da}, Y_{ga}, Y_{da}$ and $Y_{gda})$ the residual series and shunt parasitic access elements are withdrawn by simple matrix manipulations.

4.2. Extraction of the extrinsic capacitances

Figure 6 shows the cross-section of a fully depleted SOI MOSFET with its metallic drain and source interconnections. The physical origins of the parasitic extrinsic capacitances indicated in Fig. 1 are multiple.

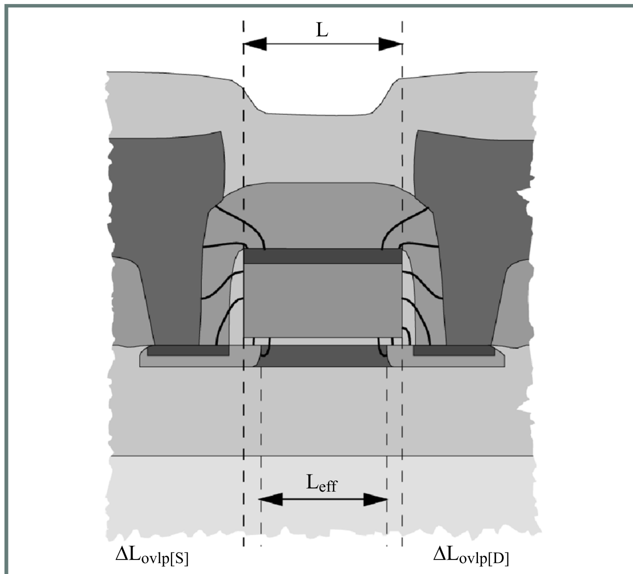

Fig. 6. Cross-section of a fully depleted SOI MOSFET with its metallic drain and source interconnections.

We have the overlap gate-to-drain and gate-to-source capacitances $(C_{gse} = \varepsilon_{ox}\Delta L_{ovlp[S]}/d_{ox}, C_{gde} = \varepsilon_{ox}\Delta L_{ovlp[D]}/d_{ox})$. We can limit these parasitic capacitances by controlling the thermal diffusion of doping atoms from the source and drain regions into the transistor channel. The extrinsic capacitance C_{dse} corresponds to the proximity parasitic capacitance between drain and source diffusion regions. That parasitic capacitance can be quite important for sub-quarter micron MOSFETs.
C_{gsee}, C_{gdee} and C_{dsee} are the extrinsic capacitances due to parasitic couplings between metallic interconnection lines outside the transistor active zone between gate-source, gate-drain and drain-source, respectively. The values of these capacitances are independent with bias conditions and depend on the transistor size and also on the design of the transistor metallic interconnection structure. In order to extract the extrinsic capacitances the transistor S-parameters are measured in deep depletion $(V_{gs} << V_{th})$ and V_{ds} = = 0 V. Under these bias conditions, the equivalent circuit of the MOSFET is simplified, as shown in Fig. 7. As

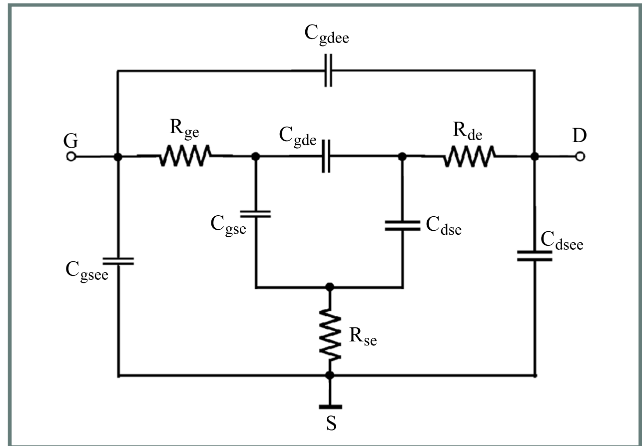

Fig. 7. Simplified small-signal equivalent circuit for a common source SOI MOSFET in deep depletion $(V_{gs} << V_{th})$ and V_{ds} = 0 V.

explained in [9], at relatively low frequencies the effects of the extrinsic resistances can be neglected and therefore, the extrinsic capacitances are directly obtained from the imaginary part of the measured Y-parameters. However, due to the dimension shrinkage of the recent transistors (channel length < 0.25 μm), the parasitic capacitances between transistor fingers and metallic connection vias along the active region of the transistor structure become non-negligible. Because all of those parasitic extrinsic capacitances are connected in parallel with the extrinsic overlap and drain-

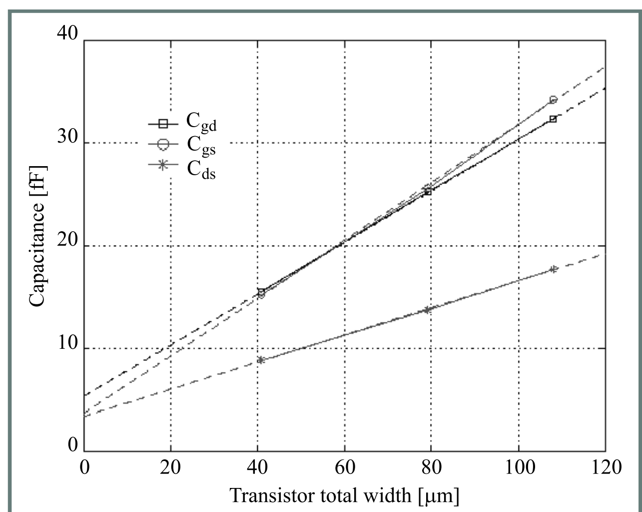

Fig. 8. Evolution of the total extrinsic capacitances measured in deep depletion at V_{ds} = 0 V for various total active zone widths (W).

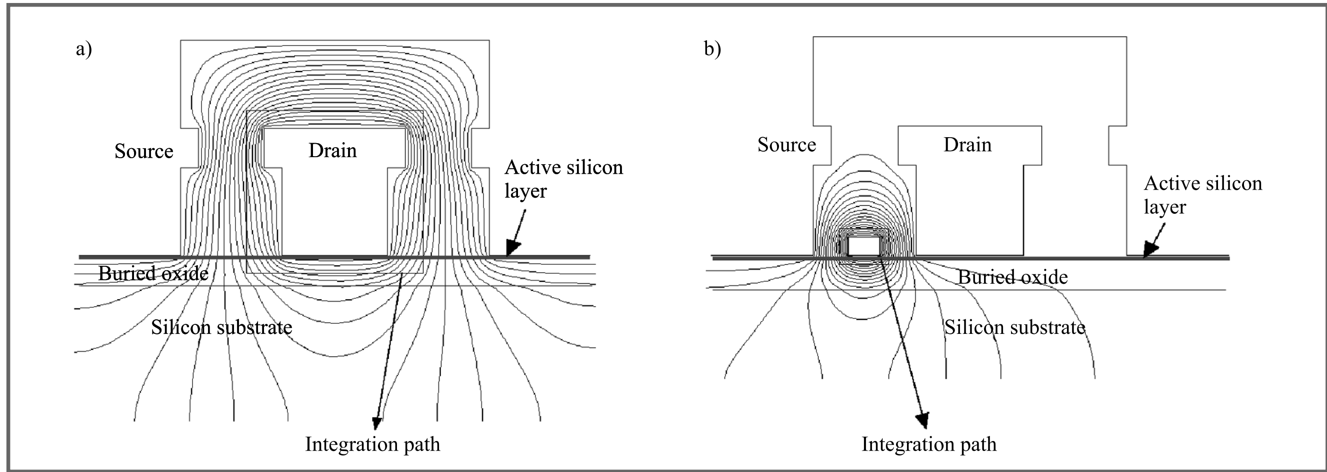

Fig. 9. 2D electrostatic simulations for the estimation of the parasitic source-to-drain (C_{dsee}) (a), gate-to-drain (C_{gdee}) and gate-to-source (C_{gsee}) (b) coupling capacitances.

-to-source proximity capacitances $((C_{gse}, C_{gsee}), (C_{gde}, C_{gdee})$ and $(C_{dse}, C_{dsee}))$ as shown in Figs. 1 and 7, their extraction is not straightforward.

Figure 8 represents the evolution of the total capacitances ($C_{gs} = C_{gse} + C_{gsee}, C_{gd} = C_{gde} + C_{gdee}$ and $C_{ds} = C_{dse} + C_{dsee}$) measured in deep depletion at V_{ds} = 0 V for various total active zone widths (W).

In order to dissociate the different extrinsic capacitances, we have used a 2D electrostatic simulator for estimating the parasitic coupling effects existing between the gate, drain and source metallization levels (C_{gsee}, C_{gdee} and C_{dsee}). Figure 9 shows the equipotential lines calculated by the 2D electrostatic simulation software for two different boundary conditions. The capacitances are obtained by integrating the electric field along the integration path as indicated in the schemes. From the calculated capacitance values C_{gsee}, C_{gdee} and C_{dsee} and the measured imaginary part of Y-parameters (C_{gs}, C_{gd} and C_{ds}) for the transistor biased in deep depletion (Fig. 8), the extrinsic capacitances $C_{gde} (= C_{gd} - C_{gdee}), C_{gse} (= C_{gs} - C_{gsee})$, respectively, the gate-to-drain and gate-to-source overlap capacitances, and $C_{dse} (= C_{ds} - C_{dsee})$, the source-to-drain proximity capacitance, are extracted.

4.3. Extraction of the extrinsic resistances

After removing the parallel extrinsic capacitances (C_{gsee}, C_{gdee} and C_{dsee}) by simple matrix manipulations, we consider the parametric curves defined in a two dimensional plane $[x_1, x_2]$ by $[\mathrm{Re}(Z_{\sigma\pi ij}(\omega)), \mathrm{Re}(Z_{\sigma\pi kl}(\omega))]$, where $\{i, j\} \neq \{k, l\}$, for the transistor biased in saturation ($V_{ds} > V_{gs} - V_{th}$). It has been demonstrated that these curves are straight lines and from their slope and intercept at the origin the extrinsic resistances (R_{ge}, R_{de} and R_{se}) are directly extracted [9]. Figures 10 and 11 represent the parametric plot of resistances in the 0.5÷40 GHz band at $V_{gs} = 1$ V and $V_{ds} = 2$ V for 12 x (6.6/0.35) μm^2 and 10 x (24/0.75) μm^2 SOI n-MOSFETs, respectively. The

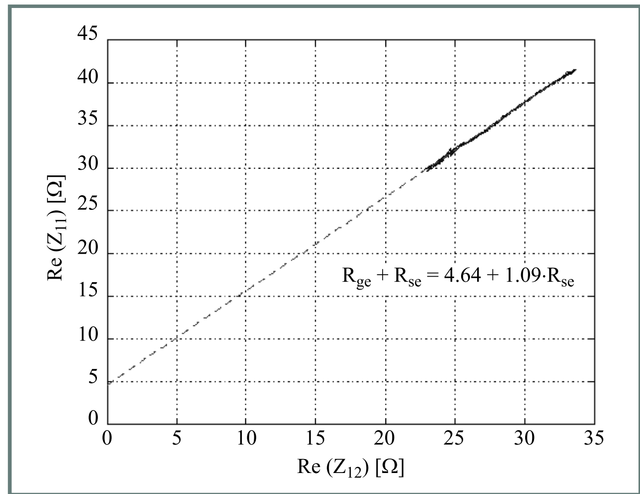

Fig. 10. Parametric plot of resistances in the 0.5÷40 GHz band for 12 x (6.6/0.35) μm^2 SOI n-MOSFET at V_{gs} = 1 V and V_{ds} = 2 V.

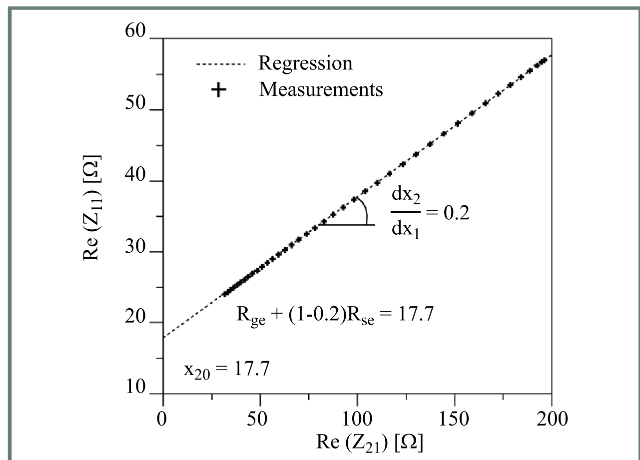

Fig. 11. Parametric plot of resistances in the 0.5÷40 GHz band for 10 x (24/0.75) μm^2 SOI n-MOSFET at V_{gs} = 1 V and V_{ds} = 2 V.

accuracy of the extracted resistance values is related to the precision with which the slope and the intercept at the origin can be determined by linear regression from the measured Z-parameters. By comparison of Figs. 10 and 11, it appears that higher accuracy on the extracted resistance values is reached if the measurements frequency band includes the cut-off frequency of the measured transistor. The current gain cut-off frequency (f_T) for the measured 12 x (6.6/0.35) μm^2 and 10 x (24/0.75) μm^2 SOI n-MOSFETs are 40 and 14 GHz, respectively.

In order to overcome that lack of accuracy on the extrinsic resistances extraction for sub-quarter micron MOSFETs, we have defined one additional linear relationship involving the summation of extrinsic resistances R_{se} and R_{de}. In fact, it can be demonstrated that at low frequencies (from 1 to 5 GHz) and for bias points chosen in linear region ($V_{gs} = > V_{th}$ and $V_{ds} << V_{gs}$) the real part of Z_{22} parameters are given by:

$$\mathrm{Re}(Z_{22}) = R_{de} + R_{se} + f(intrinsic\ elements)\ . \qquad (5)$$

Figure 12 presents the real part of Z_{22} measured in linear region from 1 to 5 GHz versus the layout channel length for 160 μm width SOI n-MOSFETs. A linear function is observed. By definition for a channel length equal to zero all of the intrinsic elements vanish, and therefore, from Eq. (5) and the intercept at the origin obtained from a linear regression on the measured data points (Fig. 12), the value of $R_{se} + R_{de}$ is extracted.

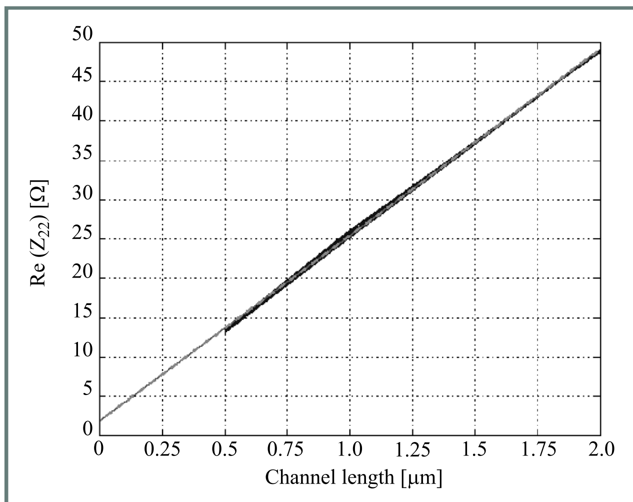

Fig. 12. Evolution of the Z_{22} parameter real part versus the layout channel length.

Table 1 shows all of the extrinsic elements values extracted for 12 x (6.6/0.35) μm^2 by using the characterization procedure explained in this section.

4.4. Determination of all intrinsic parameters

After subtracting the extrinsic resistances and capacitances from the measured S-parameters, all of the intrinsic elements ($C_{gsi}, C_{gdi}, C_{sdi}, R_{gsi}, R_{gdi}, G_{mi}, G_{dsi}$, and τ) for an arbitrary bias condition can be directly extracted by using simple matrix manipulations on the intrinsic Y-matrix [10]. Figure 13 presents the evolution of the different intrinsic elements versus frequency for $V_{gs} = V_{ds} = 0.9$ V. Except for the frequencies below 3 GHz, where the deviations from the horizontal are attributed to the low frequency limit of the TRL calibration, the values of the extracted intrinsic parameters remain fairly constant up to 40 GHz. The flatness of the extracted intrinsic elements curves over a wide frequency band is directly related to the completeness of the model used, the validity of the assumptions considered and the quality of the extraction procedure itself. In fact, all of the lumped elements of the small-signal SOI MOSFET model presented in Fig. 1 are considered by definition frequency independent.

Table 1
Extracted extrinsic capacitances and resistances for a 12 x (6.6/0.35) μm^2 SOI n-MOSFET

C_{gsee}	C_{gdee}	C_{dsee}	C_{gse}	C_{gde}	C_{dse}
[fF]					
5.77	5.77	10.4	16.5	14	6.5
R_{ge}	R_{de}	R_{se}			
[Ω]					
5	13.7	4			

The direct extraction method described above has been successfully applied to both SOI p- and n-MOSFETs of various sizes (W and L) up to 40 GHz.

Figure 14 presents the good agreement between measured and simulated S-parameters magnitudes and phases for a 12 x (6.6/0.35) μm^2 SOI n-MOSFET at $V_{gs} = = V_{ds} =$ 0.9 V.

5. Technological parameters extraction

Based on the same concept, technological parameters can be extracted from the S-parameters measurements. In fact, the transistor effective channel length (L_{eff}) can be obtained from the intercept at the origin of the linear regression on the data points plotted in a two dimensional plane $[x_1, x_2]$ by $[C_{gdi}, L]$, C_{gdi} being obtained by subtracting Y_{12} in depletion from Y_{12} in strong inversion ($V_{gs} >> V_{th}$ and $V_{ds} =$ 0 V). In fact, when the intrinsic gate-to-drain capacitance C_{gdi} equal to zero the residual channel length corresponds to the total overlap length ($\Delta L = \Delta L_{ovlp[S]} + \Delta L_{ovlp[D]}$). The effective channel length is then defined as $L_{eff} = L - \Delta L$.

Figure 15 shows the extracted intrinsic capacitance C_{gdi} for SOI n-MOSFETs composed of 12 gate fingers connected in parallel with a total width of 80 μm and a channel length of 0.25, 0.35, 0.5 and 1 μm.

¿From the extracted value of L_{eff}, the gate oxide thickness (t_{ox}) is obtained by $t_{ox} = \varepsilon_{ox}\ WL_{eff}/2C_{gdi}$.

For the measured transistors described above in this section, the extracted gate oxide thickness is 5.48 nm.

Fig. 13. Evolution of the intrinsic lumped extracted values (i.e. conductance (a), delay (b), capacitance (c), intrinsic non-quasi-static resistance (d)) versus frequency for a 12 x (6.6/0.35) μm^2 SOI n-MOSFET at $V_{gs} = V_{ds} = 0.9$ V.

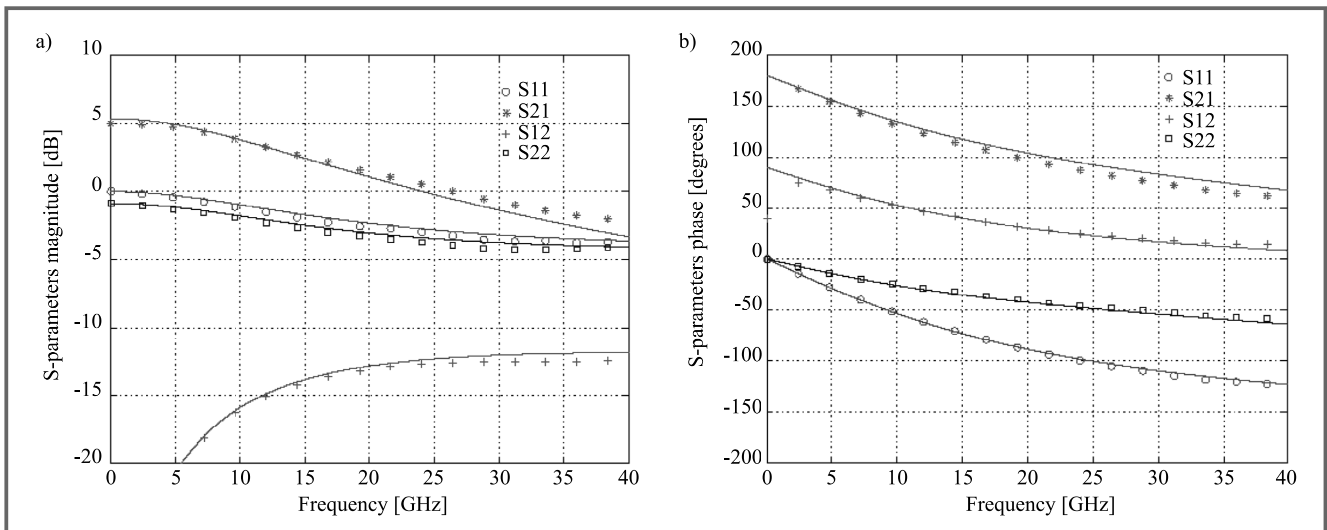

Fig. 14. Measured (lines) and simulated (symbols) S-parameters magnitudes (a) and phases (b) for a 12 x (6.6/0.35) μm^2 SOI n-MOSFET at $V_{gs} = V_{ds} = 0.9$ V.

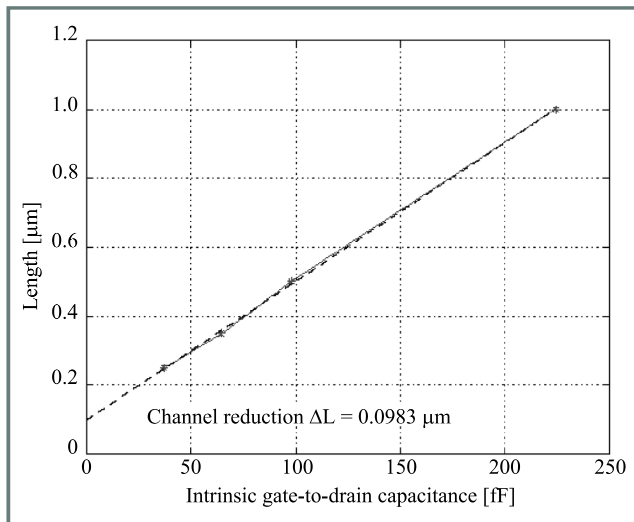

Fig. 15. Parametric curve defined in a two dimensional plane by $[C_{gdi}, L]$.

6. Conclusion

Direct extraction techniques based on measured S-parameters at different bias conditions are presented for determining technological parameters and microwave small-signal model of MOSFETs. This characterization procedure has been used to control and optimize the different steps of the fabrication process. The extracted equivalent circuits have been introduced in commercial simulators for successfully designing microwave SOI CMOS functionalities such as LNA, mixer and oscillators at 1.8 and 5.8 GHz.

Acknowledgements

The authors would like to thank their collaborators at LETI for processing the wafers.

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