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Preface

Rumors about forthcoming twilight of silicon-based microelectronics seem to be exaggerated. Microelectronics has been continuously developing for the past three decades – for instance every three years a new generation of memories becomes available on the market with the capacity four times larger than that of the previous generation. The current „official" development forecast published by SIA (Semiconductor Industry Association) reaches ahead to the years 2012–2015. There are, however, more aggressive forecasts available that reach even as far as the year 2020.

While the development of silicon microelectronics in the past could be attributed mostly to the reduction of the feature size (progress in lithography), today it relies more on new material solutions, such as SOI, SiGe or SiC. The combination of this trend with continuous miniaturization provides the opportunity of moving into the range of very high frequencies.

Silicon microelectronics for fast analog and RF circuits, as well as for mainstream wireless and computational applications – these are the new application areas in telecommunications, which is one of the most powerful drivers of microelectronics product development. It is clear that with the anticipated $f_{max} \approx 50$ GHz and $f_T = 40$ GHz to be reached by RF transistors in 2005, according to the International Technology Roadmap for Semiconductors (SIA, 1999), a lot of effort must be put into the development of appropriate material, processing, characterization and modeling. However, such an outstanding progress will not happen without increased speed offered by new material solutions. As is generally known, carrier mobility in SiGe is several times higher than in silicon due to internal strain. On the other hand, higher speed of operation in SOI devices is achieved mainly due to the reduction of parasitic capacitances.

High-speed is, however, not everything. Portable wireless products push, for obvious reasons, for low-power solutions. This trend, too, requires new material, such as SOI where current drivability is higher than in conventional devices due to reduced thickness of the active region.

In this volume the Reader will find a selection of papers and lectures (part I of two parts) presented during the conference „Advanced Silicon Devices and Technologies for ULSI Era", which took place in Museum of Earth, Warsaw, Poland on 28–30 June 2000. A number of these papers is devoted to high-speed silicon-based microelectronics devices, e.g. Silicon Germanium (SiGe) structures as well as their new application fields, e.g. MicroElectroMechanical Systems (MEMS). There are also papers related to no less exciting and prospective domains of microelectronics (e.g. high-power and high-temperature electronics, etc.), the development of which is currently being tightly associated with the progress in SOI or SiC device technology.

We hope that Readers will find these Proceedings useful and interesting.

Guest editors: Andrzej Jakubowski, Aleksander Werbowy, Lidia Łukasiak

Invited paper

Silicon-germanium for ULSI

Steve Hall and Bill Eccleston

Abstract — The paper describes recent progress for the introduction of silicon-germanium, bipolar and field effect heterostructure transistors into mainstream integrated circuit application. Basic underlying concepts and device architectures which give rise to the desired performance advantages are described together with the latest state-of the-art results for HBT and MOSFET devices. The integration of such devices into viable HBT, BiCMOS and CMOS is reviewed. Other contributions that SiGe can make to enhance the performance of ULSI circuits are mentioned also.

Keywords — silicon-germanium, HBT, SiGe-CMOS.

1. Introduction

Pioneering work by Kasper et al at AEG (now Daimler-Chrysler) in the mid 1970s [1] and Bean et al at Bell Laboratories in the 1980's [2] gave rise to a new materials system for device engineers to employ. The associated heterojunction or band-gap engineering concept had been foreseen by both Shockley [3] and Kroemer [4] on a theoretical basis, in the earliest days of bipolar transistor technology. Seminal papers by Kroemer [5] in the 1980s have been inspirational to a generation of bipolar transistor device engineers resulting in the realisation of very high performance SiGe HBT devices with application to circuits which can operate in the lucrative 0.9÷5.8 GHz mobile phone and wireless LANS markets. The potential for the use of SiGe alloy in MOSFET devices for CMOS and particularly BiCMOS application has been recognised by the major companies. In fact, a number of companies are now offering products aimed mainly at the mobile communications and satellite markets and a good set of links to these is maintained by Douglas Paul at Cambridge University UK [6]. The SiGe technology is developing very rapidly and is driven by the large corporations. Production level CVD batch systems have been developed by IBM [7] who also offer most of the parts to realise SiGe HBT, r.f. solutions (see „Whitepaper" on IBM web-site). The most mature SiGe device is the heterojunction bipolar transistor and many companies have viable production process with $f_T >> 50$ GHz, in many cases compatible with their BiCMOS process. The performance and integratability of the HBT device into CMOS manufacturing are key requirements for immediate markets. The high performance HBT has the potential to replace the III/V components in mobile products allowing an all-Si solution.

In this paper, the basic concepts, development and most recent state-of-the art device and technology results will be presented in the context of mainstream application. The contributions by some of the UK University community will be a particular focus. Section 2 contains an account of SiGe HBT which offers the easiest incorporation of the new material into relatively standard production processes. Some ideas for low voltage logic circuits based on concepts closer to Kroemer's vision are contained within this section also. Section 3 describes oxidation of SiGe. The production of good dielectrics, together with the abundance of Si constitute the two key reasons for the success of Si in the market place compared to other semiconductors. Section 4 reviews recent progress towards the realisation of SiGe CMOS and the final sections contain comments on SOI-SiGe, other applications of SiGe and conclusions.

2. Heterojunction bipolar transistor

The inclusion of SiGe alloy into the base of a bipolar transistor produces a narrow band gap base region, whereby most of the band discontinuity appears in the valence band edge. This is extremely fortuitous as the associated potential barrier effectively serves to inhibit the reverse injection of holes into the emitter. Hole transport into the emitter constitutes the dominant base current mechanism so the result is a large increase in the current gain, β. In the context of SiGe HBTs it is more appropriate to say that the base current remains the same as an equivalent all-Si device, but the collector current is enhanced by the presence of SiGe in the base which implies increased minority carrier injection. The result is the same and the very high gain can be traded by pushing up the base doping level to reduce base resistance. The heavily doped base can also be made very thin for reduced base transit, taking care to maintain an adequate Early voltage V_A, especially for the case of analogue devices. Lower doped emitters can be used to reduce base-emitter capacitance also. Thus devices can be designed with very high f_T, $f_{\max}$ and also reduced base noise level. The Ge profile can be optimised for either digital (high f_T) or analogue (high βV_A) application as indicated in Fig. 1. A full account of physics and design issues together with details of process integration for 0.25 µm BiCMOS has been reported by IBM [8, 9]. The SiGe base is produced by epitaxy for optimal performance and is relatively easy to introduce into a manufacturing process with only marginal cost penalty.

The schematic diagram of Fig. 2 illustrates the IBM BiCMOS process. Extremely impressive performance has been reported for SiGe HBT's, with values of f_T and $f_{\max}$ of 130 [10] and 160 GHz [11] respectively and gate delays of 11 ps [12]. An 0.2 µm, near to BiCMOS compatible SiGe HBT technology was recently reported by Hitachi, with 107 GHz $f_{\max}$ and 6.7 ps ECL ring oscillator delay [13]. The HBT showed 47 GHz f_T at a lower current of 0.1 mA showing the potential for low power operation.

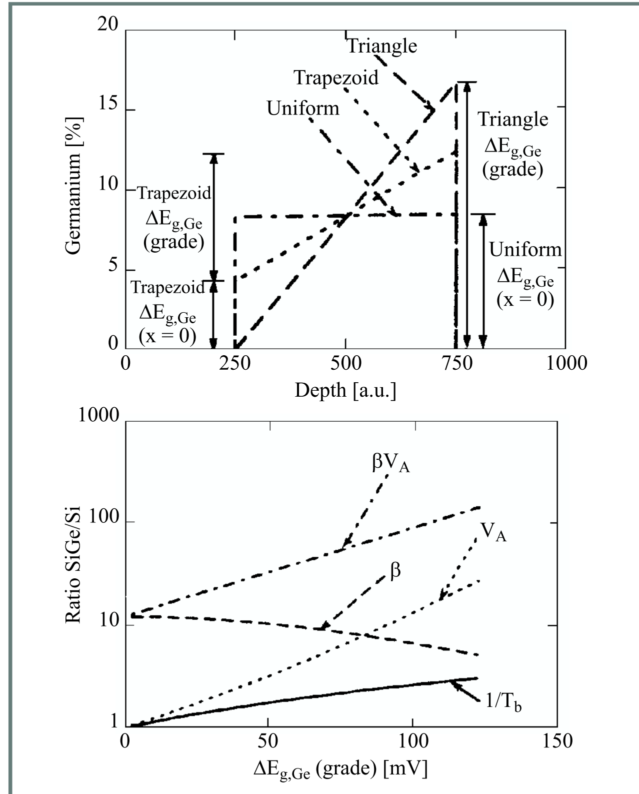

Fig. 1. Optimisation of base Ge profile for different applications (*reproduced from [8]*).

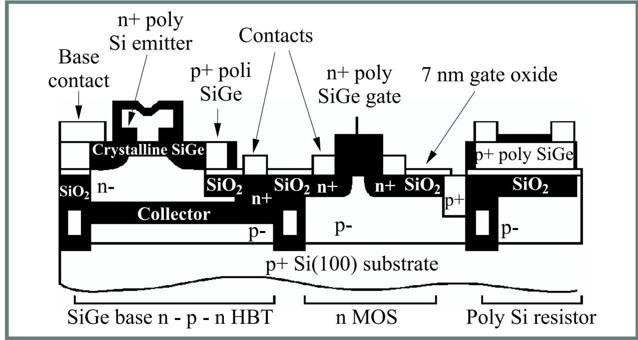

Fig. 2. Schematic diagram of IBM SiGE HBT BiCMOS process [8] (*diagram reproduced from [27]*).

As illustrated in Fig. 3, these devices are highly optimised in both the vertical and lateral dimensions, for high f_T and $f_{\max}$ respectively. Full integration of 55/90 $f_T/f_{\max}$ SiGe:C HBTs into a 0.25 μm BiCMOS process has been reported [14]. Note that carbon is incorporated to suppress B out-diffusion of the base. This out-diffusion is a particular problem of SiGe HBT technology because of the very highly doped base bounded by relatively lightly doped collector and emitter regions. The propensity for B out-diffusion is exacerbated by Si interstitial injection following extrinsic base implants: so-called transient enhanced diffusion. The out-diffusion causes parasitic barriers to be formed in the conduction band edge, reducing collector current and hence f_T. Thin, undoped SiGe spacer layers can help to alleviate the problem. Parasitic barriers can also form at high injection levels: the „modified Kirk effect".

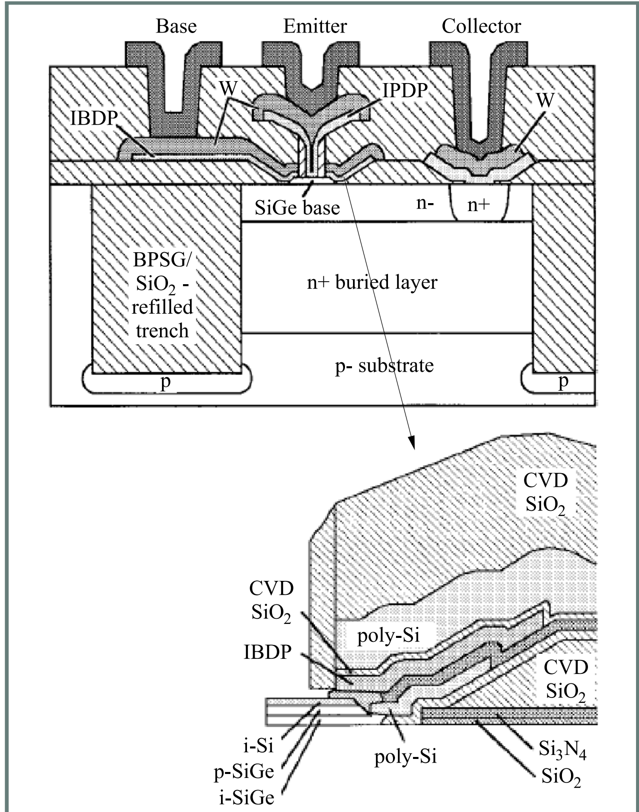

Fig. 3. State-of-the-art SiGe HBT: selective SiGe epitaxial base, self-aligned stacked metal/in-situ doped poly-Si (SMI) electrodes, trench isolation [13].

The initial approach by industry was to introduce the heterojunction into their standard poly-Si emitter processes and this does not bring the full benefits of the band-gap engineering concept. The primary motivation was the reduction of noise and perhaps most importantly, an early introduction of products into the market place. A further possible quick route to production is offered by forming the SiGe by Ge implantation [15] and this may be particularly useful for improving the performance of the p-n-p device for analogue application. There are considerable materials problems to overcome although the use of subsequent Si amorphisation and regrowth (EPIFAB process) pushes end of range defects deep into the substrate and can improve material quality [16].

The optimum route to achieve a truly optimised HBT involves selective and non-selective epitaxial growth and this strategy has been used in the state-of-the-art results achieved so far. The concept is illustrated in the architecture shown in Fig. 4 which shows a collector region grown with selective epitaxial growth (SEG) in an oxide window followed by a non-selectively grown (NSEG) base region and low doped emitter. A poly-Si emitter contact can be used to further increase gain. Such an approach allows full exploitation of the heterostructure principle although prob-

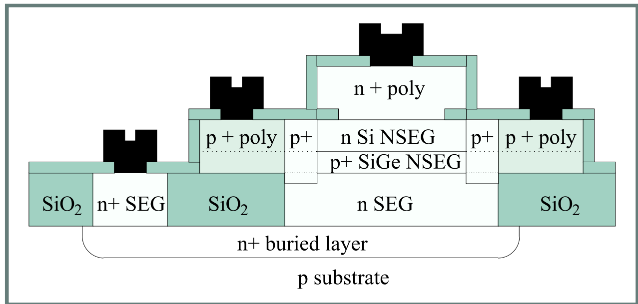

Fig. 4. Schematic diagram of SiGe HBT produced using selective epitaxy [17].

lems can exist with excess leakage currents at the collector periphery [17].

An advantage of HBT's is the reduced charge storage and this has initiated a re-appraisal of saturated logic families which can operate at very low voltages. Such a logic family is integrated injection logic (I^2L) which comprises of n-p-n switching transistors operating in inverse mode with integrated p-n-p [18] or resistive loads [19]. Gate delays down to 60 ps have been suggested by simulation; performance which is considerably slower than that of HBT-ECL. Nevertheless, the very low voltage effect supply voltage (~ 0.8 V), low power-delay product and high packing density looks attractive for mobile, mixed signal environments. The use of resistive loads rather the (poor) lateral p-n-p load can reduce I^2L gate delay further [19]. The SEG/NSEG approach allows self-aligned gate architectures closer to Kroemer's original vision whereby arrays of transistor operating in both normal and inverse modes can be realised in oxide windows to produce very compact low voltage circuits, as illustrated schematically in Fig. 5. The

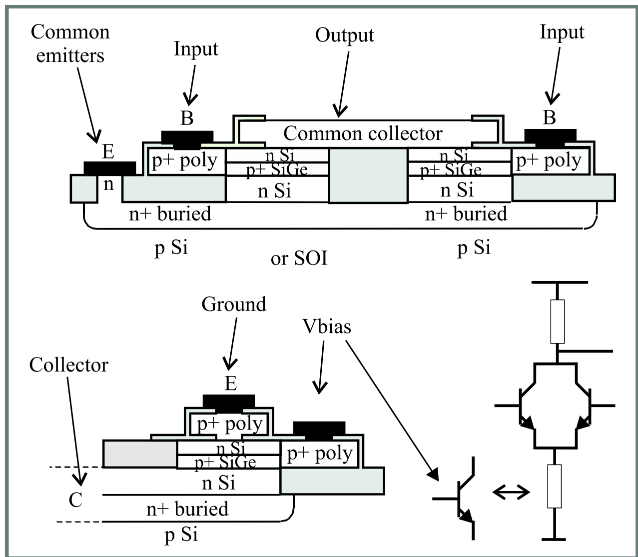

Fig. 5. Concept for high packing density, low voltage SiGe HBT logic. Top schematic shows emitter-down switches forming NOR logic; bottom diagram illustrates integration of an active bias (emitter-up) which could replace bottom resistor.

inherent symmetry of SiGe-HBT's is particularly suitable for collector up mode of operation and such HBTs with $f_{max} = 33$ GHz have been reported recently [20].

3. Oxidation of SiGe

The ability to realise a high quality dielectric and interface with semiconductor is a key factor in the success of Si technology. It is important that the incorporation of SiGe into the process flow does not compromise dielectric integrity. Growth rate enhancement (GRE) is apparent for wet thermal oxidation of SiGe but not for dry oxidation [21]. Our own experiments on low temperature plasma anodisation, using the system shown in Fig. 6, also show GRE but no Ge snow-plough [22, 23]. It has been suggested that oxida-

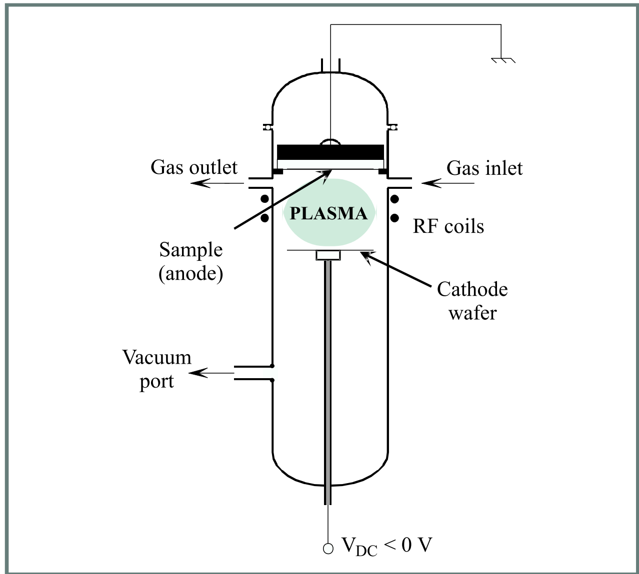

Fig. 6. Low temperature plasma anodisation system which allows growth of oxides at room temperature.

tion regimes that are surface reaction rate limited tend to lead to snow-ploughing of Ge from the growing film [22]. This produces a Ge-rich interface with high fast state density which is unsuitable with regard to both gate oxide and passivation application. Oxidation regimes that are mass transport limited tend to preclude snow ploughing of Ge and the surface can be inverted to allow transistor action [24] but the presence of unoxidised Ge in the oxide constitutes electron traps which compromise reliability [23]. It is unlikely that such effects can be overcome and the conclusion must be that direct oxidation of SiGe should be avoided. For this reason, the use of sacrificial Si capping layers that are partly consumed by gate oxidation is usual in SiGe MOS processes. Implanted Ge HBT processes can experience problems with poly-Si emitter/base engineering, associated with oxide growth rate enhancement. Reliability problems associated with SiGe HBTs as a result of SiGe oxidation are as yet unclear although it is likely that SiGe layers can be kept away from interfaces with dielectric by design. A further issue concerns the thermal budget for

the incorporation of strained layers into IC processes and the use of low temperature oxidation processes may be of interest in this regard in the future (see [22] for a review).

4. SiGe MOSTs and H-CMOS

The incorporation of SiGe into CMOS technology is far more problematic than that of SiGe HBTs into bipolar or even BiCMOS process flows. The motivation for incorporating SiGe is firstly that hole mobility can be enhanced allowing better matching of the p-channel and n-channel devices and there is also the potential for higher mobilities (μ) for both carrier types. This will increase drive capability which is the critical factor for both sub-micron (device length, L) technologies where the „μ/L^2" rule applies and very deep sub-micron technologies where interconnect capacitance becomes dominant. The key issue is that the added complexity of the SiGe CMOS process must bring sufficient benefit to be commercially viable. There are essentially two classes of device and both are constructed from successive layers of epitaxial material. The first is the modulation doped FET (MODFET), shown schematically in Fig. 7, which employs the so-called modulation doping concept whereby the channel is formed in undoped material with carriers provided by an adjacent doped layer. A conducting sheet of charge typically of the order low 10^{12} cm^{-2} thus exists prior to application of the gate voltage. Alternatively, a heterostructure device without doping can be produced with carriers induced purely by gating, as outlined in Fig. 8.

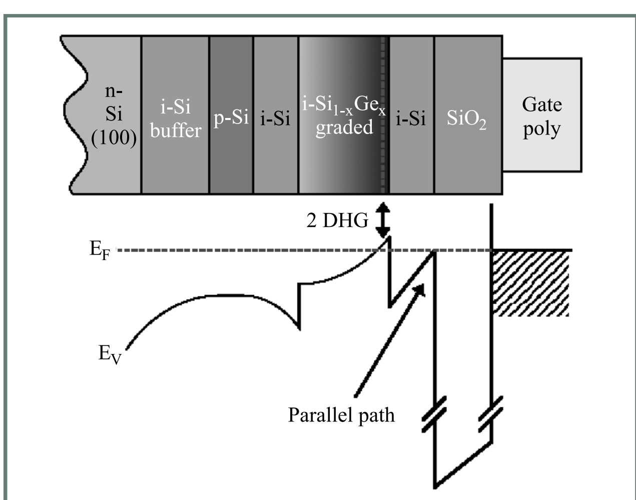

Fig. 7. Epitaxial layer structure illustrating the modulation doping concept [25] (*diagram reproduced from [27]*).

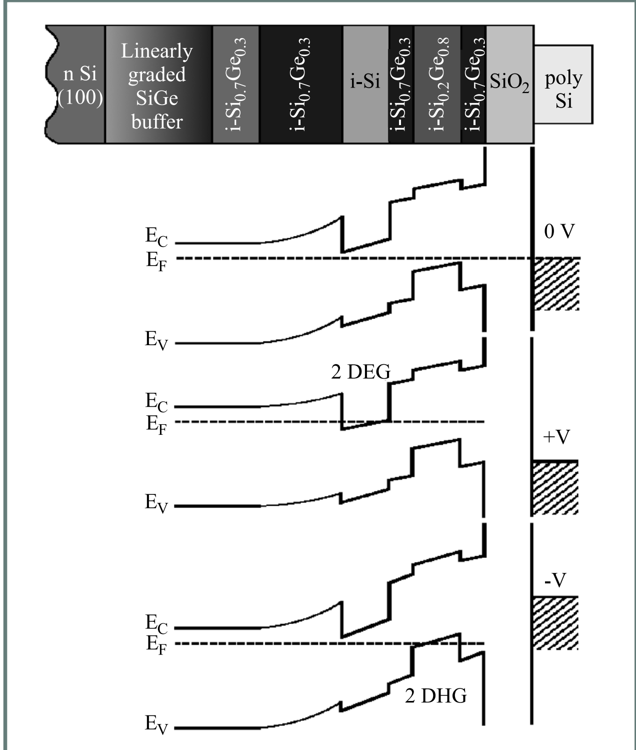

Fig. 8. Epitaxial layer structure illustrating the heterojunction MOS concept [34] (*diagram reproduced from [27]*).

As discussed in the previous section, there is a need to avoid the direct oxidation of SiGe and so a Si capping layer, upon which the gate oxide is formed, is included on top of the SiGe channel layer. The channel is thus buried and the transport is away from the comparitively rough Si/SiO_2 interface providing a further source of mobility improvement. Simple devices incorporating a so-called pseudomorphic SiGe layer has the band gap discontinuity in the valence band edge providing confinement of holes to form a buried channel. This means the device is suitable for p-MOST realisation but not for n-MOST. In terms of CMOS, this means that SiGe is incorporated into the p-channel device only; the n-MOST can be a conventional surface channel device. An important early study [25] produced a MODFET with best hole mobility of 220 cm^2 V^{-1}s^{-1} which is probably too low to justify the added complexity of incorporating the SiGe layer. Most recently, a high performance p-MODFET with a mobility of 930 cm^2 V^{-1}s^{-1} has been reported [26]. A preliminary study using low temperature grown gate oxides has produced both p- and n-channel devices with SiGe surface channels [24]. The device concept features surface channels of intrinsic SiGe and employs a sacrificial Si capping layer which is consumed by the plasma oxidation. The concept relies on the planarisation effect of PO whereby any surface roughness leads to field intensification.

More encouraging results have been obtained for devices built on so-called virtual substrates comprising of a linearly graded SiGe epitaxial buffer layer on a Si substrate. The grading serves to direct defects downwards away from the surface and in principle, very low defect density surfaces can be produced by this means. A further layer is grown and depending on the Ge concentration, band-edge discontinuities in either conduction or valence band can be realised so that both p- and n-channel buried channels can be formed. This approach may offer the best route to CMOS although there are considerable materials prob-

lems to overcome to realise reliably, low defect density virtual substrates, as reviewed in [27]. Record mobilities of 2830 cm^2 V^{-1}s^{-1} and 1300 cm^2 V^{-1}s^{-1} have been reported for n-MODFETs [28] and p-MODFETs respectively [29]. Fig. 9 shows relative performance of field effect devices [27] whereby SiGe n-MODFETs exhibit f_T comparable to III/V MODFETs and p-MODFETs show record performance.

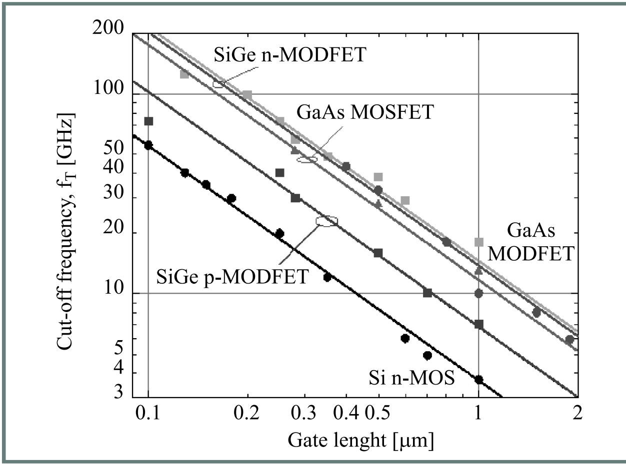

Fig. 9. Relative performance of high frequency field effect devices [27].

The conclusion from the individual device studies is that best results are obtained for a strained Si channel n-FET and strained SiGe (or Ge) channel p-FET [30]. The former devices have comparable speed performance to III/V devices and p-MODFETs have exhibited order of magnitude mobility improvements over conventional p-MOSFETs. Silicon based MODFETs have further advantages to III/V counterparts as a result of the better thermal conduction properties of Si although further work is required to ascertain noise performance. To implement these devices into CMOS production introduces a fresh set of problems. Progress into CMOS realisation has been reviewed by Maiti et al [31] and Schäffler [32]. The aim is to realise both n- and p-channel devices in a single set of epitaxial layers, without the requirement to return the wafers to the growth chamber. Designs have been reported based on modulation doping and more conventional MOSFET action. The devices have employed either Schottky or MOS gating. An early implementation [33] of CMOS employed a mesa isolation strategy similar to that of III/Vs. A n-MODFET was formed on a strain relaxed SiGe buffer. These layers were etched away locally to allow formation of a lower-level pseudo-morphic SiGe channel p-MODFET. Schottky gates were used. Downward penetrating defects from the buffer layer made the p-channel device unacceptably poor however. A somewhat similar concept also employing (Pt) Schottky gates was suggested by Ishmail [30]. For commercial processes, MOS gates are preferred to Schottky gates for reasons of leakage, reproducibility and reliability. The aim also is to produce both device types on the same strain-adjusting layer thus avoiding the need for local removal of layers and maintaining planarity. Note that compromises are required in the individual device design as it is not feasible to produce separate virtual substrate layers individually for p- and n-channel devices. The planar CMOS concept of Ishmail [30], later reported by Sadek et al [34] and illustrated in Fig. 10, uses a 30% Ge, SiGe virtual substrate with a strained Si channel n-MOSFET and a subsequent SiGe (> 70% Ge) channel for the p-MOSFET. Common

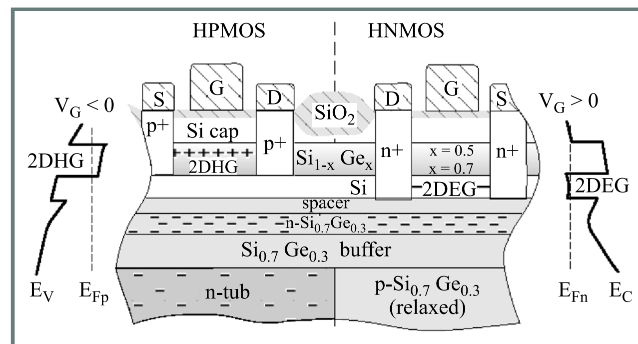

Fig. 10. Complementary HMOSFET with a Si channel for the n-type and an SiGe channel for the p-type device. A common relaxed buffer is used for both transistors [34] (*diagram reproduced from [32]*).

gate material of p+ poly-Si can be used if layer dopings are adjusted appropriately, to produce quite low threshold voltage (< 0.4 V) required for low power operation. Full CMOS with a SiGe p-MODFET and conventional surface channel n-MOSFET has been realised with hole mobility of over 320 cm^2 V^{-1}s^{-1} [35], using LTO deposited and plasma anodic gate oxides. Finally, large electron and hole mobilities (> 2000 cm^2 V^{-1}s^{-1}) have been predicted for strained Si channels [36]. The ability to use strained Si for both channels suggests a simpler CMOS process.

5. Other applications of SiGe

Silicon germanium has been used in a number of other ways in IC processes. Vertical MOSFETs can benefit from a SiGe source region: a reverse heterojunction effect whereby the gain of the parasitic bipolar transistor formed by source/body/drain is reduced considerably giving higher breakdown voltage for the MOST [37]. Poly-SiGe (50% Ge) looks attractive as an alternative gate electrode material for reduced threshold voltages and common gate material in CMOS application [38], where the work function can be tailored by the Ge concentration. Gate poly depletion effects are ameliorated also by the enhanced dopant activation at low temperatures. Implanted Ge in the drain region of MOSFETs can alleviate hot electron effects due to the reduced ionisation threshold arising from the lower band gap [39]. SiGe can also be used as an etch-stop in bonded wafer SOI technology. The temperature coefficient of resistance can be controlled in polycrystalline SiGe resistors for better thermal performance. Finally, thin film poly SiGe transistors offer higher carrier mobility for large area

electronics whereby pixel addressing driver circuitry can be realised on the flat panel displays for a cheaper solution.

6. SiGe-on-insulator

Introduction of silicon-on-insulator substrates brings additional benefits to the fabrication of SiGe MOSFETs as well as the inherent advantages of SOI technology in its own right. For MOS application, the elasticity of the buried insulator can help reduce the defect density of SiGe layers and also provide a simplified CMOS process to aid integration of SiGe into the process flow. SOI brings its own benefits including ease of isolation, reduced drain/source and bulk capacitances and increased packing density [40]. A recent result from Toshiba [41] demonstrates hole mobilities greater than the universal mobility of Si for non-optimised layer structure. For HBT's, SOI substrates offer reduced collector to substrate capacitance as well as ease of isolation. A 60 GHz f_T super self-aligned HBT on SOI has been realised by NEC fabricated on SOI substrate and its application to 20 Gbit/s optical transmitter IC's demonstrated [42]. An advanced technology for r.f. application has been proposed whereby an SOI-SiGe HBT has been realised using bonded wafer technology and is illustrated schematically in Fig. 11. The buried ground plane produces

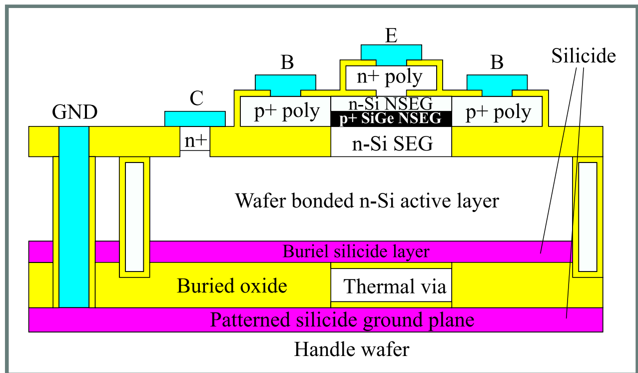

Fig. 11. Schematic of the „ultimate" r.f. transistor featuring SEG/NSEG epitaxial growth, trench isolation, SOI substrate with thermal vias. Low resistance silicide layer for low collector resistance and buried ground plane under the buried oxide, for cross-talk suppression. (*By kind permission Prof. P. Ashburn, Southampton University, UK, Prof. H. S. Gamble, Queen's University Belfast, UK*).

effective screening of analogue and digital circuits on the same substrate (mixed signal). This buried ground plane concept has been demonstrated to achieve nearly −90 dB suppression of substrate cross-talk [43]. The technology also features thermal vias to allow the heat to escape – a significant problem with SOI technology particularly for analogue application. Heating can cause thermal run-away in HBT's and reduction of drive capability due to mobility degradation in MOSFET devices.

7. Conclusions

SiGe can be used to further improve Si bipolar and MOSFET device performance in quite a wide variety of ways. SiGe BiCMOS is undoubtedly the main driver for the industry in the short term, because of the benefits it can bring to wireless markets. A number of products are also available in SiGe HBT where the low noise and high frequency of operation are particularly noteworthy. Some doubt remains as to whether full SiGe CMOS will make it to the market place due to the high costs of new fabrication plants and the need to comply with the SIA roadmap. In any event, it may be that other technologies such as SOI can provide the improved performance in a more cost-effective way. It is conceivable that both SOI and SiGe CMOS will be used for a „last generation" of CMOS when existing scaling strategies run out of steam. However, it is almost certain that SiGe material will find a place in mainstream ULSI CMOS in some capacity and a likely contender is its use as gate material for low power application.

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Paper

CVD growth of high speed SiGe HBTs using SiH_4

Henry H. Radamson, Jan Grahn, and Gunnar Landgren

Abstract — The growth of high frequency HBT structures using silane-based epitaxy has been studied. The integrity of SiGe layers in the base and the control of the collector profile using As- or P-doping grown at 650°C have been investigated. The results showed that the growth rate of SiGe layers has a strong effect on the evolution of defect density in the structure. Furthermore, B-doped SiGe layers have a higher thermal stability compared to undoped layers. The analysis of the collector profiles showed a higher incorporation of P in silane-based epitaxy compared to As. Meanwhile, the growth of As- or P-doped layers on the patterned substrates suffered from a high loading effect demanding an accurate calibration.

Keywords — SiGe, epitaxy, HBT, silane.

1. Introduction

Silicon-germanium alloys are extendedly used for novel electronic devices such as heterojunction bipolar transistors (HBT) [1–5] and quantum well devices [6, 7] during recent years. The developments in the epitaxial technologies e.g. molecular beam epitaxy (MBE) [1, 3] and chemical vapor deposition (CVD) [8, 9] have provided the possibility to fabricate HBTs with high quality for high frequency application [1–5]. Both selective [10] and non-selective [4] growth processes were applied to integrate the SiGe epitaxial layers in device structures. In general, the base and the collector doping profile are the significant keys for high frequency behavior in HBTs. Selectively implanted collectors (SIC) are commonly used in high-speed medium breakdown voltage bipolar processes [11, 12]. A retrograded profile with $2\cdot10^{18}$ cm^{-3} has been used a collector layer in a HBT to obtain a cut-off frequency of 90 GHz [12]. The drawback with this technique is that a RTA step around 1000°C is needed to remove the implantation induced effects. This method may not be suitable for HBTs designed for cut-off frequency above 100 GHz since the annealing step degrades the quality of SiGe layer and can affect the performance of the device. A potentially superior method for fabricating a desired collector profile is to apply epitaxy for accurate control of the doping profile. In contrast to ion implantation, abrupt and defect-free buried layers can be grown. Low temperature epitaxy using both P and As as n-type dopants has been investigated by several authors [10, 13–15]. In these studies, the growth temperature for silane-based epitaxy has been in the range of $700 \div 800$°C and a fully controlled dopant profile was not achieved.

One of the important points for the manufacturing devices is the thermal stability of epitaxial layers. Any outdiffusion of the dopants from the base or the collector affects severely the high frequency performance behavior. Defects in a HBT structure decreases the carrier mobility causing a degradation of the device performance. It has been reported previously that SiGe layers grown at low temperature contain a higher defect density and the thermal stability was poor [16]. Thus, investigating the thermal stability can be used as a criteria to compare the defect density of the epi-layers. This can be used as a feed-back for optimizing the growth parameters to improve the quality of SiGe layer. In general, a high annealing temperature causes a partial relaxation which degrades the performance of the device. This limits the thermal budget of the process and must be considered as an important point in designing of the structure. One of the most powerful tools to detect a minor relaxation is high resolution X-ray diffraction. This technique is a non-destructive method which has been used to characterize and quantify the lattice misfit parallel and perpendicular to the growth direction. Thus the relaxation amount can be calculated from the derived misfit parameters.

Another point to be considered for the growth of HBT structures on patterned substrates is that the growth rate differs from the blanket wafers. This effect so-called loading effect can influence the Ge and dopant profiles requiring an accurate calibration in the case of the patterned substrates.

In this paper we present the growth of high frequency HBTs using silane-based epitaxy. We also propose a way to minimize the defect density in the SiGe base layer and a study of the incorporation of As or P in the Si collector layer at low temperature is presented.

2. Experimental details

Silicon-germanium samples were grown on blanket and patterned Si(100) substrates in Epsilon 2000 ASM CVD reactor. The reaction chamber is isolated from the clean room ambient by two nitrogen purged loadlocks. Si substrates were chemically cleaned and loaded for at least 30 min purging in the loadlock. *In-situ* cleaning were performed by baking at 1100°C for 2 min and 950°C for 20 min in H_2 in the reactor for the blanket and the patterned substrates, respectively. The epitaxial growth was carried out 650°C under atmospheric or reduced pressure (ATMP/RP) of 40 torr using SiH_4 as the silicon source. Gas sources of 10% Ge, 1% PH_3, 1% AsH_3 and 1% B_2H_6 in H_2 were used to grow

the structures. The As, P and B concentrations in the epilayers were determined by secondary ion mass spectrometry (SIMS) and the Ge content by using X-ray diffraction. Boron concentration in SiGe was in the range of $5 \cdot 10^{18}$ to $1 \cdot 10^{21}$ cm^{-3} and the Ge amount 10÷20%. The concentration of As or P in the collector was in the range of $2 \cdot 10^{17} \div 2 \cdot 10^{18}$ cm^{-3}.

High resolution reciprocal lattice mapping (HRRLM) [17, 18] were obtained by using a Philips Expert high resolution, multi-reflection X-ray diffractometer with Cu $K_{\alpha 1}$ radiation. The equipment limits the angular divergence of both the incident and detected beams to 12 arcsec or less. A HRRLM can be obtained by performing several $\omega/2\Theta$ scans, i.e. rotation of both the sample and the detector with a ratio of 1:2 (ω: angle of incidence, 2Θ: the diffraction angle), for a range of incident angles $\omega + \Delta\omega$ as the starting value. In a HRRLM, an ω-scan probes the orientation variations for defined interplanar spacing, while an $\omega - 2\Theta$ scan probes interplanar spacing variations for the same orientation. The shape and position of the substrate and the layer peaks in HRRLM provide information about the misfit for both the directions parallel and perpendicular to the surface and thus relaxation amount can be calculated.

3. Results and discussions

3.1. The growth of collector layers

Figure 1 shows SIMS profiles of four samples with a buried As and P layer grown at 650°C (a) $6 \cdot 10^{17}$ and $2 \cdot 10^{18}$ cm^{-3} without and with 30 sccm HCl (selective mode) and (b) P-doped layer with concentration $1 \cdot 10^{18}$ cm^{-3}. Figure 1a shows an As segregation towards the undoped Si causing a background doping of $4 \div 7 \cdot 10^{17}$ cm^{-3}. Adding HCl to obtain a selective mode decreases the growth rate, however it has no effect on the As segregation. SIMS measurements from other series of As-doped samples show that the background doping in the Si undoped cap layer remains at the same level for buried layers with As concentration in range of $5 \cdot 10^{17}$ to $3 \cdot 10^{18}$ cm^{-3}. Our results showed that an annealing treatment of the buried layers slightly improves the profile of the samples in Fig. 1a, however, it is still far from acceptable. Figure 1b illustrates that the incorporation of P is higher in SiH_4-based epitaxy with a sharper leading edge. This makes P attractive for low temperature epitaxy, however, a low thermal budget is demanded in manufacturing of the device to avoid any out-diffusion of the P from the collector layer. The previous reports have not succeeded to illustrate a fully-controlled P-doped buried layers grown at reduced pressure using silane-based epitaxy. This is due to the applied growth temperature in the range of 700 ÷ 800°C which is considerable high temperature due to high P diffusivity.

Applying the low temperature epitaxy of As-doping in a bipolar transistor structure e.g. Si:As/i-Si/Si:B ($1 \cdot 10^{19}$ cm^{-3})/i-Si creates a problem in a larger scale.

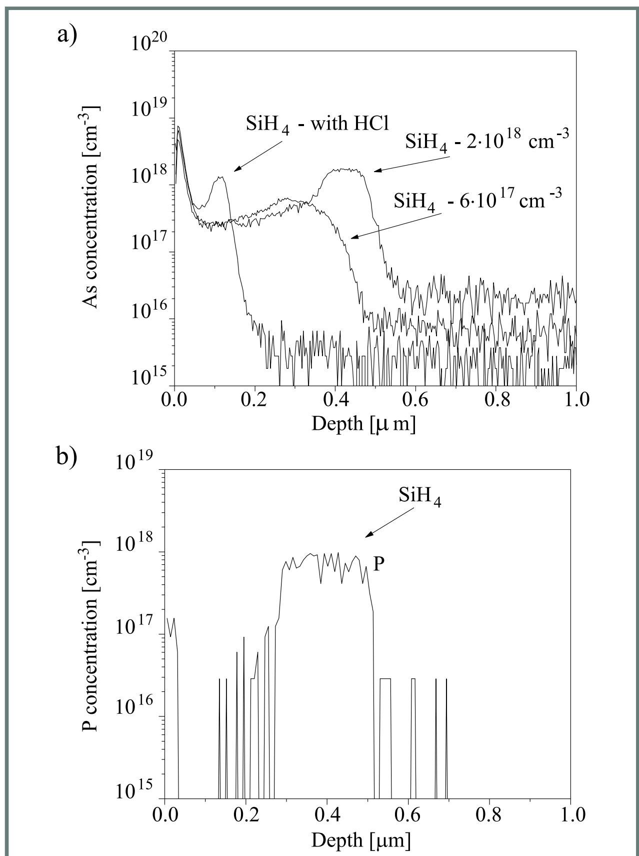

Fig. 1. SIMS profiles for buried n-type layers grown at 650°C, 40 torr (a) As-doped layers without and with HCl (selective mode), and (b) P-doped layer.

Figure 2 shows SIMS results of integrated As-doped layers with concentration of (a) $2 \cdot 10^{18}$ cm^{-3}, and (b) $2 \cdot 10^{17}$ cm^{-3}. The surface segregated As atoms incorporate strongly in the in the base layer due to presence of B impurities, creating a highly compensated layer. The device simulations show that the high n-type doping concentration (segregated atoms) in the base results in a punch-through condition for the low forward bias. These results indicate that As-doped layers using silane is not suitable for low temperature epitaxy of HBT structures. In addition, the growth of As-doped layers on patterned substrates showed a high loading effect of ~30% (a thinner collector layer) while P-doped layers showed a lower value of ~15%.

3.2. The growth of SiGe base layers

The other crucial point for the high frequency performance of HBTs is the base technology. In order to study the evolution of the defects in SiGe layers a series of undoped layers were grown at atmospheric and reduced pressure. Figure 3 shows Ge-content vs germane flux for different silane flux for samples grown at ATMP or RP. There is a sensitivity limitation for Mass-Flow-Controller which has also marked in the figure. The figure shows that a higher germane flux is required for RP-grown layers compared to ATMP-grown layers in order to obtain a certain Ge content. Our results

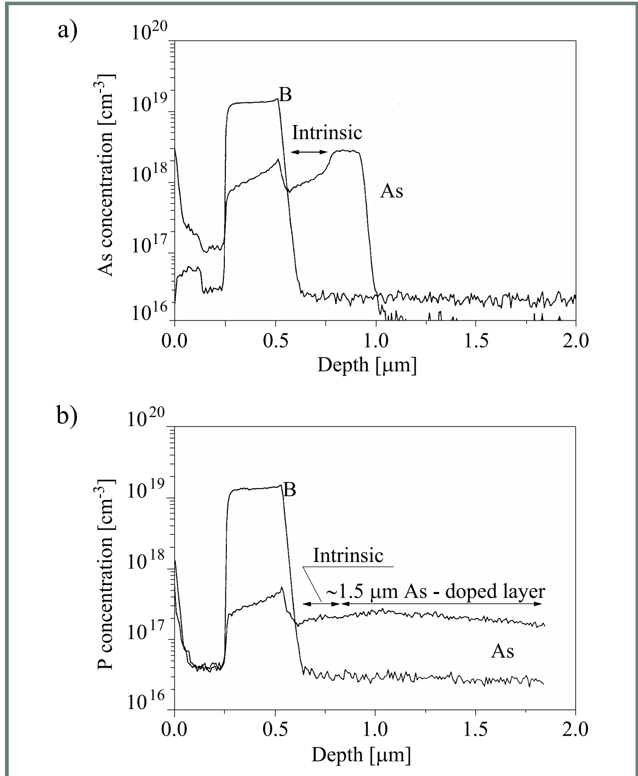

Fig. 2. SIMS profiles of As-doped layer with concentration of (a) $2 \cdot 10^{18}$ cm^{-3}, and (b) $2 \cdot 10^{17}$ cm^{-3} integrated in a bipolar transistor structure.

show also that the growth rate of RP-grown samples is higher than ATMP-grown for a specific Ge in above figure. This raises the question if the incorporation of defects is affected by growth rate and consequently could alter the

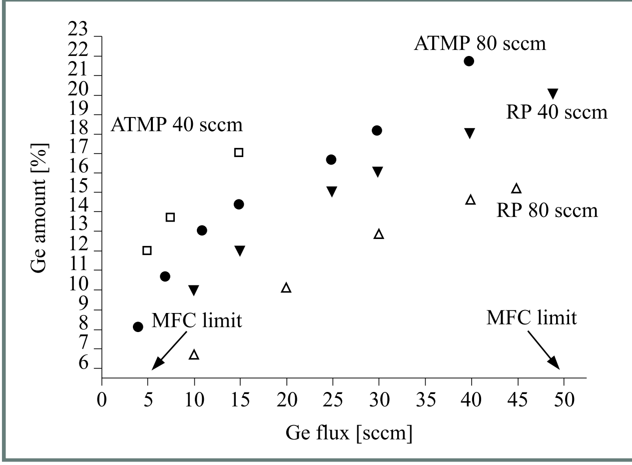

Fig. 3. A plot of Ge amount versus Ge flux for ATMP- and RP-grown samples with silane flux of 80 and 40 sccm.

thermal stability. To support this hypothesis we have grown SiGe samples at atmospheric and reduced pressure with different growth rates. By changing SiH_4 and GeH_4 fluxes but preserving the fraction of the fluxes, the growth rate could be modulated for a certain Ge amount. In order to compare the epitaxial growth quality of the epilayers we have

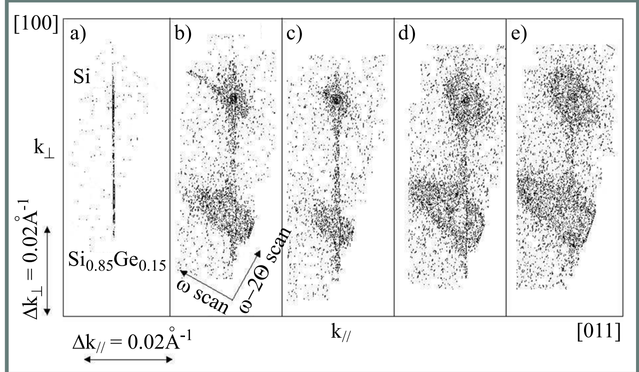

Fig. 4. High resolution reciprocal lattice mapping around the (311) reflection of a 1200 Å thick as-grown or RTA at 900°C for 10 s of $Si_{0.85}Ge_{0.15}$ layers with growth rate; (a)÷(d) explanation in the text.

studied the thermal stability of the samples by annealing at 900°C for 10 s. In this way, the samples with different defect density can be easily distinguished. Figure 4 shows HRRLM of $Si_{0.85}Ge_{0.15}$ RP-grown layers with a thickness of 1200 Å: (a) as-grown with growth rate of 156 Å/min, and annealed samples at 900°C for 10 s grown with growth rate of (b) same in (a), (c) 218 Å/min, (d) 368 Å/min, and (e) 392 Å/min. All the as-grown samples in Figs. 4b to 4e had an identical feature shown in Fig. 4a. The parallel-to-surface lattice mismatch for as-grown samples is zero to the accuracy of the measurements indicating that the layers were fully strained. However, all annealed samples in Figs. 4b to 4e show a mosaicity broadening in ω-direction which is an indication of a partial relaxation of SiGe layers. The amount of mosaicity broadening is an image of defect density of epi-layers. It is obvious that SiGe layer illustrated in Fig. 4c has a minimum defect density.

Figure 5 shows the growth rate versus Ge-content for RP- or ATMP-grown samples. In this investigation the samples were grown with the same thickness for a certain Ge concentration in the metastable region. HRRLM was performed to investigate the thermal stability of all samples in Fig. 5 similar shown in Fig. 4. A „×” mark in the figure show the samples with minimum defect density. These results indicate that the defect density in SiGe layers can be decreased by choosing an appropriate growth rate which varies depending on the Ge-content. These results show that the optimized growth rate is a parameter which must be considered in the integrity of SiGe layers for device applications.

Figure 6 shows HRRLM of ATMP-grown $Si_{0.87}Ge_{0.13}$ with 1200 Å thick (a) as-grown undoped layer, (b) sample in (a) was annealed at 900°C for 10 s, (c) B-doped with concentration of $1 \cdot 10^{19}$ cm^{-3}, (d) sample in (c) was annealed at 900°C for 10 s. The as-grown layers show no defects while the annealed layers show a mosaicity broadening indicating partial relaxation. The B-doped SiGe samples show a smaller mosaicity broadening in comparison with the undoped layers in the figure. In general, the boron atoms at substitutional sites induce a tensile

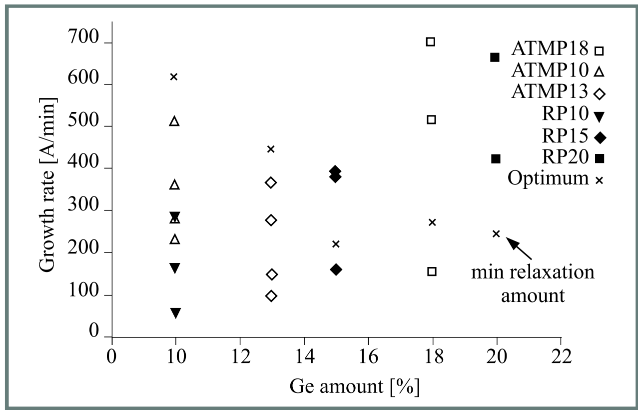

Fig. 5. A plot of growth rate versus Ge amount for ATMP- and RP-grown samples. „×" mark shows the samples with minimum defect.

strain with lattice contraction coefficient relative to silicon of $6.3 \pm 0.1 \cdot 10^{-24}$ cm^{-3}/atom [19] which counteract the strain induced by Ge atoms. This compensation effect results in a shift in the (100)-direction of the layer. This compensation effect in principle should increase the thermal stability of SiGe. However, the effects is negligible for boron concentration of $1 \cdot 10^{19}$ cm^{-3} and the tetragonal lattice strain induced by Ge atoms is dominant. The boron doping in SiGe is high causing a decrease in the density of the self-interstitials. This may act as an important factor for retarding the relaxation of SiGe layer since the activation energy for nucleation and formation of dislocations has been increased due to a lower defect density. This in turn may be responsible for the higher thermal stability of B-doped SiGe layers. HRRLMs showed that a defect-free SiGe layer with boron concentration of $5 \cdot 10^{20}$ cm^{-3} can be obtained. This value is close to the earlier reported value of $3 \cdot 10^{20}$ cm^{-3} for B-doped SiGe layer grown by MBE [20].

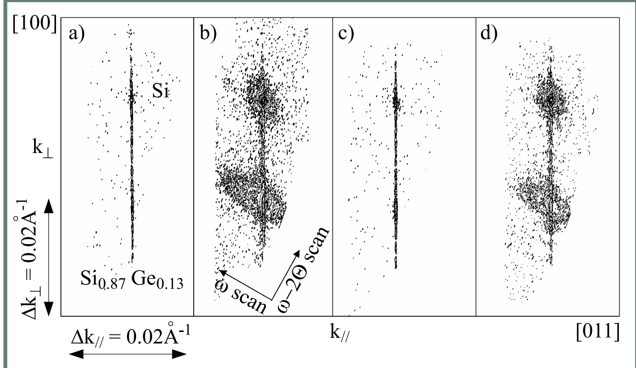

Fig. 6. High resolution reciprocal lattice mapping around the (311) reflection of a 1200 Å thick $Si_{0.87}Ge_{0.13}$ (a) undoped layer, (b) sample in (a) was RTA at 900°C for 10 s, (c) B-doped layer with concentration of $1 \cdot 10^{19}$ cm^{-3}, (d) sample in (c) was RTA at 900°C for 10 s.

4. Conclusions

P-doped buried layers grown at 650°C using silane as Si source shows abrupt profiles in contrary to As-doped layers which suffers from a high segregation. This makes P an attractive dopant for the growth of collector layers in HBTs. A high loading effect was observed in growth of As- and P-doped layers on the patterned substrates demanding an accurate calibration. The incorporation of defects in SiGe base layer depends strongly on the growth rate and an optimum point with minimum defect density can be obtained. B-doping in SiGe increases thermal stability in comparison with the undoped SiGe layers. Moreover, a defect-free SiGe B-doped layers with concentration $5 \cdot 10^{20}$ cm^{-3} has been obtained.

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Paper

Optimization of selected parameters of SiGe HBT transistors

Agnieszka Zaręba and Andrzej Jakubowski

Abstract — SiGe-base HBTs with Gaussian doping distribution are modeled including the effect of the drift field and variable Ge concentration in the base on the diffusion coefficient. Two different Ge distributions in the base are considered: a triangular one and a box one.

Keywords* — *heterojunction bipolar transistor, base transit time, current gain.

1. Introduction

The past few years have seen significant progress in SiGe heterojunction bipolar transistor (HBT) technology. Today, the use of SiGe-base HBTs is becoming increasingly popular in wireless and high-speed digital communications. In these transistors, band gap grading gives rise to a drift field which aids the minority carrier transport through the base. This fact has been used to realize devices with high cut-off frequency f_T (over 100 GHz).

The design of Ge profile and base doping profile to minimize the base transit time in SiGe HBTs has been studied extensively in the literature [1–5]. The triangular Ge profile is effective in optimizing the band gap grading in the base to minimize $t_{B\mathrm{SiGe}}$ (base transit time-the dominant factor in f_T).

Since the exponential base doping profiles and similar ones have already been examined [4, 5] our purpose was to investigate the Gaussian distribution of dopants in the base. In conventional devices such a distribution resulted in a decreased base transit time [6], therefore it would be useful to estimate its influence on the SiGe HBT. Moreover, in real transistors the doping profiles are closer to a Gaussian distribution than to an exponential one.

Two important parameters of the SiGe HBT are modeled, i.e. base transit time and current gain. The model incorporates not only high-doping effects but also the dependence of the diffusion coefficient on the drift field and the variable Ge concentration along the base.

Two types of Ge distribution in the base are examined: the triangular one and the box one [4, 7].

2. Theory

2.1. The base transit time

The base transit time $t_{B\mathrm{SiGe}}$ of a n-p-n SiGe HBT may be expressed as [8]

$$t_{B\mathrm{SiGe}} = \int_0^{W_B} \frac{n^2_{i\mathrm{SiGe}}(y)}{N_A(y)} \left(\int_z^{W_B} \frac{N_A(x)}{n^2_{i\mathrm{SiGe}}(x) D_{n\mathrm{SiGe}}(x)} dx \right) dy , \quad (1)$$

where W_B – base width, N_A – base doping, $n_{i\mathrm{SiGe}}$ – intrinsic carrier concentration of the SiGe base given as [8]

$$n^2_{i\mathrm{SiGe}}(x) = n^2_{i0} \exp\left(\frac{\Delta E_g}{\mathrm{k}T} \frac{x}{W_B} \right) , \quad (2)$$

where n_{i0} – intrinsic carrier concentration in undoped Si, k – the Boltzmann constant, T – temperature [K], ΔE_g – effective band gap reduction in the base due to the presence of Ge ($\Delta E_{g\mathrm{Ge}}$) and due to heavy doping effects (ΔE_{gDOP}):

$$\Delta E_g(x) = \Delta E_{g\mathrm{Ge}}(x) + \Delta E_{gDOP}(x) . \quad (3)$$

The band gap narrowing due to the presence of Ge is assumed to have a linear dependence on Ge concentration: 7.5 meV per 1% of Ge [5] and the Slotboom – de Graff band gap narrowing model [9] is used to model (ΔE_{gDOP}):

$$\Delta E_{gDOP} = = 9\ \mathrm{meV} \left(\ln\left(\frac{N_A(x)}{10^{17}} \right) + \sqrt{\ln^2\left(\frac{N_A(x)}{10^{17}} \right) + 0.5} \right) . \quad (4)$$

The model of electron mobility in a SiGe base used in our analysis is as follows [4]

$$\mu_{n\mathrm{SiGe}}(x) = \left(1 + 3y_{\mathrm{Ge}}(x) \right) \mu_{n\mathrm{Si}}(x) , \quad (5)$$

where $\mu_{n\mathrm{SiGe}}(x), \mu_{n\mathrm{Si}}(x)$ – electron mobility in the SiGe base and in silicon, respectively and $y_{\mathrm{Ge}}(x)$ – Ge concentration in the base.

The model of the impurity-concentration-dependent and the electric-field-dependent electron mobility in silicon proposed in [6] has been used

$$\mu_{n\mathrm{Si}} = \frac{\mu_{nc}}{\sqrt{1 + \dfrac{\left(\dfrac{\mu_{nc}|E(x)|}{\nu_c} \right)^2}{\left(\dfrac{\mu_{nc}|E(x)|}{\nu_c} + G_n \right)} + \left(\dfrac{\mu_{nc}|E(x)|}{\nu_S} \right)^2}} , \quad (6a)$$

$$\mu_{nc} = \mu_{n1} + \frac{\mu_{n0}}{1 + \dfrac{N_A(x)}{N_{ref}}} , \quad (6b)$$

where: $\mu_{n1} = 232$ cm^2/Vs, $\mu_{n0} = 1180$ cm^2/Vs, $\nu_c = 4.9 \cdot 10^6$ cm/s, $\nu_S = 1.04 \cdot 10^7$ cm/s, $G_n = 8.8$,

$N_{ref} = 8 \cdot 10^{16}$ cm^{-3}. Using Einstein's relation, the electron diffusion coefficient may be obtain from the following equation:

$$D_{n\mathrm{SiGe}}(x) = \frac{\mathrm{k}T}{q}\mu_{n\mathrm{SiGe}}(x) \ . \tag{7}$$

To express the base doping profile we introduced a Gaussian-type function

$$N_A(x) = N_0 \exp\left(-\ln\left(\frac{N_0}{N_C}\right)\left(\frac{x}{W_B}\right)^2\right) . \tag{8}$$

This function satisfies the boundary conditions

$$N_A(0) = N_0 \ , \tag{9a}$$

$$N_A(W_B) = N_C \ . \tag{9b}$$

Additionally, we assume that the drift field at the base-collector junction is large enough to saturate the electron velocity. The transit time through the neutral base region is thus given by

$$\mathrm{t}_{B\mathrm{SiGe}} = \int_0^{W_B} \frac{n^2_{i\mathrm{SiGe}}(y)}{N_A(y)}\left(\int_z^{W_B} \frac{N_A(x)}{n^2_{i\mathrm{SiGe}}(x) D_{n\mathrm{SiGe}}(x)}dx\right)dy + \\ + \frac{1}{\nu_S}\int_z^{W_B} \frac{N_A(W_B) n^2_{i\mathrm{SiGe}}(x)}{n^2_{i\mathrm{SiGe}}(W_B) N_A(x)} dx \ , \tag{10}$$

where ν_S is the saturation velocity of electrons. Comparing (1) and (10) one may easily see that the base transit time is higher in the latter case.

2.2. The current gain

The influence of the variations of the band gap, Eq. (3) and electron diffusion coefficient, Eq. (7) on the dc terminal properties of the SiGe HBT may be expressed in a closed-form for a Gaussian base doping profile, Eq. (8) using the generalized Moll-Ross formula [8]:

$$J_{C\mathrm{SiGe}} = \frac{q\left(\exp\left(\frac{qU_{BE}}{\mathrm{k}T}\right) - 1\right)}{\int_0^{W_B} \frac{N_A(x)}{n^2_{i\mathrm{SiGe}}(x) D_{n\mathrm{SiGe}}(x)}dx} = \\ = J_{C0\mathrm{SiGe}}\left(\exp\left(\frac{qU_{BE}}{\mathrm{k}T}\right) - 1\right) , \tag{11}$$

where all parameters have been defined above. Incorporation of the carrier velocity saturation effects to $J_{C0\mathrm{SiGe}}$ yields the following expression [10]

$$J_{C0\mathrm{SiGe}} = \frac{q}{\int_0^{W_B} \frac{N_A(x)}{n^2_{i\mathrm{SiGe}}(x) D_{n\mathrm{SiGe}}(x)}dx + \frac{N_A(W_B)}{n^2_{i\mathrm{SiGe}}(W_B)\nu_S}} \ . \tag{12}$$

For identically constructed devices, the ratio of β between SiGe HBT and Si BJT can be determined from the equation [7]

$$\left.\frac{\beta_{\mathrm{SiGe}}}{\beta_{\mathrm{Si}}}\right|_{U_{BE}} \approx \left.\frac{J_{C0\mathrm{SiGe}}}{J_{C0\mathrm{Si}}}\right|_{U_{BE}} \ . \tag{13}$$

3. Results

In the present study, we have considered a SiGe-base HBT transistor with the neutral base width of 50 nm and the Gaussian doping profile with the peak concentration $N_0 = 10^{19}$ cm^{-3} and minimum concentration $N_C = 10^{17}$ cm^{-3}.

First of all we have examined transistor with triangular Ge profile with concentration at the emitter edge of base $y_{E\mathrm{Ge}} = 0\%$ and varying concentration of Ge at the collector edge $y_{C\mathrm{Ge}}$.

The ratio of the base transit time $t_{B\mathrm{SiGe}}/t_{B\mathrm{Si}}$ (for identically constructed HBT and BJT) is plotted in Fig. 1 as a function of $y_{C\mathrm{Ge}}$. To illustrate the influence of the drift field

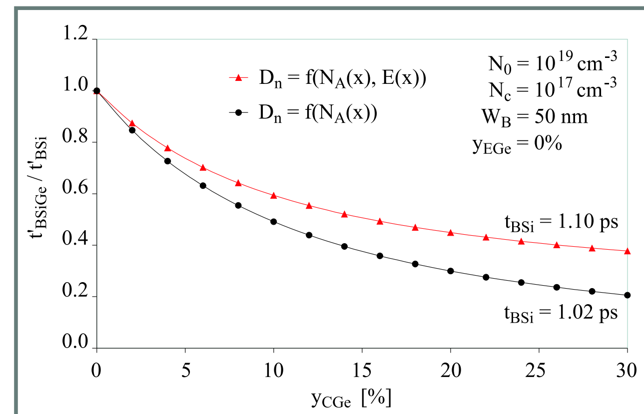

Fig. 1. Normalized base transit time versus Ge concentration at the collector edge of the base for cases: diffusion coefficient dependent and independent on the drift field.

the base transit time was calculated in two ways: with the diffusion coefficient either dependent or independent of the field. The high-doping effects were taken into account in both cases. As seen calculation of the base transit time assuming diffusion coefficient independent on the field underestimates the value of this parameter.

The current gain β was studied in a similar (Fig. 2). This time assumption that the diffusion coefficient is independent on the drift field results in a severe overestimation of the gain.

For the purposes of comparison we have repeated the above mentioned analysis calculating the diffusion coefficient as a function of $y_{tot\mathrm{Ge}} = \frac{y_{C\mathrm{Ge}} + y_{E\mathrm{Ge}}}{2}$ [4] rather than as a function of the position-dependent Ge concentration. It turned out that the base transit time was not sensitive to the change, while in the case of the current gain the simplified method yields overestimated values (Fig. 2).

The effect of finite velocity saturation on the base transit time is illustrated in Fig. 3. It is obvious that this effect increases the transit time. On the other hand, the changes of the current gain are almost imperceptible.

Moreover, we have modeled the parameters of a transistor with a box Ge profile and the proposed Gaussian doping profile. All effects mentioned above have been incorporated. A comparison of the normalized base transit times

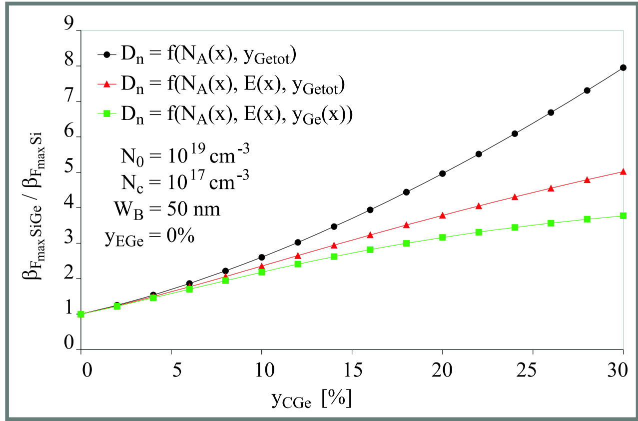

Fig. 2. Normalized current gain versus Ge concentration at the collector edge of the base for cases: A. diffusion coefficient dependent and independent on the drift field; B. diffusion coefficient dependent on constant $y_{totGe} = \frac{y_{CGe}+y_{EGe}}{2}$ or variable Ge concentration along the base.

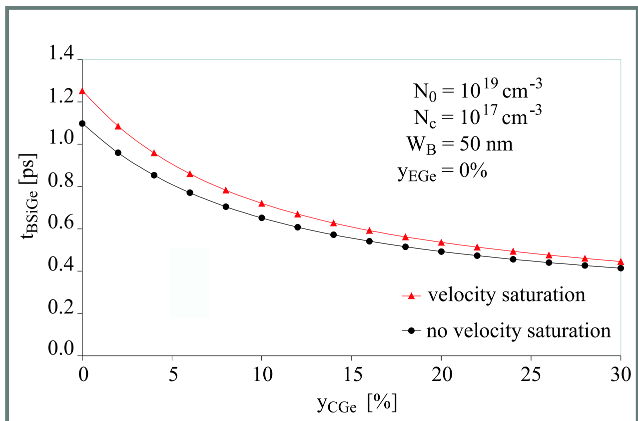

Fig. 3. Base transit time versus Ge concentration at the collector edge.

in the case of box and triangular Ge profiles in the base is show in Fig. 4 as a function of the total Ge concentra-

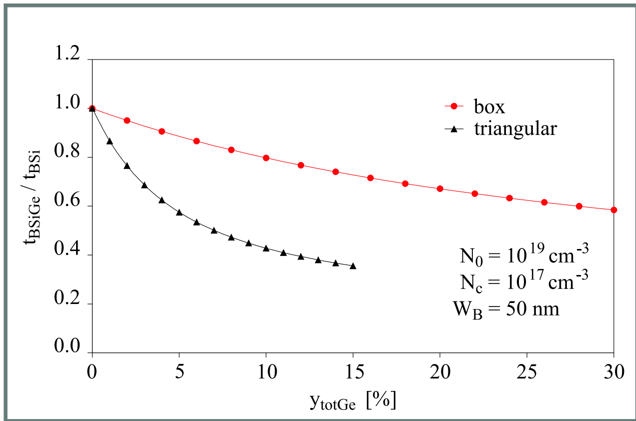

Fig. 4. Normalized base transit time versus total Ge concentration for box and triangular Ge profile.

tion in the base. A similar plot of the normalized current gain is presented in Fig. 5. As seen the reduction of t_B in the box case is not as significant as in the triangular case, however β is much higher in the box case than in the other one (Fig. 5).

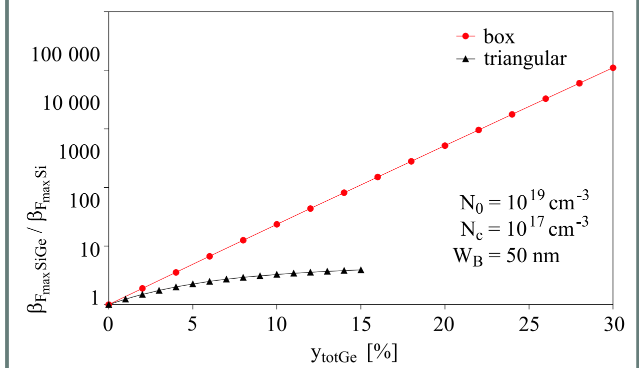

Fig. 5. Normalized current gain versus total Ge concentration for box and triangular Ge profile.

4. Conclusions

The results of numerical modeling of parameters of SiGe-base HBT transistor with the Gaussian base doping profile and different Ge profiles are presented for the first time. The importance of including the dependence of minority carrier diffusion coefficient on the drift field and variable Ge concentration along the base is demonstrated.

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Invited paper

Roadmap for SiC power devices

Mietek Bakowski

Abstract — Silicon carbide (SiC) power devices offer significant benefits of improved efficiency, dynamic performance and reliability of electronic and electric systems. The challenges and prospects of SiC power device development are reviewed considering different device types. A close correlation between an exponential increase of current handling capability during recent five years and improvement in substrate quality is demonstrated. The voltage range of silicon and SiC unipolar and bipolar power devices with respect to the on-state voltage is determined based on device simulation. 4H-SiC unipolar devices are potentially superior to all silicon devices up to 10 kV. 4H-SiC unipolar devices are superior to all SiC bipolar devices up to 8÷9 kV. The low end of SiC unipolar devices is determined to be around 200 V provided substrate resistance is reduced by thinning the substrate down to 100 μm. The influence of reduced channel mobility on the specific on-state resistance of 4H-SiC DMOSFETs and UMOSFETs is shown. It has been demonstrated that 6H-SiC DMOSFETs could be a better choice compared to 4H-SiC MOSFETs in the voltage range below 600 V utilising better channel mobility obtainable so far on 6H-SiC polytype. An impact of super junction (SJ) concept on silicon and SiC MOSFET specific on-resistance limits is demonstrated.

Keywords — SiC power devices, roadmap for, status, development trends, unipolar and bipolar SiC devices, super junction devices, applications, system benefits, current handling capability, simulations.

1. Introduction

Silicon carbide is an example of a so-called wide band gap semiconductor, a material whose electronic and physical properties promise a major qualitative leap in semiconductor device performance. Intense research and development has been going on throughout the last decade in many centres over the world. In particular, activities in Sweden have been at the forefront of development. The beginning of the new century represents the threshold for commercialisation of SiC based devices. A number of companies are announcing the release of products and the number of material producers has multiplied four-fold.

2. Applications of power devices

Emerging WBG (wide band gap) semiconductor devices, of which silicon carbide is currently the most mature, face a well-established market of power electronics practically totally dominated by silicon devices. Silicon carbide power devices have high potential of finding its way into the mainstream applications and of capturing important parts of the market thanks to the specific material properties of SiC that translate into high value added for electronic power systems. Specifically high electric field breakdown in combination with reasonably high electron mobility and high thermal conductivity translate into improved efficiency, dynamic performance and reliability of electronic and electric systems. It is relatively straightforward to envision savings on cooling requirements connected with increased working temperature of the devices well above 125°C typical of silicon power devices as well as reduced noise, size and weight of systems due to greatly increased operating frequency. To overcome both limitations has long been desired in especially high voltage applications above 1 kV where bipolar silicon devices must be used. Such devices are necessarily slow and suffer from high switching losses due to substantial recovery charge that makes them the limiting component in terms of performance of many systems.

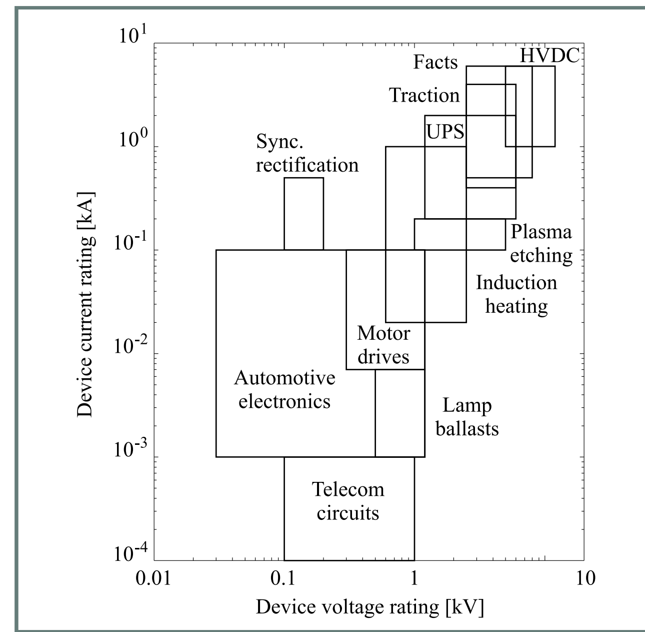

Fig. 1. Current and voltage ratings of power devices used in different applications.

In Fig. 1 applications for power devices are summarised in relation to required current and voltage ratings. In Fig. 2 the same applications are summarised in relation to required device power ratings and operating frequency. Types of silicon power devices used in different applications are shown in the graph.

3. System benefits of WBG semiconductors

In general SiC power devices have compared to Si power devices the advantages of lower on-state voltage drop for

Table 1
System benefits of WBG semiconductors

Device properties	System benefits	Driver
Low on-state voltage Low recovery charge Fast turn-off and turn-on High blocking voltage Higher junction temperature High power density	Higher efficiency Higher frequency Reduced noise Smaller size and weight – reduced value of reactive components – fewer devices stacked in series – smaller size of heat-sink – natural convection – saving costs of forced convection and fans	Power distribution and conditioning HVDC FACTS Motor drives UPS

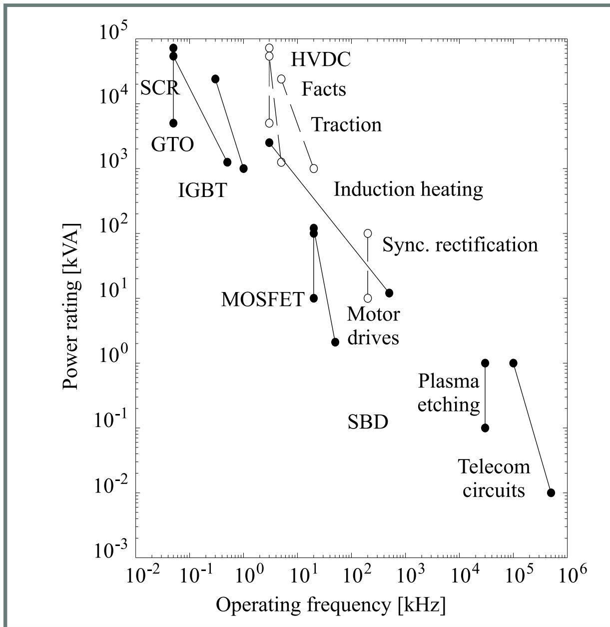

Fig. 2. Device power rating and operation frequency for different applications. The desired operation frequency is shown by empty symbols and dashed lines. The type of silicon power devices used today in different power and frequency ranges is shown as well.

unipolar devices (lower specific on-resistance) as well as excellent dynamic characteristics, high switching speed and low losses for both unipolar and bipolar devices due to extremely low recovery currents. Furthermore, they have theoretical potential of handling 100 times higher power density making possible higher packing density of device chips and reduction of the size of power devices [1–4].

In short SiC devices are an obvious choice in all applications where low R_{on} (alt. low conduction losses), high frequency (alt. low switching losses) and working temperature above 150°C (alt. reduced cooling requirements) lead to significant system benefits.

The predicted benefits of introducing SiC power devices in the electronic power systems are summarised in Table 1.

4. Silicon carbide device development trends

Development of SiC devices in terms of voltage handling capability has been remarkably fast ever since the first commercial material from Cree Research Inc. became available in 1993. High voltage capability has been demonstrated in almost all types of SiC power devices. The progress in terms of voltage blocking capability has been controlled by the availability of low doped thick epitaxial layers. The evolution of blocking voltages follows closely the constant improvements in CVD epitaxial growth of low doped n-type layers and their commercial availability. Schottky barrier diodes have been demonstrated with blocking voltages of 1.75 kV and 3.0 kV (1996 and 1998, Kyoto University and Linköping University, respectively) [5, 6] and 4.9 kV (1999, Purdue University) [7]. PiN diodes were made blocking voltages of 2.0 kV (1993, NASA Lewis Research) [8], 4.5 kV (1995, ACREO (IMC)) [9], 6.2 kV (1999, Cree Research/Kansai Electric Power) [10] and 8.6 kV (1999, Cree Research) [11]. PiN diodes blocking over 4.5 kV have been repeatedly done within ABB/KTH facilities in Kista. JBS diodes blocking 1.8 kV (1998, ABB/ACREO (IMC)/Daimler-Benz) [3] and 3.6 kV (1999, Cree Research/Kansai Electric Power) [12] and 3.7 kV (2000, Hitachi/Kansai Electric Power) [13] have been demonstrated. High voltage MOSFET devices have been made, like 1.4 kV trench UMOSFET (1997, Northrope-Grumman) [14], lateral 2.6 kV implanted DMOSFET (1997, Purdue University) [15] and recently 1.4 kV UMOSFET (1998, Cree Research/Kansai Electric Power) [16] and 1.8 kV DMOSFET (1999, Siemens) [17]. Other unipolar switches include high voltage 1.8 kV vertical JFET (1998 and 2000, respectively, Siemens) [18, 19] and 2.0÷4.5 kV vertical JFETs (2000, Cree Research/Kansai Electric Power) [20]. Also bipolar devices like GTO thyristors with blocking voltage of 1.0 kV (1997, Northrope-Grumman) [21] and 2.6 kV (1999, Cree Research) [22] were demonstrated.

However development of current handling capability has been slow up to now and limited by the quality of the

material and more specifically by the size of the defect free areas on the SiC wafers.

4.1. Material development

The increase in substrate size has been dramatic over the last three years, motivated by the prospect for SiC technology to enter production phase (see Fig. 3). Today both 50 and 75 mm wafers can be purchased and 100 mm wafers

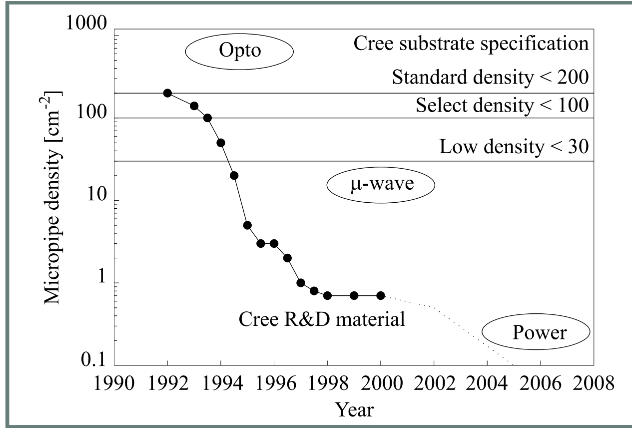

Fig. 3. The evolution of SiC wafer size from Cree Research [24].

have been demonstrated. It is likely that 100 mm wafers will be offered for sale within three years and that even larger substrates are demonstrated during the same period. The introduction of 100 mm or 4 inch substrates can be the turning point for SiC device production since much of the equipment used for processing Si can also be used for SiC. Market introduction of the SiC technology requires in addition to the reasonable wafer size an adequate quality of the semiconductor material. All the SiC power devices require at least one epitaxial layer with controlled doping and thickness to be grown on top of the highly doped substrates. The major limiting factor for the quality of SiC epitaxial films is the substrate material itself. Even if the development of SiC substrates has been successful during the last five to ten years the quality is still extremely poor compared to the substrates of other commercially available semiconductor materials.

Epitaxial layers typically contain a high density of detrimental defects like dislocations (10^5 cm^{-2}), micropipes (100 cm^{-2}) and polytype inclusions (10%), the majority of which propagate from the bulk of the substrate into the epi-layers. In addition, other defects that are generated during epitaxial growth include different growth pits ($10^2 \div 10^4$ cm^{-2}) most likely caused by substrate surface damage introduced during cutting and polishing. Since the defect free areas of the substrates today are relatively small, market factors dictate that only small area devices, like μ-wave frequency MESFETs, are economically feasible to produce. Production of large area power devices requires further significant increase of at least the micropipe free areas on the substrates (see Fig. 4). For this reason

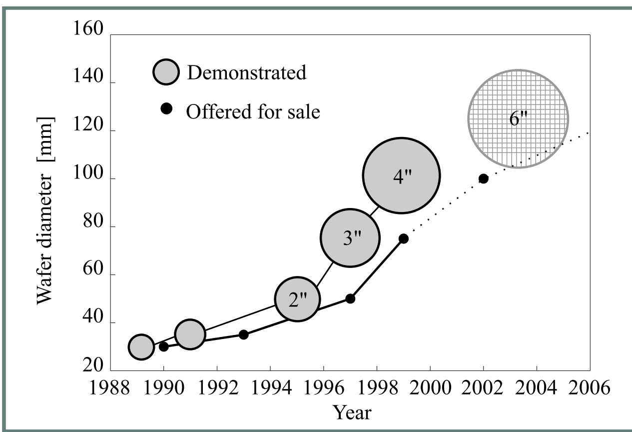

Fig. 4. The evolution of micropipe density in best R & D wafers from Cree Research [24].

multi-chip press-pack and wire-bonded module solutions are being developed and tested [16, 23].

4.2. Current handling capability

All available data point to a close correlation between the yield (measured in terms of static blocking capability) and micropipe density in the substrates. This is demonstrated in Figs. 5 and 6. In Fig. 5 development of the maximum chip

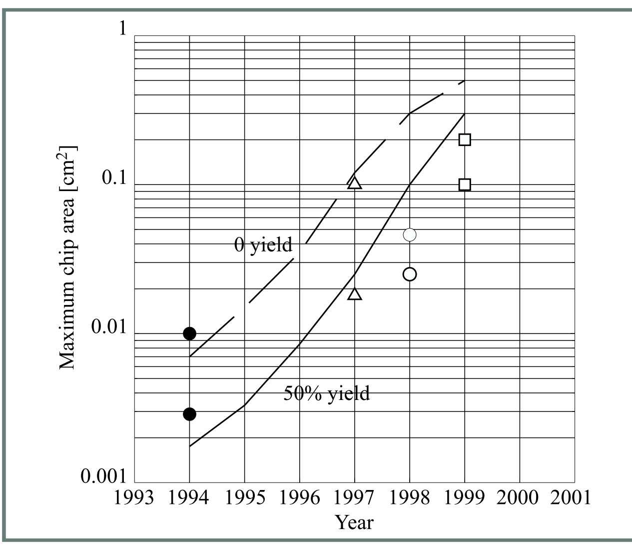

Fig. 5. Evolution of maximum chip area for estimated yield of 50% (solid line) and 0% (dashed line) based on PiN diode data (lines). Also there are shown estimated maximum areas based on SBD data from Purdue University (△) [25], and Siemens (◯) [26], on JBS data from DaimlerChrysler (□) [27], and on JFET data from NASA Lewis Research Center (•) [28].

size in time is shown as determined from the available yield data for PiN rectifiers (lines) and Schottky (SBD) rectifiers (empty symbols). The data by others are used to verify our own data. The lower line (and symbol) corresponds to a yield of 50% and upper line (and symbol) to a 0% yield as determined applying Poisson distribution model to the yield data measured on diodes of different size processed on the same wafers. In Fig. 6 the defect density extracted

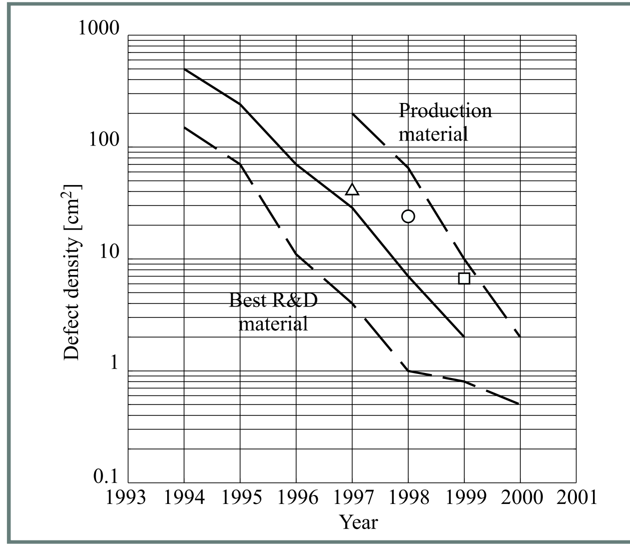

Fig. 6. Defect density extracted from yield data using Poisson model as illustrated in Fig. 7 and micropipe density in Cree Research substrates after ref. [24]. The time scale is that of publication (one year has been added to the wafer manufacturing date).

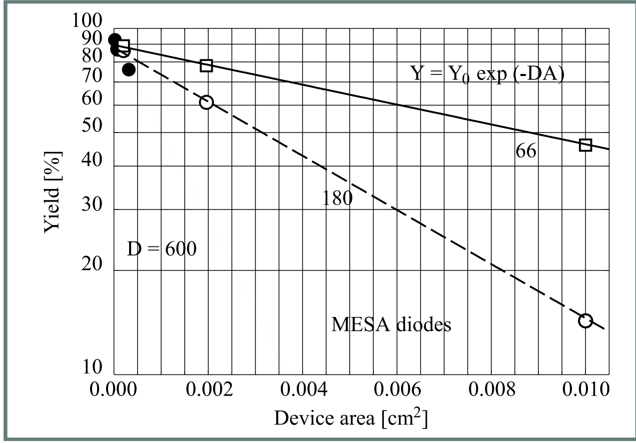

Fig. 7. Extraction of defect density and maximum chip area for a given yield for three different wafers each containing diodes with three different diameters. The Poisson yield model is used as shown in the figure. The diodes were processed 1994, 1995 and 1996, respectively.

using Poisson model from PiN diode data (solid line) and SBD data (empty symbols) is plotted together with micropipe density data published by Cree Research for their best material (lower dashed line) and standard production grade material (upper dashed line) [24]. The time axis for the substrate data was shifted one year forward to account for the fact that it takes about one year from the time the material is made to the time the devices are measured and data presented at a conference. The correlation between the defect density obtained from Poisson model and those from micropipe defect density in substrate material is astonishing. An example of extraction procedure is shown in Fig. 7 where static blocking voltage yield data are plotted for PiN diodes of different size from the same wafer processed 1994, 1995 and 1996 (SiC substrates from Cree Research were produced 1993, 1994 and 1995, respectively). Latest PiN data are based on reference [23]. The data are fitted with a function $Y = Y_0 \exp(-D \cdot A)$ where D is defect density and A is device area. The value (100%-Y_0) is a measure of „dead" area. Usually the area close to the edge of the wafer has much higher concentration of defects than the rest of the wafer. Devices in this area have not been excluded beforehand when calculating the yield. The percentages of dead area and the fatal defect densities for the wafers in Fig. 7 are 7% and 600 cm^{-2}, 12% and 180 cm^{-2} and 10% and 66 cm^{-2}, respectively. All the devices were processed on the Cree Research substrates. The epitaxial layers were grown at different sites. At Linköping University (PiNs), at Siemens (Siemens SBDs), at Nasa Lewis (NASA Lewis JFETs) and at Cree Research (Purdue Universities SBDs and DaimlerChrysler JBS diodes).

Micropipes appear to be the dominant single type of defect when it comes to yield based on the static blocking capability. As the quality of the material and density of the micropipes decreases it becomes easier to observe and distinguish the influence of other types of defects on the electrical performance of the devices. The influence of the defects and lateral non-uniformities normally increases with the increasing area of the device. The awareness of the role played by other types of defects and imperfections increases as more and larger size devices are made and is reflected in the rapidly increasing number of papers on reliability related issues [29–36].

Recently, other defects present in SiC material like screw dislocations have also been given extra attention [37, 38]. These defects are suspected to influence dynamic performance of the devices and were shown to be responsible for soft breakdown phenomena in device characteristics. The role of these defects is, however, not clear as yet. Their effect on the device performance is clearly not as detrimental as that of micropipes. The final judgement has to wait since long time stability data under both static (DC) and switching conditions (frequency tests) are still missing.

A lot of the fundamental questions related to stability and reliability of SiC devices remain at present unanswered. These issues related to material bulk and surface properties and to surface passivation and gate insulation in MOSFETs will be crucial during the coming years for the success of wide band gap semiconductor materials and high temperature electronics. Issues of passivation and insulation are also starting to attract more and more attention [39, 40]. It is a rapidly expanding field of research. Oxide/nitride/oxide stacks and also oxides subjected to nitridation have been shown to have improved dielectric strength [41, 42] however oxide is still a base of this gate dielectric system determining interface properties. Also monocrystalline AlN was suggested and tried [43, 44] but its deposition or MBE growth requires high temperatures ($>$ 1000°C). Reliability issues are expected to dominate the research field of SiC (and later also of GaN) at the present stage of technology and device development and for many years to come.

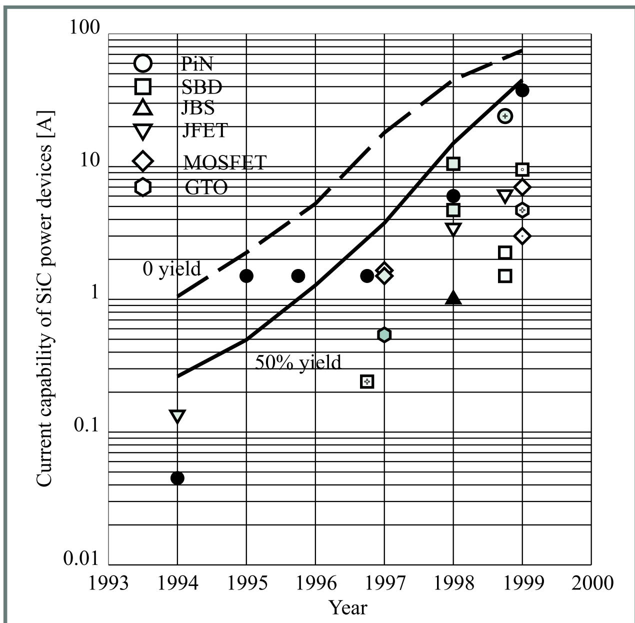

Fig. 8. Evolution of current handling capability in SiC power devices. The best published data from different manufacturers are summarised in the figure according to publication date.

In Fig. 8 most of the published results from different device types are summarised in terms of current handling capability assuming a current density of 150 A/cm^2 for all the devices. The line of 50% yield and 0% yield is based on the data from HV PiN diode development using a Poisson yield distribution fit to experimental data over the years. All other data are from other manufacturers. Data show a dramatic (exponential) progress in current handling capability taking place in the most recent couple of years. This means that we can expect current handling capability to reach levels adequate for most practical applications in a few years.

4.3. Status of SiC power devices

A summary of the status of development of SiC power devices is given below by listing devices in the order of decreasing maturity and specifying optimal voltage range for each device.

1. Schottky barrier rectifiers (SBDs), voltage range 0.2 to 2.5 kV, higher leakage current compared to PiN and JBS at higher temperatures. SBDs with blocking voltages up to 4.9 kV have been demonstrated.

2. PiN rectifiers, voltage range above 4.5 kV, high on-state voltage due to WBG, voltages in excess of 10 kV require significant improvement of carrier lifetime. PiN rectifiers with blocking voltages up to 8.6 kV have been demonstrated.

3. JBS diodes, voltage range 0.2 to 10 kV, a device of choice for working temperatures above 150°C, due to lower leakage current compared to SBDs. JBS rectifiers with blocking voltages up to 3.9 kV have been demonstrated.

4. Vertical JFETs, voltage range 0.2 to 10 kV, normally-on devices, can be used in cascode configurations with low voltage Si MOSFET to obtain insulated gate control and normally-off function. Vertical JFETs with blocking voltages up to 1.8 kV have been demonstrated.

5. GTO thyristors, voltage range 8 to 40 kV, robust devices for high temperature, high radiation environments, can be operated in cascade configuration with low voltage Si/SiC MOSFET for insulated gate control. GTOs with blocking voltages up to 2.6 kV have been demonstrated.

6. MOSFETs, voltage range 0.2 to 8 kV. SiC MOSFETs suffer from low channel mobility values. However even though this lowers their performance compared to the ideal material limit they are already today superior in performance compared to Si devices for voltages over 0.5 kV. MOSFETs with blocking voltages up to 2.6 kV have been demonstrated. The trend of continuous improvements in channel mobility and device performance by technology development and by novel designs is continuing.

5. Power devices. Choices and prospects

5.1. Unipolar versus bipolar Si and SiC devices

Introduction of SiC power devices will change with time the scene of preferred semiconductor devices used in different applications. It is important for the system designer and semiconductor device engineer alike to be able to understand the potential and limitations of different devices as well predict the pace of their development. In Fig. 9 the ideal performance limits of unipolar and bipolar Si and SiC power devices are shown in the domain of on-state voltage and blocking voltage. In the Si case the on-state voltage curves based on the actual device data are shown for fast PiN rectifiers, MOSFETs, IGBTs and GTO thyristors together with an ideal limit equal to the resistivity of the uniformly doped drift region of unipolar device only. In the SiC case the on-state voltage curves based on device simulations are shown for DMOS and UMOS transistors, vertical JFETs, Schottky barrier rectifiers, PiN rectifiers and IGBTs. The SiC device data represent the ideal limit for different types of devices. The device lateral design uses high-density layout with small cell pitch equal to 3 μm, 5 μm and 10 μm for UMOSFET, VJFET and DMOSFET, respectively. The ideal bulk mobility is assumed for all the devices in both the channel and the drift region. The contribution from substrate resistance is included and minimised assuming only 100 μm thick substrate with a doping of $1 \cdot 10^{19}$ cm^{-3}. The ideal limit for 4H-SiC based on the resistivity of the uniformly doped unipolar device drift region only is shown including the influence of the substrate

Table 2
Challenges in development of SiC PiN rectifiers

		Primary	Secondary	Driver
Improvement	Continuous	Increase current handling capability	Reduce on-state voltage Reduce contact resistance Reduce substrate resistivity	Power distribution HV applications
	Breakthrough	Improve stability Improve performance at high current densities Adequate passivation High carrier lifetime material $(2 \div 10\,\mu s)$	Substrate thinning	Low V_{on} Reliability

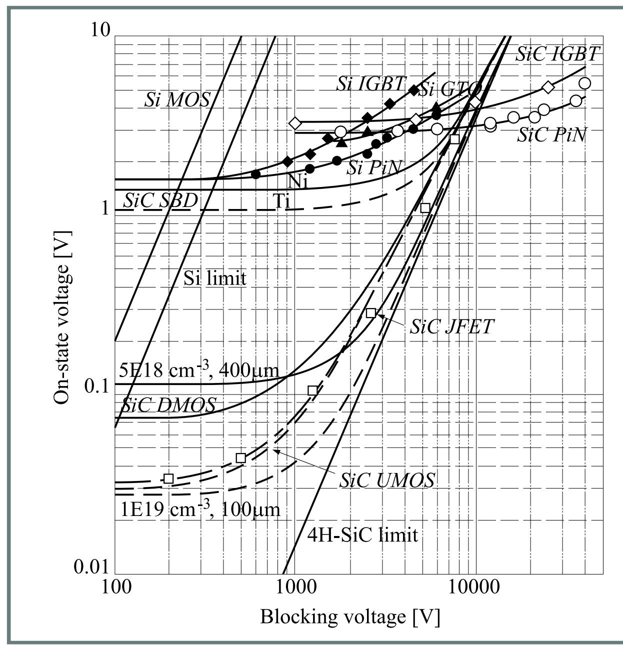

Fig. 9. On-state voltage of Si (actual) and SiC (simulated) power devices as a function of blocking voltage.

resistance in the case of thick and low doped and thin and higher doped substrate. The 400 μm thick substrate with a doping of $5 \cdot 10^{18}$ cm^{-3} represents substrates available today and the 100 μm thick substrate with a doping of $1 \cdot 10^{19}$ cm^{-3} illustrates the improvement possible by using thinner and higher doped substrates. In the case of very high voltage SiC bipolar devices the single most important parameter is free carrier lifetime. The curves for SiC PiN rectifiers and SiC IGBTs shown in the diagram are based on simulations using carrier lifetime of 5 μs in the range from 1 kV to 40 kV. A carrier lifetime of 2 μs results in on-state values not much worse than shown up to the blocking voltage of about 6 kV and 15 kV for IGBTs and PiN rectifiers, respectively. On the other hand, IGBT and PiN devices with blocking voltage in excess of 25 kV and 30 kV, respectively, require a lifetime of 10 μs in order not to deviate more than 0.5 V from the drawn curves.

Several important conclusions can be drawn from the data presented in Fig. 9. First of all the application area of unipolar devices is greatly expanded. The SiC unipolar devices are superior to silicon power devices with respect to the on-state voltage in the voltage range up to at least 10 kV. Considering superiority of unipolar devices over bipolar in terms of dynamic behaviour and switching losses it means that SiC unipolar devices have the potential of replacing silicon bipolar devices in all their present applications (assuming the same current and voltage ratings). Secondly, the application area of SiC bipolar devices starts above blocking voltage of 8–10 kV which is above the Si power devices with highest ratings available today. The SiC bipolar devices are superior to the Si bipolar devices with respect to the switching losses due to the low plasma level and low accumulated charge in the device during conduction. This is caused by 10 times smaller thickness of the n-base and to the lower minimum lifetime required for efficient conductivity modulation. It can also be seen that above 4.5 kV SiC PiN rectifiers are superior to Si PiN rectifiers also with respect to the on-state voltage. The same applies to the SiC IGBTs with voltage rating above 2.5 kV as compared to the Si IGBTs. In the case of Schottky barrier devices there is hardly any gain other than the cost of the epitaxy to differentiate between different voltage designs for voltages lower than about 1 kV. Finally it can also be seen that in order to use fully potential of SiC unipolar devices also at the low voltage end it is necessary to lower the resistance contribution of the substrate material. With standard substrate material available today the practical lower limit of the design voltage is around 1 kV. Thinning of the SiC substrate would expand that limit down to about 200 V. The idealised evolution in time between different power devices and materials with respect to the voltage range is pictured in Fig. 10; assuming constant continued improvement in material quality and disregarding cost.

Table 2 summarises challenges in the area of SiC PiN rectifiers.

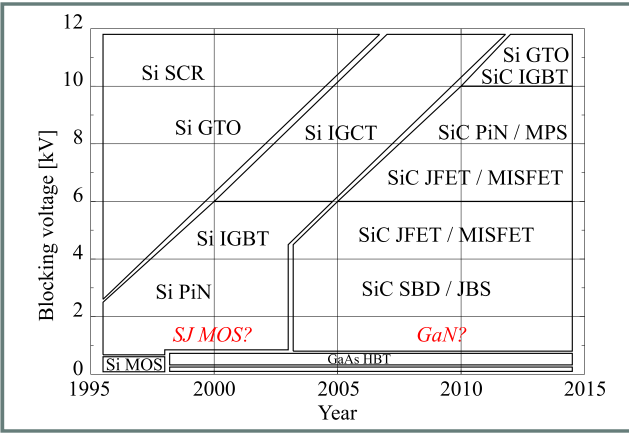

Fig. 10. Preferred device type and semiconductor material based on the data in Fig. 9.

5.2. Unipolar devices

In Fig. 11 a summary of the best published specific on-resistance values from different unipolar devices is given to substantiate what was said before. Also shown in the diagram is the theoretical material limit for on-resistance in Si and SiC. The newest development in the field of MOSFET on-resistance so called Cool MOS (Siemens) is shown. The principle for the breakthrough in reducing on-resistance in MOSFETs is called Super Junction design. It means that the drift region is divided into alternating narrow layers of n- and p-type parallel to the current flow. The doping of the n- and p-type layers must be controlled in such a way that the n- and p-type regions are depleted under

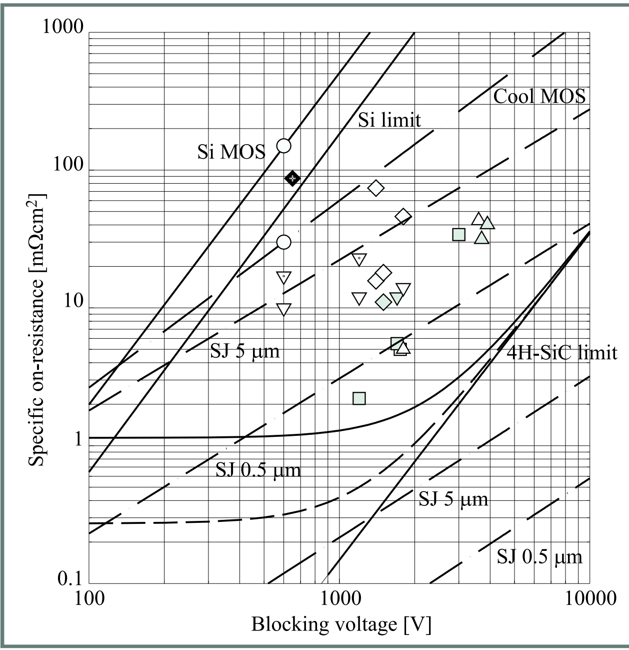

Fig. 11. Specific on-resistance of unipolar Si and SiC devices. The meaning of symbols is like in Fig. 8. The diamond with cross is a lateral MOSFET. The lines for SJ devices are shown for 5 μm and 0.5 μm wide regions (10 μm and 1 μm pitch, respectively).

blocking condition and that the charge in n- and p-type layers due to doping is equal. The donator and acceptor charges neutralise each other. In this way the doping of the n-type layers constituting new channels for current during conduction can be increased without influencing negatively the blocking voltage. The higher is n-type doping the larger is the reduction of the on resistance. However that means that n-type regions must be made smaller and smaller in order to be depleted under blocking conditions. If not the increase in electric field will cause the premature breakdown. The SJ principle removes the limitation of having to lower drift region doping with increase in blocking voltage and the resulting quadratic dependence of the on-resistance on the design voltage. The impact of SJ design with different width of super junction regions on both Si and SiC MOSFET performance is shown by the stretched lines (simulated). The technology for realisation of the depicted benefits is not easy or cheap. Today's Cool MOS technology is rather coarse and could be depicted as 10–20 μm [45–47]. The point is that similar concept can be realised in the case of SiC devices. Another point is that SiC MOSFETs with today's poor channel mobility values are already superior to the best silicon devices.

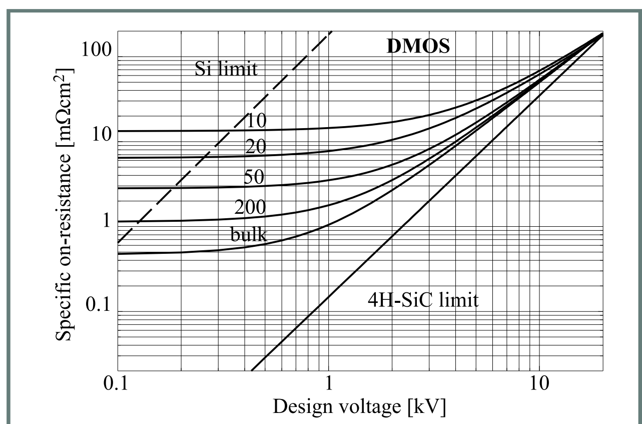

Fig. 12. Influence of the channel mobility on specific on-resistance of 4H-SiC DMOSFETs.

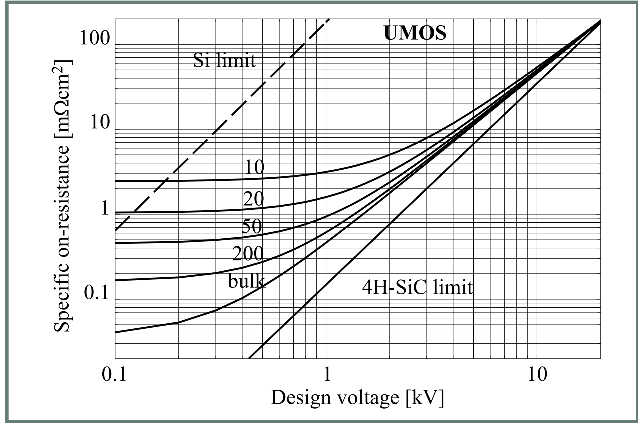

Fig. 13. Influence of the channel mobility on specific on-resistance of 4H-SiC UMOSFETs.

In Figs. 12 and 13 the influence of the channel resistance on the specific resistance of the 4H-SiC DMOSFETs and UMOSFETs is shown, respectively, in the voltage range from 100 V to 20 kV. The simulated structures are those used in Fig. 9 with cell pitch of 10 μm and 3 μm for DMOSFET and UMOSFET, respectively. The channel length is about 1 μm. The voltage design of structures is adjusted by varying resistivity and thickness of the drift region except for the structures for voltages lower than 1 kV. In those structures also the doping in the p-base was reduced improving the channel resistance for the structures with bulk channel mobility. The value of the channel mobility in the case of the DMOSFET is the average mobility due to the gaussian p-well doping distribution used in the simulations. It can be seen from simulations that channel mobility of $100 \div 200$ cm^2/Vsec can be regarded as target channel mobility for acceptable devices provided it is not coupled to interface conditions giving rise to operational instabilities in threshold voltage and sub-threshold characteristics.

The SiC/SiO_2 interface properties on 4H SiC material are much poorer compared to 6H SiC polytype [48, 49]. These is a reason for much better channel mobility values reported for MOSFETs made on 6H-SiC compared to 4H-SiC. The 6H-SiC material may then be a better choice for reasonably low voltage MOSFETs compared to the 4H-SiC alternative regardless of much poorer bulk mobility value of 6H-SiC influencing the contribution of the drift region. The results of simulations performed on 4H-SiC and 6H-SiC DMOSFET and UMOSFET structures in order to define the voltage limit for such an approach are summarised in Figs. 14 and 15. The simulated structures are the same as those used to obtain data in Figs. 12 and 13. As can be seen from the presented data, it may be advantageous to use the 6H-SiC material for devices below about 0.6 kV. At design voltage of 1 kV, however, the specific resistance of 6H-SiC devices becomes higher than the specific resistance of 4H-SiC devices regardless of the value of channel mobility. This is due to the fact that drift region contribution to the specific resistance is dominating for devices with design voltages larger than about 600 V [50].

Challenges in development of SiC MOSFETs are summarised in Table 3 and challenges related to development of SiC Schottky rectifiers (SBD, JBS and MPS (merged Schottky and PiN rectifiers)) are summarised in Table 4.

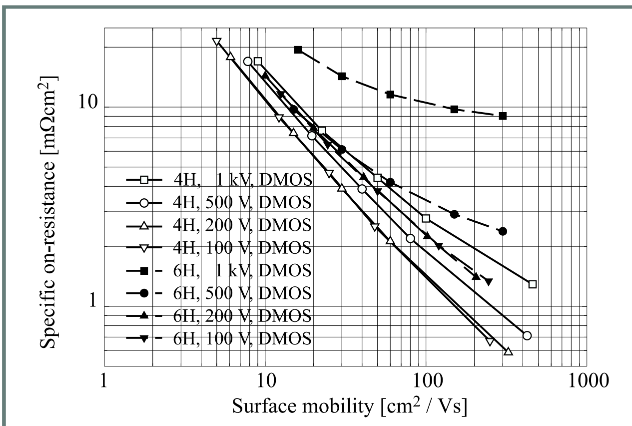

Fig. 14. Specific on-resistance of 4H-SiC and 6H-SiC DMOSFETs as a function of the channel mobility.

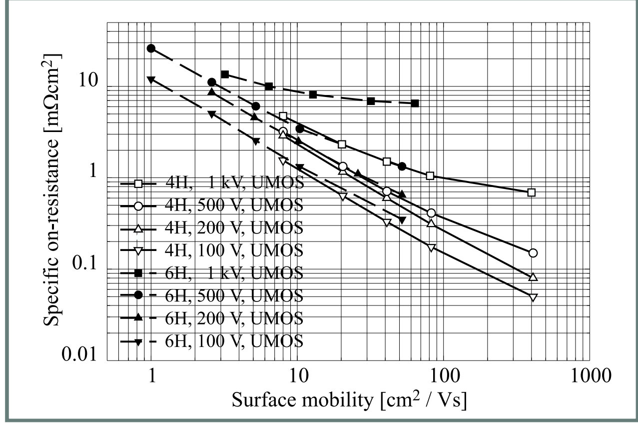

Fig. 15. Specific on-resistance of 4H-SiC and 6H-SiC UMOSFETs as a function of the channel mobility.

6. Silicon carbide electronics

6.1. Device perspective

Challenges in SiC electronics from the device perspective are summarised in Table 5.

6.2. Total system perspective

The appearance of the SiC power devices on the market will bring about and accelerate new developments in the areas of packaging, passive components (capacitors), circuit and system design as well as improvements in construction and operation of electric motors. It will not be in general most effective just to substitute SiC devices for silicon ones in existing circuits. It will be necessary to adopt new solutions in order to utilize full potential of increased operational frequency, working temperature and reduced size of active devices. Advent of SiC power devices will enforce thinking in terms of the total power system including electrical, mechanical and electromechanical components. This will provide incentive towards increased integration of electronics and electromagnetic and mechanical parts of the system. Also electrical motors will have to be developed in order to facilitate integration and utilisation of the benefits of high frequency operation.

The necessity of new solutions is most apparent and urgent in the area of packaging. Especially considering that the modular solution utilising parallel connection of small chips as opposed to large area single devices will be the most efficient way to increase current handling capability for a long time. This actualises necessity of high temperature, high frequency and high packing density module technology. Challenges in packaging are summarised in Table 6.

Table 3
Challenges in development of SiC MOSFETs

		Primary	Secondary	Driver
Improvement	Continuous	Improve channel mobility Improve interface quality Increase current handling capability	Reduce contact resistance Reduce resistivity of implanted layers Reduce substrate resistivity	Low R_{on} Feasibility
	Breakthrough	New gate dielectrics Channel engineering – crystallographic orientation (ex. a-plane) – polytype (ex. 15R) – buried channel etc. (depletion type)	Substrate thinning	Low R_{on} Reliability

Table 4
Challenges in development of SiC Schottky (SBD, JBS and MPS) rectifiers

		Primary	Secondary	Driver
Improvement	Continuous	Low leakage junction termination Increase current handling capability	Reduce on-state voltage Reduce contact resistance Reduce substrate resistivity	Low R_{on} Low leakage currents
	Breakthrough	High barrier materials for $T > 150°$ C Adequate passivation	Substrate thinning	Reliability

Table 5
Challenges in SiC electronics

		Primary	Secondary	Driver
Improvement	Continuous	Wafer quality and size MISFET technology – improve channel mobility – improve interface quality Niche application Increase current handling capability	Contact resistance Resistivity of implanted layers Substrate resistivity	Material supply
	Breakthrough	New gate dielectrics Adequate passivation Novel structures Implantation damage Packaging for HT New material suppliers	Carrier lifetime	Speed Losses High T_j System benefits

Table 6
Challenges in packaging for SiC devices

		Primary	Secondary	Driver
Improvement	Continuous	Lower R & L	High reliability die attach High reliability bonding Low stress compounds	Surface mount Automotive
	Breakthrough	Reduce pkg/chip footprint Better voltage isolation Better CTE matching Diamond heat spreaders Flip-chip mounting EMI immunity	High T_g plastics	Surface mount Reliability

7. Conclusions

Commercialisation of SiC power devices is facing a lot of extremely difficult challenges. Especially, reliability issues constitute the biggest challenge in the coming years.
It is however, difficult to see anything that could prevent SiC power devices from entering the electronic market in the first decade of this century considering:

a) the tremendous benefits offered to the electronic systems,

b) the momentum gained by the development activities involving many people in different countries,

c) the spectacular results in device performance obtained so far,

d) the dramatic increase in the ratings of test devices during the recent years.

This last point is a reassuring indication of the continued positive development.

Acknowledgments

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Invited paper

Advanced compact modeling of the deep submicron technologies

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Abstract — The technology of CMOS large-scale integrated circuits (LSI's) achieved remarkable advances over last 25 year and the progress is expected to continue well into the next century. The progress has been driven by the downsizing of the active devices such as MOSFETs. Approaching these dimensions, MOSFET characteristics cannot be accurately predicted using classical modeling methods currently used in the most common MOSFET models such as BSIM, MM9 etc, without introducing large number of empirical parameters. Various physical effects that needed to be considered while modeling UDSM devices: quantization of the inversion layer, mobility degradation, carrier velocity saturation and overshoot, poly-depletion effects, bias dependent source/drain resistances and capacitances, vertical and lateral doping profiles, etc. In this paper, we will discuss the progress in the CMOS technology and the anticipated difficulties of the sub-0.25 µm LSI downsizing. Subsequently, basic MOSFET modeling methodologies that are more appropriate for UDSM MOSFETs will be presented as well. The advances in compact MOSFET devices will be illustrated using application examples of the EPFL EKV model.

Keywords — ultra deep submicron (UDSM) technology, compact modeling, EKV MOS transistor model, MOSFET, matching, low power and RF applications.

1. The ultra deep submicron CMOS technology developments

Over the last 25 years, technology of CMOS large-scale integrated circuits (LSI's) has achieved advances stage. However, even before the downsizing of the LSI devices reaches its fundamental limits this process is expected to encounter severe technological and economic problems when the minimum features of the active devices are being shifted to dimensions below sub-quarter micron, the so-called ultra deep submicron (UDSM) technology. The downsizing allowed minimizing geometry of transistor. The number of the transistors in a chip increases and the functionality, switching and operation speed of the LSI's circuit is improved. Indeed, these continuous technology improvements are correctly predicted according the Moore's law [1]. Moreover, at the research level, many institutions have already reported successful fabrication of sub-0.1 µm MOSFET devices operation at room temperature. As indicated in Fig. 1, for most aggressively scaled DRAM, the integration scale will reach 256 Gbit by the year 2010. There seems to be no physical limitation for feature size down to 25 nm. Furthermore, there are no apparent fundamental limits for Si, in terms of tunneling and other quantum mechanical effects

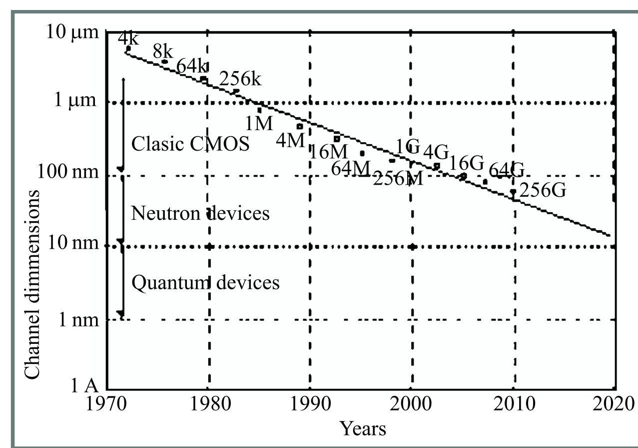

Fig. 1. Trends of the MOSFET gate length scaling in advanced LSI technologies.

for the features size. The challenges to surmount these problems encompass almost all aspects of the device physics, processing, and integration including interconnection and patterning technologies. In the long term, as the semiconductor feature size reaches the atomic limit, alternative means for computation will be needed to further increase the information throughput.

The great success has been achieved with the scaling methods in miniaturizing MOSFETs down to gate lengths of 0.18 µm at the LSI product level and 0.01 µm at the research level, respectively. However, the actual scaling of the parameters has been different from that originally proposed [3] and is shown in Table 1. The major difference is the supply voltage reduction. The supply voltage was not reduced in the early stage of the LSI generation in order to keep a compatibility with the supply voltage of conventional systems and to obtain higher operation speed at higher electric fields. The supply voltage started to decrease at the level of 0.5 µm CMOS processes because the electric field across the gate oxide would have exceeded value of 4 MV/cm, which has been regarded as the maximum limitation in terms of time-dependent dielectric breakdown and hot-carrier induced degeneration for short channel transistors, generally speaking reliability issues of the MOSFET devices. Now, however, it is not easy to reduce supply voltage because of the difficulties in reducing the threshold voltage of the MOSFET. Too small threshold voltage leads to significant large subthreshold leakage current and forcing designers to design IC operating in subthreshold (moderate inversion) regime. The supply voltage higher then expec-

Table 1
Main EKV v2.6 intrinsic model parameters for first and second order effects

Name	Description	Default	Unit
COX	Gate oxide capacitance	0.7E-3	F/m^2
XJ	Junction depth	0.1E-6	m
VTO	Nominal threshold voltage	0.5	V
GAMMA	Body effect factor	1.0	V$^{1/2}$
PHI	Bulk Fermi potential (2)	0.7	V
KP	Transconductance parameter	50E-6	A/V^2
E0	Mobility reduction coefficient	1E12	V/m
UCRIT	Longitudinal critical field	2E6	V/m
DL	Channel length correction	0.0	m
DW	Channel width correction	0.0	M
LAMBDA	Depletion length correction	0.5	-
LETA	Short channel effect coefficient	0.1	-
WETA	Narrow channel effect coefficient	0.1	-
Q0	RSCE peak charge density	0.0	A s / m^2
LK	RSCE characteristic length	0.3E-6	m
IBA	First impact ionization coefficient	0.0	1/m
IBB	Second impact ionization coefficient	3E8	V/m
IBN	Saturation voltage factor for impact ionization	1.0	-

ted form the original scaling is one of the reasons for the increased distributed power.

An increase of the number of transistors in a chip by more than factor of K^2 is another reason for the power increase. In fact, the transistor size decreased by a factor of 0.7 while the transistor area decreased by factor of 0.5 for every generation. Present complex digital designs cannot wait for the downscaling and thus the actual chip size increased by a factor of four, more than predicted by standard scaling rules. Introducing new technologies such as multilayer interconnections, double polysilicon and further complicated cell structures for the memories partially solves the problem of insufficient IC area.

Recent progress in the CMOS scaling has been achieved using improved DUV lithography tools. Originally, targeted at the 0.35 µm devices, these tools were successfully introduced at 0.25 µm level and are being used in the current 0.18 µm generation. The use of these tools is projected at least for 0.15 µm devices. Further progress is required to adapt popular reticle enhancement technique (RETs), proximity correction and phase shift mask (OPC/PSM) to obtain improved packaging densities. ¿From the extrapolation of traditional scaling, UDSM devices are expected to have excellent drive current and the projected performance suggests circuits operating at frequencies up to 10 GHz. On the other hand, one should remember that there are serious technological and economic limitations of further, accelerated improvements of the standard CMOS technologies and the transistor performance could be, to some extent, compromised. In aggressively sized technologies, oxide scaling leads to rapidly increased gate currents, regardless of the oxide quality. Further improvements in the reduction of the gate tunneling currents require the use of alternative gate dielectric materials. High-k materials are good candidates to replace standard gate oxides. Similarly, potential solutions (e.g. low energy implantation) for advanced source/drain extension engineering, which would approach the physical limit of ultra-shallow but low-resistance junctions, have been discussed in the literature. Table 2 lists scaling problems of the advanced LSI devices and possible technology and architecture solutions.

2. Challenges of the compact modeling

As previously mentioned, in aggressively scaled UDSM technologies, the gate oxide thickness is approaching the inversion layer thickness resulting in high fields at the silicon surface. These high electric fields at the surface cause various physical effects such as quantization of accumulation/inversion layers (QM effect), carrier saturation velocity and velocity overshoot that must be taken into account while developing UDSM transistor model. Other physical effects, which are additional to the short channel effects are polysilicon gate depletion effect, impact of nonuniform channel doping profile on threshold voltage, bias dependent source/drain resistances and capacitances, drain induced barrier lowering (DIBL) are relevant to UDSM modeling, as well.

First of all, the regional approach, which is the most frequently used that combines different equations for different regions of device operation and then piece them together by smoothing function to avoid eventual discontinuities. There are a number of advantages. Firstly, it allows for a simple implementation of the short channel effects using empirical relations. Then it offers relatively fast computation time, which is not always true for other models like BSIM3. Nevertheless, it has some disadvantages such as ignoring the

Table 2
Parameter scaling

Ideal Scaling Rules		Limiting factor	Example values
Parameter	Scale		
Gate length (L_g)	$1/K$	Lithography	0.18 μm
Gate width (W_g)	$1/K$	Lithography	
Gate area (A_g)	$1/K^2$	Lithography	
Oxide thickness (t_{ox})	$1/K$	Defects, direct tunneling	5 nm
Gate capacitance ($C_{ox} \sim A_g/t_{ox}$)	$1/K$		
Gate charge ($Q_g \sim C_{ox}V$)	$1/K^2$		
Propagation delay (t_{pd})			20 ps
Clock frequency ($f \sim 1/t_{pd}$)	K	Power consumption, circuit speed	600 MHz
Channel doping (N_{sub})	K	Junction leakage current	10^{18}cm^3
Junction depth (x_j)	$1/K$	Sheet resistance	0.04 μm
Threshold voltage (V_{th})	$1/K$	Off leakage current	0.4 V
Supply voltage (V_{dd})	$1/K$	Lower V_{th}, circuit speed	2.7 V
Number of transistors (n)	K^2	Power consumption, Circuit speed	3-22 M
Chip size ($\sim nA_g$)	1	Yield	3 cm^2
Power ($1/2fnCV^2$)	1	Heat generation	10 W

inversion layer thickness and consequently the quantization of the inversion layer. This leads to wrong deduction of the non-physical gate oxide thickness which in turn results in inaccurate capacitance simulations. The model scalability over full range of available device geometries (W, width/L, length) is rarely possible without so-called parameter binning. The binning is artificially introduced into the model structure and usually generated discontinuities across the boundaries. Most common way of including L and W dependence on a parameter P is:

$$P = P_0 + \frac{P_1}{L} + \frac{P_2}{W}$$

assuming that the model parameters are inversely proportional to L and W. However, a better binning scheme have been proposed in [4]:

$$P = P_0 + P_1\left[\frac{1}{L} - \frac{1}{L_{ref}}\right] + P_2\left[\frac{1}{W} - \frac{1}{W_{ref}}\right] + \\ + P_3\left[\frac{1}{L} - \frac{1}{L_{ref}}\right] \cdot \left[\frac{1}{W} - \frac{1}{W_{ref}}\right],$$

where L_{ref} and W_{ref} are large reference device length and width, respectively.

To model UDSM technology processes, more and more parameters are introduced into models based on the regional approach. The increased number of adjustable parameters complicated the parameter extraction process and model usage.

Most of above mentioned shortcomings of the regional based models are solved using surface potential approach. The full operation range of the MOSFET device from weak inversion through moderate to strong inversion is described in a physical and continuous way. Artificial smoothing functions and parameter binning are not necessary. This physical description of the MOSFET characteristics is also most accurate because gate bias dependence of the surface potential is taken into account in the continuous manner. Unfortunately, the biggest disadvantage is that the surface potential needs to be solved at each bias point interactively due to the implicit nature of the bias dependence of the surface potential. Thus, the drawback of this approach is computation time because of the iteration procedure.

The third approach is the hybrid approach, which combines regional and surface based methods to take advantages of both. The hybrid methodology allows the incorporation of all the essential physics of scaled UDSM MOSFET devices such as short channel and narrow width effects, reverse short channel effect (RSCE), bias dependent source/drain resistances, and channel length modulation (CLM). Successful modeling of UDSM devices with channel length of 0.1 μm has been reported.

Growing complexity of the most commonly used compact models (including recent versions of BSIM [5], MM9 [6] and EKV [7]) can be clearly visible in Fig. 2, which shows also the increase of the number of the intrinsic DC parameters. This figure indicated that models are becoming more and more empirical rather than physical in the their description.

3. The EPFL EKV MOSFET model

A detailed description of the EKV v2.6 model formulation can be found in [7–10]; for reference some basic model equations are presented here. One of the main features of the EKV model is the continuity of the large- and small-signal characteristics and its derivatives from weak through moderate to strong inversion. The model accounts for many of the important second order effects, by using only a small set of the intrinsic parameters (see Table 3), most of which have similar meanings as in well-known Spice models.

Table 3
Scaling problems and possible technology solutions

Scaling problem	Solution	Technology	Architecture
Hot electrons degenerate gate oxide and reduce device reliability	Reduction of the high electric potential drops in drain region	Additional lightly doped drain (LDD) ion implantation	Gate Source Drain LDD Bulk
Subsequent increase of the channel doping increase S/D capacitancs	Decuppling of both parameters thru additional vertical implantation in the substrate	The retrogate well using additional implantation in the substrate	Gate Source Drain Retrograde Bulk
Parasitic leakage currents in the substrate (punch through). The potential barrier at S/D junction is reduced by high potential (DIBL)	Higher doping concentration increases S/D potential barrier	Introduction of the pocked/halo implantation step	Gate Source Drain Pocket / halo Bulk
Complex and difficult to control implantation steps introduces large variations of the process related device parameters	Substitution of the ion implantation by well controlled thin layer deposition	Improved MBE and/or CVD process steps	Gate Source Drain Ground plate Bulk
Bulk MOSFET are difficult to scale because of very complex implantation profiles	Substitution of the classic pn-junction by a insulator barrier	Bulk Si wafers are replaced by SOI wafers with buried oxide	Gate Source Drain Burried oxide SOI
Limit of the optical photolithography (alternative lithography systems are not ready)	Introduction of the 3D planar processes (Double Gate MOST)	Buried Si-SiO_2 interface as additional channel region	Gate Source Drain Gate SOI
Lithography of the planar structures are not more possible (constant channel length)	Lithography independent channel scaling using thin atomic layers	Vertical Double Gates are defined channel by thin atomic layers	Drain Gate Gate Source SOI
Classic MOST are not scalable. MOST operation is dominated by quantum effects	New quantum level devices (i.e. based on the tunnel barrier)	Multi tunnel junction (MTJ) technologies	Drain Gate Gate Source SOI
Atom level scaling (?)	Optimum of the Si technology is reached	Additional improvements of the IC performance are possible only on an algorithmic level.	

Referring the gate, source and drain voltages, V_G, V_S, and V_D respectively, to the local substrate preserves the intrinsic device symmetry. The model uses a threshold voltage VTO corresponding to the gate voltage such that the inversion charge forming the channel is zero in equilibrium ($V_D = 0$ and $V_S = 0$). A pinch-off voltage V_P corresponds to the value of the channel potential for which the inversion charge becomes zero in a non-equilibrium situation (Fig. 3). The pinch-off voltage is directly related to the gate voltage:

$$V_P = V_G' - PHI - \gamma' \left[\sqrt{V_G + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2} \right], \qquad (1)$$

$$V_G = V_G' - VTO - \Delta V_{RSCE} + PHI + GAMMA\,\sqrt{PHI}. \qquad (2)$$

The pinch-off characteristic measured at constant specific current in the transistor biased in saturation is a kernel of the EKV v2.6 parameter extraction [11, 12]. In the current formulation of the EKV v2.6 model the modified body effect factor accounts for both short and narrow channel effects:

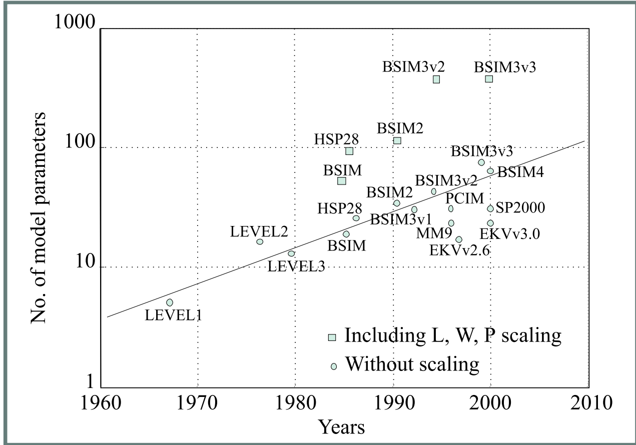

Fig. 2. Number of DC current parameters versus the year of the model introduction. Most recent versions of the BSIM, MM9 and EKV models are included.

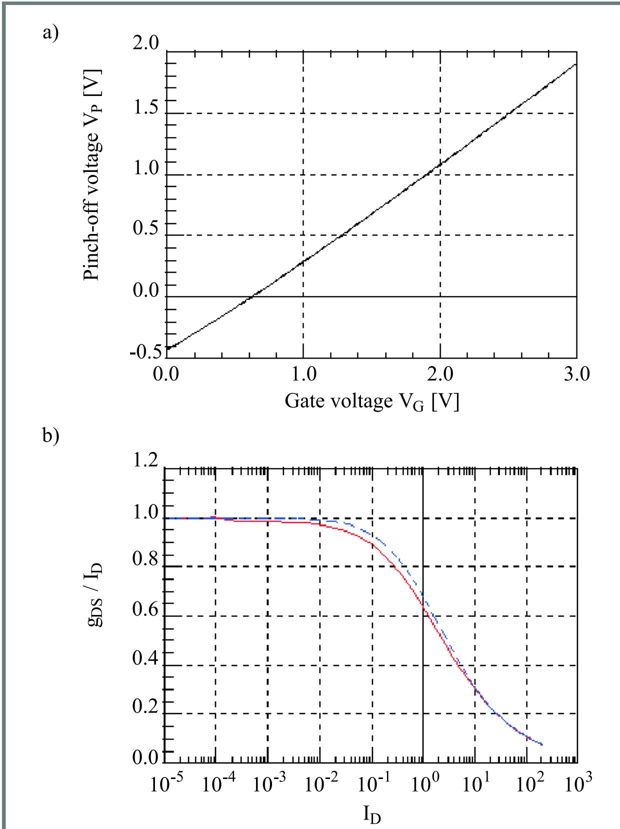

Fig. 3. (a) The pinch-off voltage (V_P vs V_G) characteristic for a NMOS transistor of a 0.5 μm technology. (b) Measured and simulated transconductance to normalized drain current (g_{DS}/I_D) ratio from weak through moderate to strong inversion.

$$\gamma' = GAMMA + \frac{\varepsilon_{Si}}{COX}\left[\frac{3 \cdot WETA}{W+DW}\sqrt{PHI+V_S} + -\frac{LETA}{L+DL}\left(\sqrt{PHI+V_D}+\sqrt{PHI+V_S}\right)\right]. \tag{3}$$

The slope factor n is defined as the inverse of the derivative of the pinch-off V_P vs V_G characteristic and therefore is a function of the same parameters: VTO, $GAMMA$ and PHI.

The drain current is derived under typical assumptions for charge-sheet models, including drift and diffusion components [9], and is normalized to the specific current I_S:

$$I_D = I_F(V_P - V_S) - I_R(V_P - V_D), \tag{4}$$

where

$$I_{F(R)}\left(V_P - V_{S(D)}\right) = I_S\, i_{f(r)}, \tag{5}$$

$$I_S \equiv 2nU_t^2\, \mu\, COX\, W_{eff}/L_{eff}, \tag{6}$$

$i_{f(r)}$ are normalized forward and reverse currents expressed by a simple function. The specific current I_S depends essentially on W/L and μ, where μ is the mobility accounting for vertical and lateral electric fields in the transistor channel.

Both components, the forward and reverse currents, have the same asymptotic behavior, which is exponential in weak inversion and quadratic in strong inversion. The intermediate region of moderate inversion is described by an interpolation function derived from physics. The expression for the drain current of an ideal long channel transistor requires only four parameters: the mobility related parameter KP, the threshold voltage VTO, the substrate effect parameter $GAMMA$ and the surface potential in strong inversion at equilibrium PHI. Second order effects such as mobility reduction due to the vertical field, velocity saturation and short- and narrow-channel effects are taken into account with additional model parameters. Another parameter, COX, is required so that charges and transcapacitances necessary for dynamic operation can also be expressed.

The reverse short channel effect (RSCE) is included in the pinch-off voltage V_P, in addition to the charge-sharing concept, to extend range on the EKV v2.6 model applications. The RSCE is described using simple expression [9]:

$$\Delta V_{RSCE} = \frac{2 \cdot Q0}{COX}\,\frac{1}{\left[1+0.5\left(\xi+\sqrt{\xi^2+C_\varepsilon}\right)\right]^2}, \tag{7}$$

where $\xi = C_1\ (10\ L_{eff}/LK - 1)$, C_1 and C_ε are constants. The parameters are the peak charge density at the source/drain ends $Q0$ and the characteristic length of charge distribution LK.

The substrate (impact ionization) current effect, which requires three model parameters, is modeled using the following expression [8]

$$I_{DB} = I_{DS}\frac{IBA}{IBB}\, V_{ds'}\, \exp\left(\frac{-IBB\, L_C}{V_{ds'}}\right), \tag{8}$$

where $V_{ds'} = V_D - V_S - IBN\ V_{DSS}$ and V_{DSS} is the drain to source saturation voltage. The substrate current is treated as a component of the total extrinsic drain current, flowing from the drain to the bulk. The total drain current is therefore expressed as $I_D = I_{DS} + I_{DB}$. Consequently, the substrate current affects the total extrinsic conductances, in particular the drain conductance.

The static DC model is completed with a continuous dynamic model, in which intrinsic charges and capacitances are expressed as continuous functions of the normalized forward and reverse currents, which are valid in all regions of operation. This implementation does not require additional model parameters. The same holds for the noise model. The thermal noise expression is continuous and valid from weak to strong inversion. A first order non-quasi-static (NQS) model for transadmittances is used for AC and transient analysis at high frequencies. Temperature behavior of the intrinsic model can be adapted using four parameters. Finally, many analog circuit applications are limited by the matching properties of the devices, which depend mainly on geometry and bias conditions. Unlike other MOS transistor models, the EKV v2.6 model also allows for geometry and bias-dependent matching analysis using Monte-Carlo statistical circuit simulation. The EKV v2.6 requires only three dedicated matching parameters.

Extrinsic model elements: series resistances, junction currents and capacitances, overlap capacitances along with temperature dependencies are implemented into model in conventional manner similar to many other models. Series resistances usually add two extra nodes. However if this should be avoided to increase efficiency, the following scheme allows to explicitly account for series resistance in drain current and conductances as discussed in [12]

$$\frac{I_D}{I_{D0}} = \frac{g_m}{g_{m0}} = \frac{g_{ms}}{g_{ms0}} = \frac{g_d}{g_{d0}} \cong \frac{1}{1+g_{ms0}\,R_S+g_{d0}\,R_D}, \quad (9)$$

where the subscript „0" denotes currents or conductances calculated without series resistances.

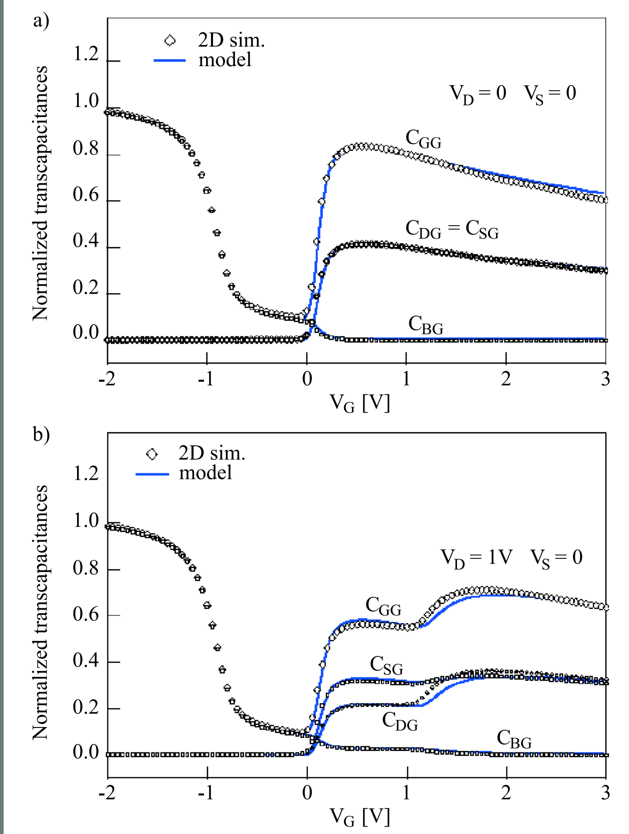

Fig. 4. Normalized transcapacitances versus gate voltage for n-channel device showing polysilicon depletion: (a) $V_D = V_S = 0$ V, (b) $V_D = 1$ V, $V_S = 0$ V. The new analytical model (lines) is compared to 2D numerical devices simulation (markers).

4. New polysilicon depletion model

The continuing increase of the channel doping concentration when scaling deep submicron CMOS technology using dual polysilicon gates accentuates the impact of the polysilicon depletion effect [16, 17] on all device characteristics. The new model, which correctly predicts transcapacitances as well as drain current and includes mobility reduction, has been published [18].

New compact modeling results are compared to the characteristics obtained from a 2D numerical device simulator. In Fig. 4, the normalized transcapacitances versus gate voltage are shown at various drain-to-source voltages, namely $V_D = 0$, 0.5, 1 V and $V_S = 0$ V. The new analytical model is compared to the numerical device simulation, and shows an excellent match for all bias conditions for all transcapacitances: C_{GG}, C_{DG}, C_{SG}, and C_{BG}. A single set of parameters is used in the analytical model for all bias conditions. The flat-band voltage has been adapted to match the measurement, and all other parameters match those underlying the 2D device simulation to within a few percent, i.e. to about the accuracy of the estimate of the doping concentrations in the gate and the substrate. The agreement at $V_D = V_S = 0$ V is excellent, $C_{DG} = C_{SG}$ is correctly predicted, and the value of $C_{DG} = C_{SG} = C_{GG}/2$ is correctly reached in strong inversion. At non-equilibrium conditions, the agreement is slightly degraded in the transition regions from saturation to non-saturation. Nonetheless, the overall qualitative behavior for an analytical model using only physical parameters remains excellent. Similar results have also been found with different levels of substrate and gate doping concentrations. Correct asymptotic behavior is found for all transcapacitances, including the ones not shown here, and is found to be further improved with respect to the previous linearization. Note that e.g. the correct behavior of $C_{BG} \rightarrow 0$ in strong inversion non-saturation, is due to the higher-order development of the bulk charge used, while its first-order counterpart would indeed lead to an incorrect asymptotic behavior of C_{BG}.

The effect of polydepletion on drain current versus gate voltage characteristics is shown in Fig. 5, for two values of drain voltage, V_D = 0.5 V and V_D = 1 V corresponding to the same cases as in Fig. 4. Two cases of polysilicon doping concentrations are shown, $N_p = 1 \cdot 10^{19}$ cm^3 corresponding to the same devices as used in Fig. 4, and $N_p = 9.1 \cdot 10^{20}$ cm^3 showing no polydepletion as a result. The same parameter set is used for the analytical model in both cases, except for the change in polysilicon doping concentration and a slight change in the flat-band voltage, due to a changed work function difference between the polyga-

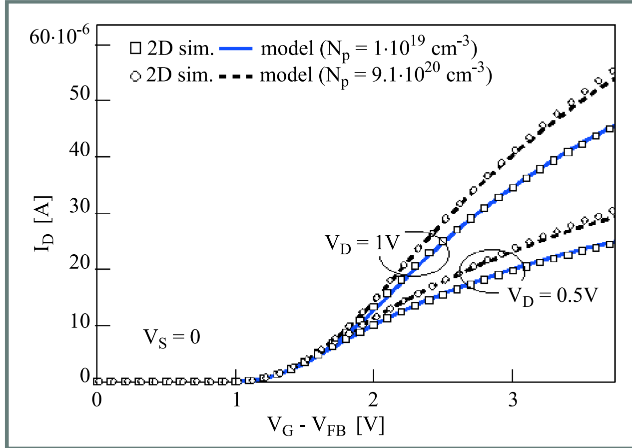

Fig. 5. Drain current versus gate voltage, for two drain voltages, V_D = 0.5 V; 1 V; V_S = 0 V, for two cases of polysilicon doping concentrations. 2D simulation (markers) and analytical model (lines). The model uses one set of parameters in all conditions except for changed gate doping concentration.

te and the substrate. The mobility model parameters have been chosen to match the case with polydepletion. As can be seen, the case without polydepletion is reasonably well matched without adapting model parameters further, confirming the coherence of the model. The slight difference observed may also stem from different processing circumstances for each cases.

5. New NQS charge based model

Despite various efforts devoted to high frequency and transient modeling of the MOS transistor, using both numerical and analytical approaches [19, 20], only incomplete sets of first-order NQS expressions were proposed for the kind of model discussed here [21]. The new model offers exact analytical of small signal NQS MOS transistor behavior, which is valid in all modes of operation and from DC to high frequencies, and was published in [22]. This is derived from a general charge based approach and uses the framework of the EKV model. It has been demonstrated that only four independent transadmittances are needed to fully characterize the small signal operation of the device. All quantities in the model are expressed in terms of normalized variables, which are independent of the process parameters. Only six independent real parameters (four transcapacitances and two transconductances) are needed to fully describe the low frequency, small signal, behavior of the intrinsic MOS transistor. It is also important to note that the intrinsic transcapacitances are nonreciprocal but satisfy the charge conservation condition.

In order to validate the model, experimental data taken from the literature have been used. These high frequency measurements were performed on PMOS transistors with 10 and 30 lm channel length and have been published [23]. The normalized y_{DG} data are plotted in Figs. 6a (magnitude) and 6b (phase). The set of curves, in both figures, depicts the normalized transconductances for the three channel lengths, in saturation mode. The corresponding theoretical characteristics, calculated in terms of Bessel functions, are also shown (note that, in Fig. 6, ny_{DG} is plotted instead of y_{DG}).

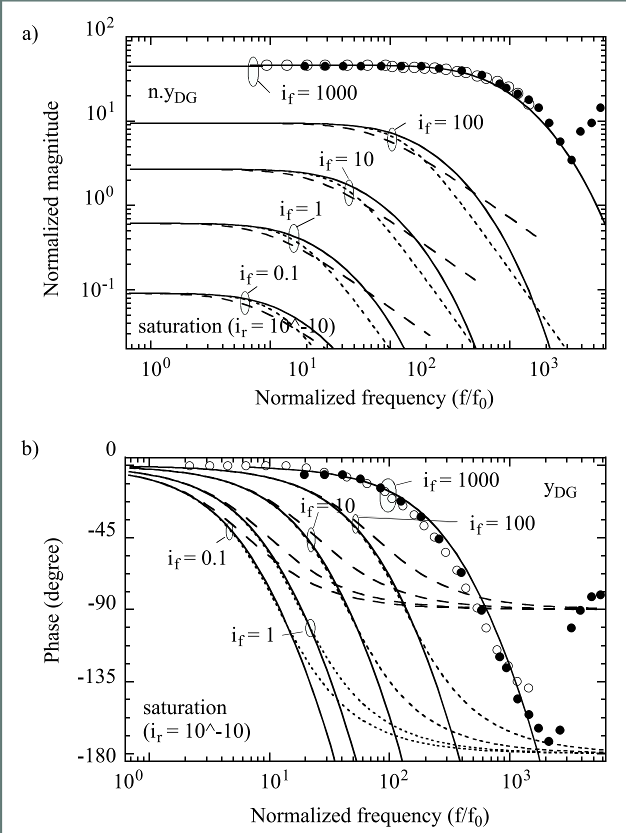

Fig. 6. Normalized plots of measured and simulated y_{DG} data: (a) magnitude and (b) phase.

A very good agreement between theory and experiment can be observed for both; the magnitude and phase characteristics, even for submicron devices. It can be noted that the phase shift appears well before the decrease in the magnitude of y_{DG}. This supports the accuracy of the model, as phase shift is difficult to predict precisely, especially over a large range of variation, as in the present case. The complete evaluation of the magnitude and phase characteristics of the model in saturation mode, from weak to strong inversion is possible. As expected, the accuracy of the second-order expressions is far better than the first-order one and appears to be sufficient for most practical applications. The agreement is fairly good for phase lags lower than 110°. On the contrary, the accuracy of the first-order expansion already degrades rapidly for phase shifts exceeding 30°.

6. RF characterization

The goal of the on-the-wafer MOSFET devices characterization is to obtain the electrical behavior of the intrinsic device, i.e. the transistor characteristic without the parasitic components associated with bond pads and interconnec-

tions. In order to achieve this goal proper vector network analyzer (VNA) calibration and MOSFET device parameter deembedding have to be performed.

6.1. VNA system calibration

Advanced VNAs offer number of the calibration options and standards. A full calibration of all parameters must be used to ensure the high accuracy needed for precise 2-port RF measurements. The calibration procedure removes most of errors including directivity, source match, load match, reflection tracking, transmission tracking and crosstalks.
The most commonly used calibration method is SOLT (short-open-load-thru) calibration available on every commercially available VNA. This calibration is the combination of two single-port SOL calibrations with additional measurements of a „thru" standard to complete the two port calibration. The SOLT standards are reasonably good modeled using simple lumped elements.

6.2. MOSFET parameters deembedding

The parasitics surrounding the transistor can be characterized by measuring two DUT pad frames after VNA system calibration. The measurements begin with the „open" test structure providing Y-parameters and with „short" test structure providing corresponding Y-parameters. The layout of both pad frames is based on a typical GSG (ground-signal-ground) pattern for on-the-wafer RF characterization. First measurements determine the interconnect parasitics which are assumed to be parallel to DUT. The second measurement is used to determine losses and phase rotation in the interconnect line. Once „open" and „short" pads frames are characterized, a large range of device geometries can be measured using the same de-embedding set. In order to demonstrate the advantages of the two-step de-embedding procedure, two experiments were performed over a wide frequency range up to 110 GHz to measure a short-channel MOSFET current gain characteristic from the Y-parameters (Fig. 7). The difference between the corrected curves applying the „open" and „open-short" de-embedding procedures is clearly seen for frequencies above 10 GHz. The simulation performed using the EKV v2.6 model with the extracted parameters from DC measurements and the factory default AC model parameters exhibits a qualitatively correct behavior, but shows the need for more a precise extraction of all intrinsic and extrinsic capacitances. The measurement data acquisition, calibration and de-embedding were performed using commercially available software packages [24, 25].

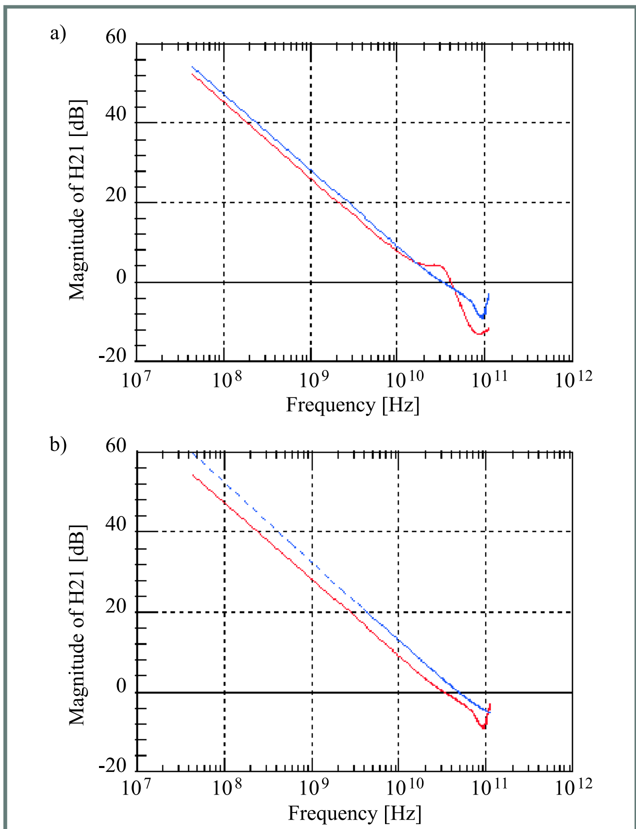

Fig. 7. (a) Open. (b) Open-short de-embedding and simulation current gain data up to 110 GHz (n-channel MOSFET device: 30 × 20 μm/0.35 μm). Bias: V_{gs} = 1.0 V, V_{ds} = 1.0 V.

6.3. RF parameter extraction

Several approaches were proposed to improve RF performance of compact models by simple modification of the MOSFET equivalent circuit. Modifications that use additional substrate resistances along with bulk diodes and series gate resistances were studied [14]; these are implemented as a simple equivalent. Elements such as gate resistance R_g and bulk resistance R_b cannot be neglected in RF operation because they are essential in forming the real part of the Y-parameters. Note that in some simulators, R_g and R_b are already parts of the MOSFET model, so that a subcircuit definition specific to RF is not needed.
The equivalent gate resistance R_g takes into account the sheet resistivity of the polysilicon gate layer and the gate contact resistance. It can be estimated from the device geometry and plays a major role in the phase characteristics of the input Y11 and transfer admittances Y12 & Y21 of short channel devices.
The addition of the substrate equivalent resistance R_b allows a simple but reasonably accurate modeling of the output characteristics Y22. It may be bias-dependent in order to include the variations of the depleted regions close to the source and drain junctions.
As Y11, Y12 & Y21 are very weakly dependent on R_b, a first estimate of R_g can be obtained from Re{1/Y11}. The total gate capacitance C_{gg} is extracted from Im{Y11} while Im{Y12} provides a precise evaluation of the gate-to-drain overlap capacitance C_{gd} . The extraction of R_b is based on Y22 data. The values of these additional parameters, as well as of other AC model parameters are then globally optimized.
Using EKV v2.6 for the intrinsic device, it is shown from

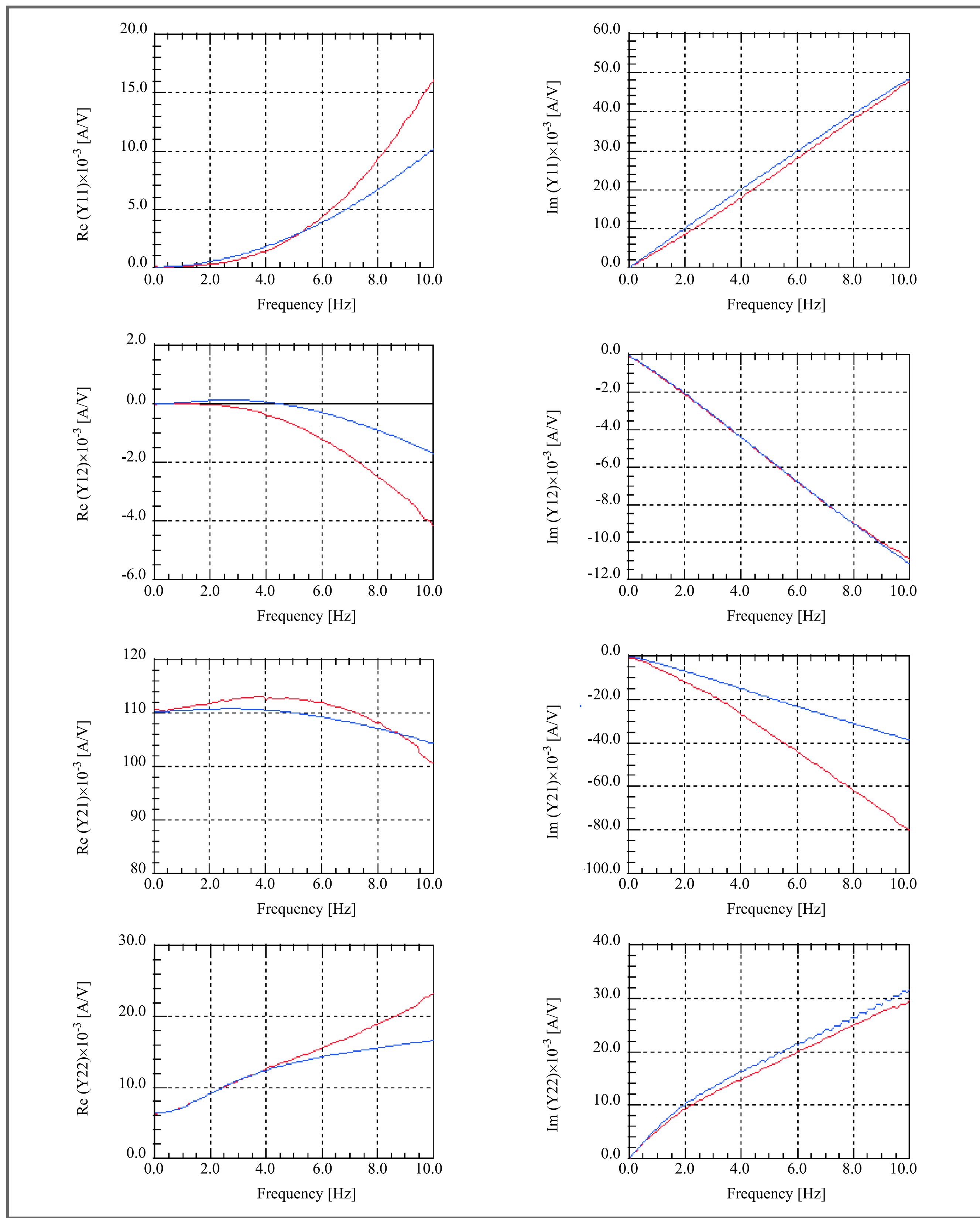

Fig. 8. Comparison between measured and simulated Y parameters for an n-channel MOSFET (30 × 20 µm/0.35 µm), $V_{gs} = V_{ds} = 1$ V. Frequency span is 0÷10 GHz.

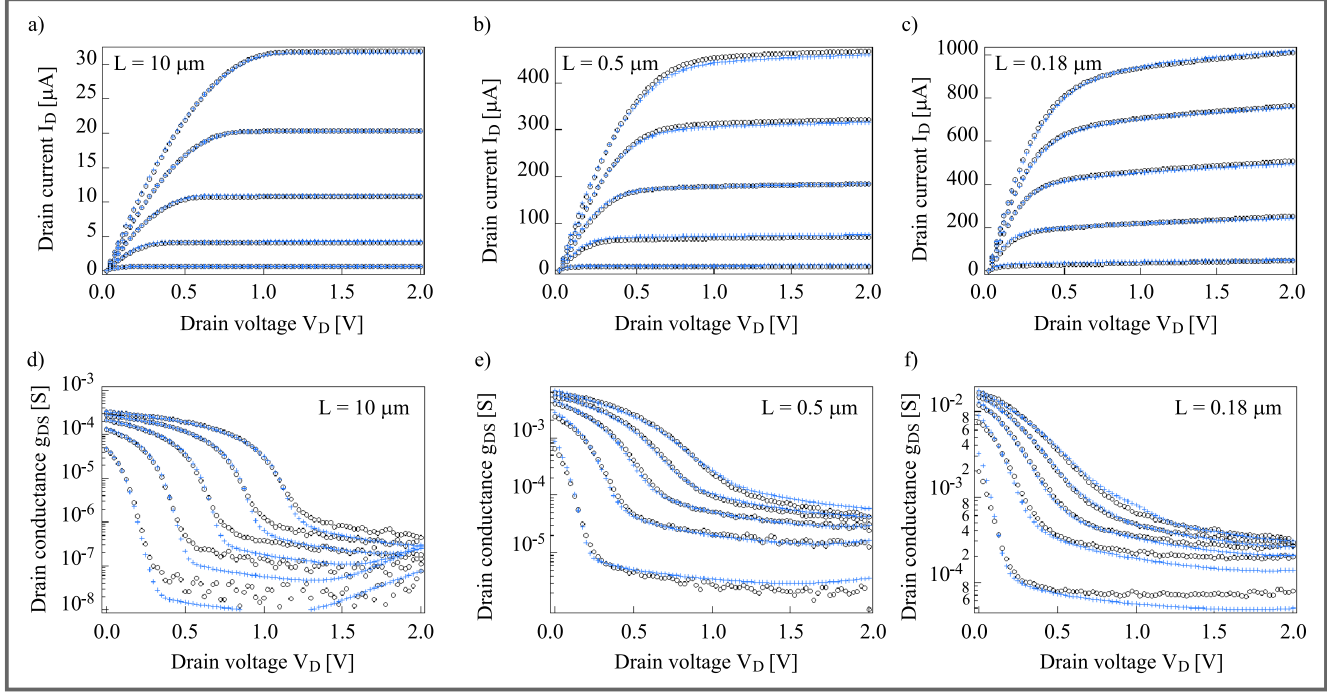

Fig. 9. The simulated (o) and measured (-) output current (I_D) (a), (b), (c) and conductance (g_{DS}) (d), (e), (f) for n-channel devices of a standard 0.18 µm CMOS process.

Fig. 8 that the resulting model validity typically covers DC to 5 GHz for 0.35 µm devices. The values for R_g and R_b were found to be 5 Ω and 50 Ω, respectively. This shows that losses associated with the bulk connection come into play already at 1 GHz. The imaginary part of the Y parameters is accurately predicted except for the Y21 transcapacitance. The latter discrepancy is attributed to short-channel effects not accounted for in the channel charge calculation. This is consistent with the noticeable difference between the measured and simulated of the current gain characteristics for this particular MOSFET transistor.

For medium- and long-channel MOSFETs, R_g can be neglected compared to the bias-dependent, nonquasistatic (NQS) effects due to the distributed nature of the channel. Although any charge-based MOS model intrinsically pro-vides a first-order fit of the transadmittance (through the so-called transcapacitances), a consistent modeling of the NQS effects requires more specific extensions of the compact model, for which the EKV MOSFET model formulation is particularly suitable [22].

7. Model applications

7.1. DC circuits evaluation

The scaling model performance with the channel length is presented using a standard 0.18 µm CMOS process. Figure 9 shows the measured and simulated output characteristics (I_D vs V_D and g_{DS} vs V_D) at different V_G for the devices with $W = 10$ µm and $L = 10$, 1 and 0.5 µm, respectively. The output conductance is adequately modeled using one unique parameter set for all geometries in conduction as well as in saturation.

The next example shows the benchmark results of D/A converter circuit analysis using the EKV v2.6 model. The insert of Fig. 10 shows a typical current divider circuit used

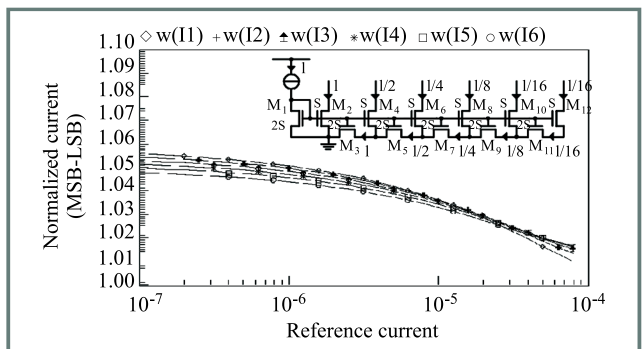

Fig. 10. The normalized branch currents versus reference current for typical current divider circuit used in D/A converters (the insert shows divider stages).

in D/A converters. The circuit designed is based on the principle of an R-2R ladder circuit. Each stage divides the reference current by a factor of 2. Simulation results show expected behavior of the perfect current divider over several decades of reference current. The estimated error is less than 5% for LSB.

7.2. RF circuits evaluation

To test the performance to the EKV v2.6 model, a circuit level evaluation was performed using two different RF

chips. As a first example, a simple power amplifier (PA) well suited for RF MOSFET model evaluation has been chosen to illustrate the use of the new subcircuit model. The core of the PA is an interdigitated 0.35 mm NMOS transistor, encapsulated into a SO-8 package. The circuit operates at 900 MHz as an overdriven class B PA. Output power vs input power characteristics (Fig. 11) were measured and simulated at two different supply voltages, 2.7 V and 1.5 V, respectively. A good agreement for broad power range has been achieved. In the second example, a harmonic oscillator was designed and fabricated in the same 0.35 mm CMOS technology. The oscillator operates at 900 MHz and with 3 V power supply has phase noise of −101 dBc/Hz 25 kHz. Figure 12 shows basic characteristics of the oscillator. Performed simulations based on the EKV v2.6 model accurately predict the circuit performance.

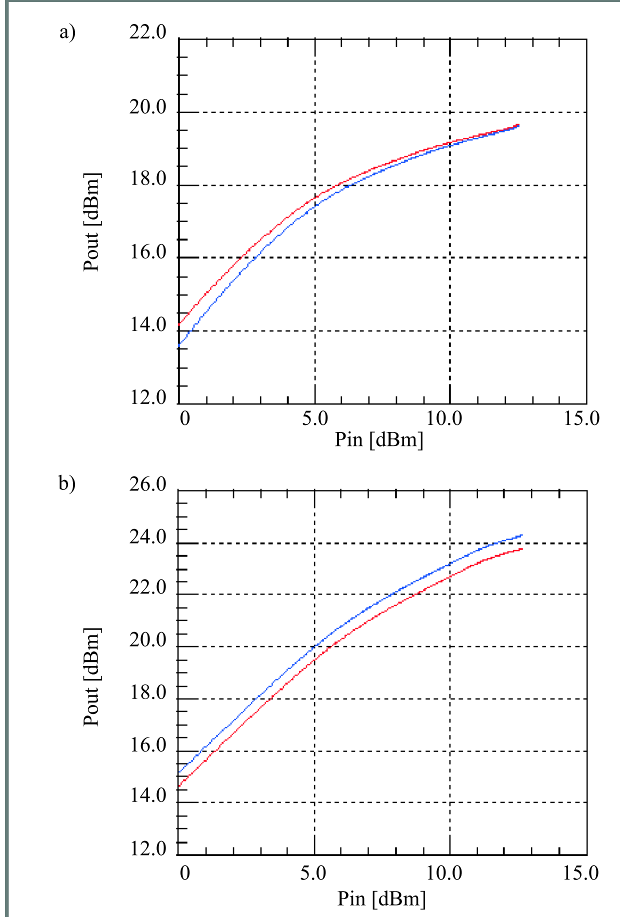

Fig. 11. Output power vs input power characteristics of the PA. Supply voltage is: (a) 1.5 V and (b) 2.7 V.

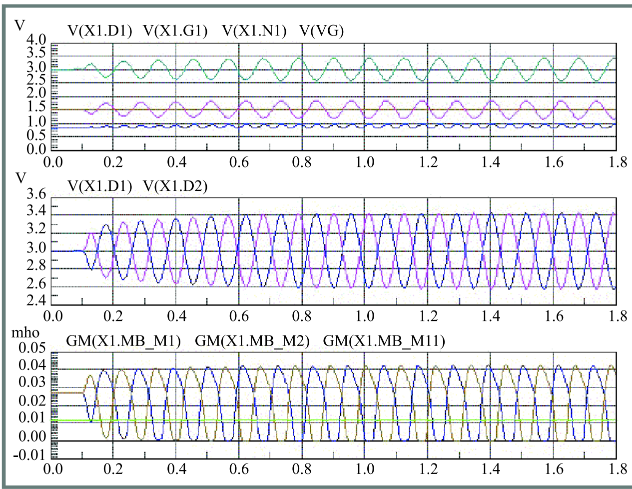

Fig. 12. Simulated characteristics of the 900 MHz harmonic oscillator.

Acknowledgments

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Invited paper

On the extraction of threshold voltage, effective channel length and series resistance of MOSFETs

Adelmo Ortiz-Conde, Francisco J. García Sánchez, and Juin J. Liou

Abstract — The first part of this article presents the modeling of the long-channel bulk MOSFET as a particular case of the SOI MOSFET. The second part reviews compares and scrutinizes various methods to extract the threshold voltage, the effective channel and the individual values of drain and source resistances. These are important device parameters for modeling and circuit simulation.

Keywords — ***threshold voltage, channel length, series resistance, parameter extraction.***

1. Introduction

Since the early 1980s, the MOSFET has become the most widely used semiconductor device in very large scale integrated circuits. This is due mainly to the fact that the MOSFET has a simpler structure, costs less to fabricate, and consumes less power than its bipolar transistor counterpart.

In this article, we will first present, in Section 2, an overview of the modeling of long-channel bulk MOSFET [1–11] as a particular case of the long-channel SOI MOSFET [12–16]. Then, we will focus on issues related to extraction of MOSFET device parameters [17–20] and it will be organized into three sections. Section 3, covers the topic of extracting the threshold voltage. An overview is first provided to discuss and compare the advantages and disadvantages of various existing extraction methods for the threshold voltage.

Section 4 is concerned with the various methods for extracting the effective channel length, probably the most important device parameter of the MOSFET. They include a method based on metallurgical junctions, current-voltage method, capacitance-voltage method, shift and ratio method, and a method based on device simulation. The procedures and developments of these methods are discussed and their accuracy, advantages, and disadvantages are compared.

Section 5 deals with the extraction of the drain and source resistances of MOSFETs, which are important device parameters in characterizing the voltage drops in the drain and source regions of these devices.

2. MOSFET modeling

The fundamental benefits of the silicon-on-insulator (SOI) structure over the traditional bulk MOSFET have motivated considerable recent research work [12–16]. The main benefits include suppression of latch-up, higher circuit speed, lower power consumption, greater immunity to radiation, increase of the density, 3D integration, and reduction of short-channel effects. Good review articles were presented recently by Jurczak [14] describing and comparing the various SOI's models, and by Alles [13] scrutinizing the motivations of using SOI in integrated circuits.

Probably the most important motivation today for using the SOI device is the lower power consumption, especially in the portable electronics arena where the supply voltage is reduced in order to decrease the power consumption. If the supply voltage is reduced, the threshold voltage must also be reduced. However, the degree of the reduction of the supply and threshold voltages is limited by the subthreshold slope, which is defined as the gate voltage required to increase the drain current by one order of magnitude in weak inversion. The SOI device has a larger subthreshold slope and thus a lower leakage current than its bulk counterpart. This allows the use of a SOI MOSFET with a small threshold voltage, thus the use of a smaller supply voltage, without having to be concerned with a significant leakage current. On the other hand, for the bulk MOSFET, a large threshold voltage, and thus a large supply voltage, is needed to ensure a small leakage current in the device.

2.1. Modeling of the (SOI) MOSFET

Figure 1 gives the schematic of silicon-on-insulator MOSFET. It can be seen that the main feature differentiating the SOI MOSFET from its bulk counterpart is the fact that the SOI MOSFET has both front and back oxide interfaces and therefore is subjected to charge coupling effects between the two gates. The bulk MOSFET can therefore be considered as a special case of an SOI MOSFET with a very large semiconductor film thickness. The mixed boundary condition at the front oxide-silicon interface yields

$$V_{GS}^{f} - V_{FB}^{f} = \Psi_{Sf} + \frac{\varepsilon_s \xi_{Sf}}{C_{of}} , \qquad (1)$$

where V_{GS}^{f} is the front-gate voltage, V_{FB}^{f} is the front-flatband voltage, C_{of} is the front-oxide capacitance, Ψ_{Sf} is the front-

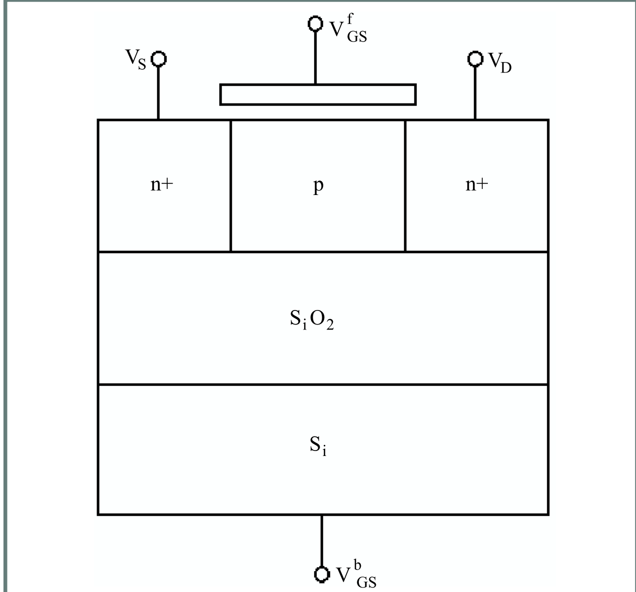

Fig. 1. A two-dimensional SOI MOSFET structure showing the top and bottom Si-SiO_2 interfaces.

surface band bending and ξ_{Sf} is the front-surface electric field.

On the other hand, at the back oxide-silicon interface, the boundary condition is

$$V^b_{GS} - V^b_{FB} = \Psi_{Sb} - \frac{\varepsilon_s \xi_{Sb}}{C_{ob}}, \quad (2)$$

where V^b_{GS} is the back-gate voltage, V^b_{FB} is the back-flatband voltage, C_{ob} is the back-oxide capacitance, Ψ_{Sb} is the back-surface band bending and ξ_{Sb} is the back-surface electric field. The front-interface ($x = 0, \Psi = \Psi_{Sf}$ and $\xi = \xi_{Sf}$) and at the back-interface ($x = t_b, \Psi = \Psi_{Sb}$ and $\xi = \xi_{Sb}$), are related by [14–16,18]:

$$\xi^2_{Sf} - F^2(\Psi_{Sf}, V) = \xi^2_{Sb} - F^2(\Psi_{Sb}, V) \equiv \alpha, \quad (3)$$

where $F^2(\Psi, V)$ is the Kingston function defined by [4]:

$$F^2(\Psi,V) \equiv \int \frac{-2\rho}{\varepsilon_s} d\Psi = = \frac{2}{\beta^2 L_D^2}\left(\left(e^{-\beta\Psi} + \beta\Psi - 1\right) + \frac{n_o}{p_o}\left(e^{-\beta V}\left(e^{\beta\Psi} - 1\right) - \beta\Psi\right)\right) \quad (4)$$

and α, unlike the bulk MOSFET, is not equal to zero but is a parameter that quantifies the charge coupling between the front- and back-gates. Here, p_o and n_o are the equilibrium hole and electron densities, $\beta = q/kT$ is the inverse of the thermal voltage, and L_D is the extrinsic Debye length given by

$$L_D = \left(\frac{\varepsilon_s}{q\beta p_o}\right)^{1/2}. \quad (5)$$

Finally, the semiconductor film thickness t_b can be expressed by

$$t_b = \int_{\Psi_{Sb}}^{\Psi_{Sf}} \frac{d\Psi}{\xi}. \quad (6)$$

The values of $\Psi_{Sf}, \Psi_{Sb}, \xi_{Sf}$ and ξ_{Sb} can be calculated numerically from Eqs. (3)–(6).

The drain current for the SOI MOSFET can be expressed by the following single-integral equation [16]:

$$I_D = \mu_n \frac{W}{L_{eff}}\Bigg[C_{of}\Bigg(\left(V^f_{GS} - V^f_{FB}\right)\left(\Psi_{SfL} - \Psi_{Sfo}\right) + - \frac{\left(\Psi^2_{SfL} - \Psi^2_{Sfo}\right)}{2}\Bigg) + \frac{Q_b n_o^2}{\beta}\left(\beta V_{DS} + e^{-\beta V_{DS}} - 1\right) + + \varepsilon_s \int_{\Psi_{Sbo}}^{\Psi_{Sfo}} \xi\left(\Psi, V = 0\right) d\Psi - \varepsilon_s \int_{\Psi_{SbL}}^{\Psi_{SfL}} \xi\left(\Psi, V = V_{DS}\right) d\Psi + + \frac{\varepsilon_s t_b \left(\alpha_L - \alpha_o\right)}{2} + + C_{ob}\Bigg(\left(V^b_{GS} - V^f_{FB}\right)\left(\Psi_{SbL} - \Psi_{Sbo}\right) - \frac{\left(\Psi^2_{SbL} - \Psi^2_{Sbo}\right)}{2}\Bigg)\Bigg], \quad (7)$$

where Q_b is the body depletion charge ($Q_b = -qN_A t_b$), $\Psi_{Sf}(y = y_s) = \Psi_{Sfo}$, $\Psi_{Sf}(y = y_d) = \Psi_{SfL}$, $\Psi_{sb}(y = y_s) = = \Psi_{Sb}$, $\Psi_{Sb}(y = y_d) = \Psi_{SbL}$, $\alpha(y = y_s) = \alpha_o$, $\alpha(y = y_d) = = \alpha_L$, and $L_{eff} = (y_d - y_s)$ is the effective channel length.

2.2. Pierret-Shield's model

For a very large t_b, as would be the case for a bulk MOSFET, the charge coupling between the front- and back gate diminishes, and α_o and α_L approach zero. Also, for this case, there will be a point x_o inside the semiconductor at which $\Psi(x = x_o) = \xi(x = x_o) = 0$. Taking the point x_o to be the back interface, we get $\Psi_{Sbo} = \Psi_{SbL} = 0$, and Eq. (7) reduces to Pierret-Shield's model [8] for the bulk MOSFET:

$$I_D = \mu_n \frac{W}{L_{eff}}\Bigg[C_o\Bigg(\left(V_{GS} - V_{FB}\right)\left(\Psi_{SL} - \Psi_{So}\right) + - \frac{\left(\Psi^2_{SL} - \Psi^2_{So}\right)}{2}\Bigg) + \varepsilon_s \int_0^{\Psi_{So}} F\left(\Psi, V = 0\right) d\Psi + - \varepsilon_s \int_0^{\Psi_{SL}} F\left(\Psi, V = V_{DS}\right) d\Psi\Bigg], \quad (8)$$

where $\Psi_S(y = y_s) \equiv \Psi_{So}$ and $\Psi_S(y = y_d) \equiv \Psi_{SL}$. This model is also valid for long-channel MOSFETs under all inversion conditions.

2.3. Charge-sheet model

It should be pointed out that using the following empirical approximation,

$$\left(F^2\left(\Psi, V\right)\right)^{1/2} \approx \approx \frac{2^{1/2}}{\beta L_D}\left(\left(\beta\Psi - 1\right)^{1/2} - \frac{\left(\beta\Psi - 1\right)^{-1/2}}{2}\right), \quad (9)$$

Pierret's model yields to the charge-sheet model [1, 9, 10] defined by

$$I_D = \mu_n \frac{W}{L_{eff}} \Bigg[C_o \Big((V_{GS} - V_{FB})(\Psi_{SL} - \Psi_{So}) - \frac{(\Psi_{SL}^2 - \Psi_{So}^2)}{2} \Big) + - \frac{q N_A L_D 2^{3/2}}{3} \Big((\beta \Psi_{SL} - 1)^{3/2} - (\beta \Psi_{So} - 1)^{3/2} \Big) + + q N_A L_D 2^{1/2} \Big((\beta \Psi_{SL} - 1)^{1/2} - (\beta \Psi_{So} - 1)^{1/2} \Big) \Bigg] . \quad (10)$$

This model, which is also valid for long-channel MOSFETs under all inversion conditions, has an error of 5% or less compared the Pao-Sah counterpart. This model has been classically derived from the assumption that the inversion charge is an infinitesimally thick layer near the interface.

2.4. Strong inversion model

The drain current models discussed above can be simplified under the strong inversion condition. For this case, the surface band bending increases very little with increasing gate bias and this allows one to assume that band bending is nearly independent of the gate bias under strong inversion. Thus,

$$\Psi_{So} \approx 2\phi_B , \quad (11)$$

at the source, and

$$\Psi_{SL} \approx 2\phi_B + V_{DS} , \quad (12)$$

at the drain where ϕ_B is the bulk potential. Also, under strong inversion, the inequality $\beta\Psi >> 1$ is valid, and Eq. (4) can be approximated by

$$F^2(\Psi, V) \approx \frac{2\Psi}{\beta L_D^2} . \quad (13)$$

Putting Eqs. (11)–(13) into Eq. (8), and integrating the resulting equation yields the following analytic expression for the drain current:

$$I_D = \mu_n \frac{W}{L_{eff}} C_o \Big[\Big(V_{GS} - V_{FB} - 2\phi_B - \frac{V_{DS}}{2} \Big) V_{DS} + - \frac{2(2\varepsilon_s q N_A)^{1/2}}{3 C_o} \Big((V_{DS} + 2\phi_B)^{3/2} - (2\phi_B)^{3/2} \Big) \Big] . \quad (14)$$

It is important to mention that the model in Eq. (14) is valid only when the inversion layer is present in the entire channel, a case which holds for a relatively small drain voltage.

2.5. SPICE model

The simplest MOSFET SPICE model (i.e., level-1 model) [3–6] can be obtained as follows. Consider the case of strong inversion and assume

$$V_{DS} \gg 2\phi_B . \quad (15)$$

Next, using the Taylor's series to approximate the terms having the power of 3/2 in Eq. (14), one obtain:

$$I_D = \mu_n \frac{W}{L_{eff}} C_o \Big[V_{GS} - V_T - \frac{V_{DS}}{2} \Big] V_{DS} , \quad (16)$$

where

$$V_T \equiv V_{FB} + 2\phi_B + \frac{2(\varepsilon_s q N_A \phi_B)^{1/2}}{C_o} \quad (17)$$

is the threshold voltage. Equation (17) can be rewritten by noting that its last term is related to the maximum depletion charge Q_{dmax} (i.e., Q_d becomes Q_{dmax}) which occurs at the onset of inversion,

$$V_T \equiv V_{FB} + 2\phi_B - \frac{Q_{dmax}}{C_o} . \quad (18)$$

It is important to point out that Eq. (17) is valid only when the substrate voltage V_{BS} is zero (i.e., no body effect). On the other hand, Eq. (18) is more general and is valid with the presence of body effect, provided the depletion charge accounts for the effect of V_{BS}.

Clearly, the threshold voltage is an important parameter for modeling the MOSFET. Beside modeling V_T, as was done in Eqs. (17) and (18), such a parameter can be determined by extraction methods, which will be discussed in detail in next section.

3. Extraction of the threshold voltage

3.1. Previous methods

One of the most important parameters to model the operation of a MOSFET is the threshold voltage, V_T . There are several definitions of threshold voltage [2, 4, 21] and many methods have been developed to extract this parameter. The majority of procedures used to determine V_T are based in the strong inversion operation characteristics. The most common methods are [18]: a) defining V_T as the gate voltage corresponding to a certain predefined practical constant drain current [17]; b) finding the gate voltage axis intercept of the linear extrapolation of the $I_D - V_{GS}$ characteristics at its maximum first derivative (slope) point [4]; c) determining V_T at the maximum of the second derivative of I_D with respect to V_{GS} [22]; d) finding the gate voltage axis intercept of the ratio of the conductance to the square root of the transconductance, which requires two derivatives of the data [23].

The procedures for extracting V_T by the linear and second-derivative extrapolation methods are illustrated in Figs. 2a and 2b, respectively.

In this figure, the measured data are from an n-MOSFET with mask channel length of 0.6 μm, oxide thickness of 14 nm and channel doping of 10^{17} cm^{-3}. For the linear extrapolation method V_T is determined by extrapolating at the point of maximum slope on the $I_D - V_{GS}$ characteristics. On the other hand, the second-derivative extrapolation method determines V_T at the point where the second derivative of $I_D - V_{GS}$ is maximum.

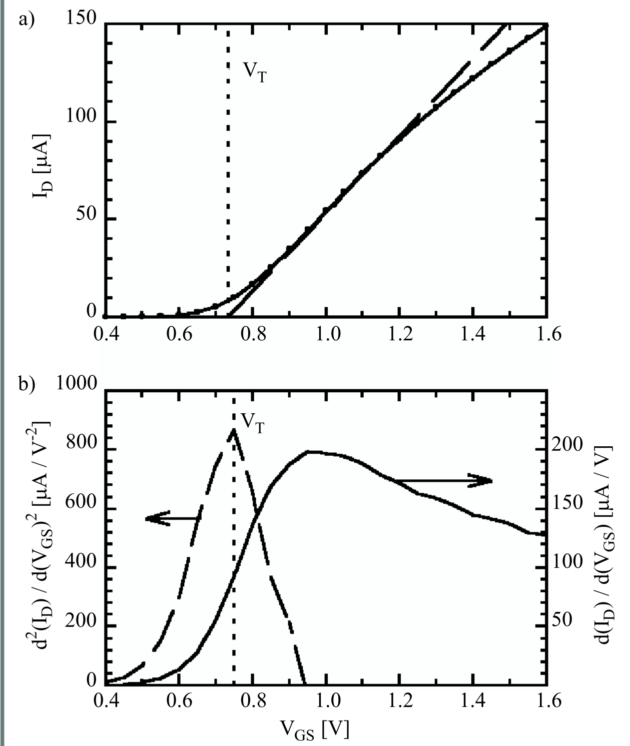

Fig. 2. Illustration of the linear extrapolation (a) and second derivative (b) methods to extract V_T.

Other methods have been proposed. One uses the subthreshold operation characteristics to determine V_T from the gate voltage necessary to make the surface potential equal to twice the bulk potential [24]. Recently a new procedure was presented to extract the threshold voltage independently of the presence of source and drain parasitic resistances [25].

Contrasting with previous methods where the extraction algorithm is generally restricted to the strong inversion characteristics, or perhaps to the subthreshold characteristics, a recent method [26, 27] that uses the transition from subthreshold to strong inversion operation to determine the threshold voltage was presented. This transition method does not utilize any differentiation of the data, rather it makes use of integration which greatly reduces the effect of possible random noise or measurement error in the experimental data.

3.2. Transition's method

The drain current in the subthreshold region, can be modeled by an exponential expression of the form [1–11]

$$I_D = I_{S0} \exp\left[\beta\left(V_{GS} - V_T\right)/n\right], \tag{19}$$

where V_{GS} is the intrinsic gate-to-source voltage, and n is a quality factor known as the subthreshold slope. I_{S0} is a coefficient that depends on the gate capacitance per unit area, the effective size, the effective mobility of the channel, the thermal voltage, and the intrinsic drain-to-source voltage [6, 18].

In contrast, in strong inversion, the drain current can be modeled for small V_{DS} by a linear expression of the form [1–11]

$$I_D \approx K\left(V_{GS} - V_T\right)V_{DS}, \tag{20}$$

where K depends on the gate capacitance per unit area, the effective size and the effective mobility of the channel. In the transition region neither Eqs. (19) nor (20) are valid and the $I_D - V_{GS}$ characteristics change from exponential to linear behavior, or correspondingly, the $\ln I_D - V_{GS}$ characteristics change from linear to logarithmic behavior, as depicted in Fig. 3 for a 10 μm long n-channel MOSFET

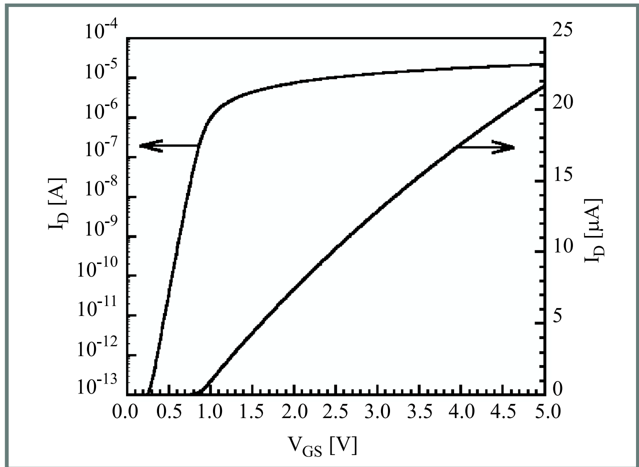

Fig. 3. Drain current as a function of gate voltage for BSIM3v3.2 modeled variable mobility long n-channel MOSFET, at $V_{BS} = 0$, $V_{DS} = 50$ mV.

simulated using the AIM-SPICE [6] Level 17 BSIM3v3.2 model [5]. This transition from linear to logarithmic behavior is analogous to the I-V characteristic of a diode with a parasitic series resistance. To eliminate the effects of the series resistance in a diode, an integral function was proposed [28, 29].

As previously stated, the threshold voltage is the value of gate voltage at which the $I_D - V_{GS}$ characteristics change from exponential to linear behavior. In order to find this transition point and thus extract the threshold voltage we will use an auxiliary function that has already proved its usefulness in getting rid of parasitic resistances when extracting the model parameters of diodes [28, 29].

First, the drain current of the MOSFET is measured versus gate voltage from below to well above threshold with zero body bias and a small constant value of drain voltage. Second, the following function is numerically calculated from

the measured data:

$$G(V_{GS}, I_D) = V_{GS} - 2\,\frac{\int_{V_{GSb}}^{V_{GSa}} I_D(V_{GS})\, dV_{GS}}{I_D}\,, \qquad (21)$$

where V_{GSb} and V_{GSa} are the lower and upper limits of integration corresponding to gate-to-source voltages below and above threshold, respectively.

Third, when $G(V_{GS}, I_D)$ is plotted as a function of $\ln I_D$ it becomes a linear function wherever $I_D(V_{GS})$ is exponential, and additionally it has the property of vanishing wherever $I_D(V_{GS})$ is linear [28, 29]. Therefore, a plot of G versus $\ln I_D$ should be a straight line below threshold, where the current is dominated by diffusion and consequently it is predominantly exponential. Furthermore, G should drop abruptly to zero as soon as the threshold voltage is surpassed, since above this point the current is dominated by drift and hence it is predominantly lineal.

Figure 4 presents a plot of such a behavior of G, which was numerically calculated using Eq. (21) and the data in

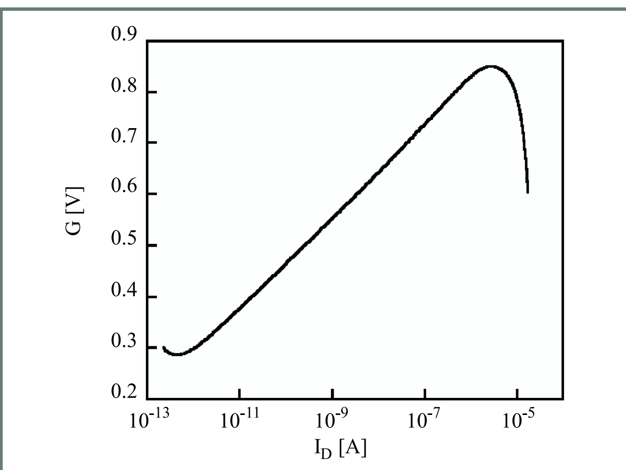

Fig. 4. Function G calculated by applying Eq. (21) to the modeled $I_D - V_{GS}$ characteristics of the previous figure. The maximum G represents the value of $V_T = 0.850$ V.

Fig. 3. As expected, the curve is seen to behave approximately as a straight line until it reaches a maximum value of about 0.850 V, at which point it falls rapidly towards zero indicating that the current has become predominantly lineal. This maximum value of G corresponds to the threshold voltage of the device and compares well to the value of $V_T = 0.855$ V which was separately extracted for this device using the conventional second-derivative method.

4. The effective channel length

The so-called channel length is a broad description of three different channel lengths. One is the mask channel length L_m, which denotes the physical length of the gate mask. Another is the electrical effective channel length L_{eff}, which defines the length of a region near the Si-SiO$_2$ interface in which the inversion free-carrier density is controlled by the gate voltage. This channel length is given by

$$L_{eff} = L_m - \Delta L_{eff}\,, \qquad (22)$$

where ΔL_{eff} is the effective channel length reduction illustrated in Fig. 5. The third channel length used frequently is

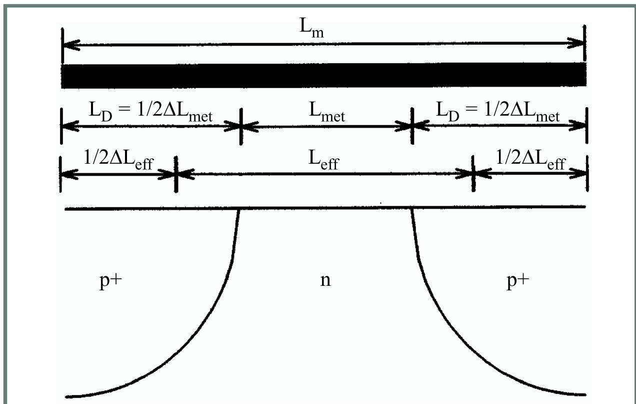

Fig. 5. Device structure of a p-channel MOSFET showing the definitions of L_{eff}, L_{met} and L_m.

the metallurgical channel length L_{met}, which is the distance between the source and drain metallurgical junctions at the Si-SiO$_2$ interface:

$$L_{met} = L_m - \Delta L_{met}\,, \qquad (23)$$

where $\Delta L_{met} = 2L_D$, and L_D is the length of the lateral diffusion of the source or drain region (see Fig. 5).

The precise determination of the effective channel length is not straightforward due mainly to the uncertainty as to whether the portion of the drain and source regions underneath the gate should be considered as part of L_{eff} (i.e., $L_{eff} > L_{met}$) or as part of the drain and source series resistance and thus not part of L_{eff} (i.e., $L_{eff} = L_{met}$). Recent studies have concluded [30, 31] that the theory of $L_{eff} > L_{met}$ is more appropriate because the free-carrier density in the drain and source regions underneath the gate is influenced by the gate voltage.

Since ΔL_{eff}, and thus L_{eff}, cannot be measured directly, various methods have been developed in the literature to extract them from the current-voltage characteristics [32–37], capacitance-voltage characteristics [38–44], or physical insight provided by numerical simulation [30, 45]. The main disadvantage of the methods based on current-voltage characteristics, called the I-V methods, is that they are often obscured by the presence of the parasitic drain and source series resistance. On the other hand, the main disadvantage of the capacitance-voltage (C-V) methods, is that equipment with high resolution is required to measure the small capacitances in the MOSFET (in the order of fento farads). Methods based on device physical insight require results simulated from device simulators, the accuracy of which depends on the proper selection of model parameters.

In the following sections, the development of the different extraction methods will be discussed.

4.1. Current-voltage methods

4.1.1. Terada-Muta or Chern et al. method

The method by Terada-Muta [33] or Chern et al. [34] was derived based on the following simple current-voltage relationship for the drain current in the linear region:

$$I_D = \frac{W}{L_{eff}} \mu C_o (V_{GS} - V_T) V_{DS} \, , \tag{24}$$

where W is the channel width, C_o is the oxide capacitance per unit area, μ is the effective free-carrier mobility, V_T is the threshold voltage, and V_{GS} and V_{DS} are the intrinsic gate-source and drain-source voltages, respectively. The intrinsic voltages can be related to the external gate-source and drain-source voltages (V_g and V_d):

$$V_{GS} = V_g - I_D R_S \tag{25}$$

and

$$V_{DS} = V_d - I_D (R_S + R_D) \, . \tag{26}$$

Here R_D and R_S are the drain and source parasitic series resistances illustrated in Fig. 6.

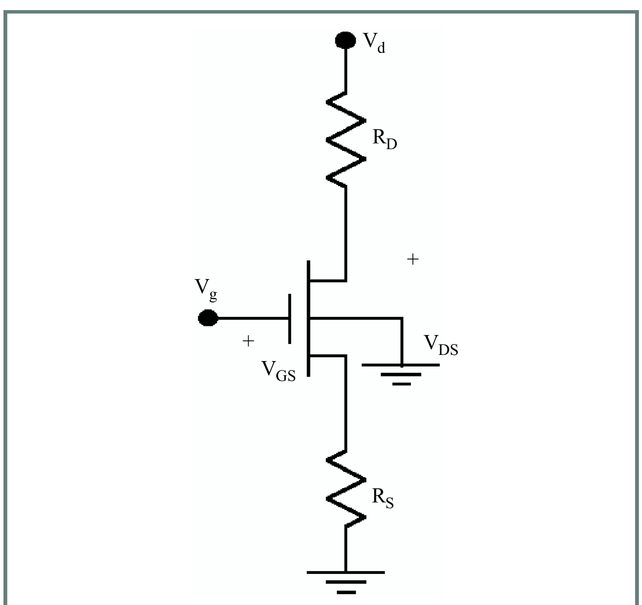

Fig. 6. MOSFET equivalent circuit including the source and drain series resistances (R_S and R_D) and having the body and source terminals grounded.

Combining Eqs. (24) and (26), the total channel resistance, R_m, can be expressed by

$$R_m \equiv \frac{V_d}{I_D} = R_{DS} + \frac{(L_m - \Delta L_{eff})}{\mu C_o W (V_{GS} - V_T)} \, , \tag{27}$$

where $R_{DS} \equiv (R_D + R_S)$ is the total drain and source resistance. For the linear region under study, $(V_g - V_T)$ is much larger than $I_D R_{DS}$, and $V_g \approx V_{GS}$. This results in

$$R_m = R_{DS} + \frac{(L_m - \Delta L_{eff})}{\mu C_o W (V_g - V_T)} \, . \tag{28}$$

Then, according to Eq. (28), the plot of R_m versus L_m is a straight line for a given $(V_g - V_T)$, and the unique intersection of all the straight lines for different $(V_g - V_T)$ yields ΔL_{eff} on the L_m axis (i.e., x axis) and R_{DS} on the R_m axis (i.e., y axis). It is important to point out that the threshold voltage is a function of L_m.

Although widely used, the Terada-Muta method has been found to fail at nitrogen liquid temperature [36, 46] because it yields no unique intersection of the straight lines as illustrated in Fig. 7. In this figure we present R_m versus L_m

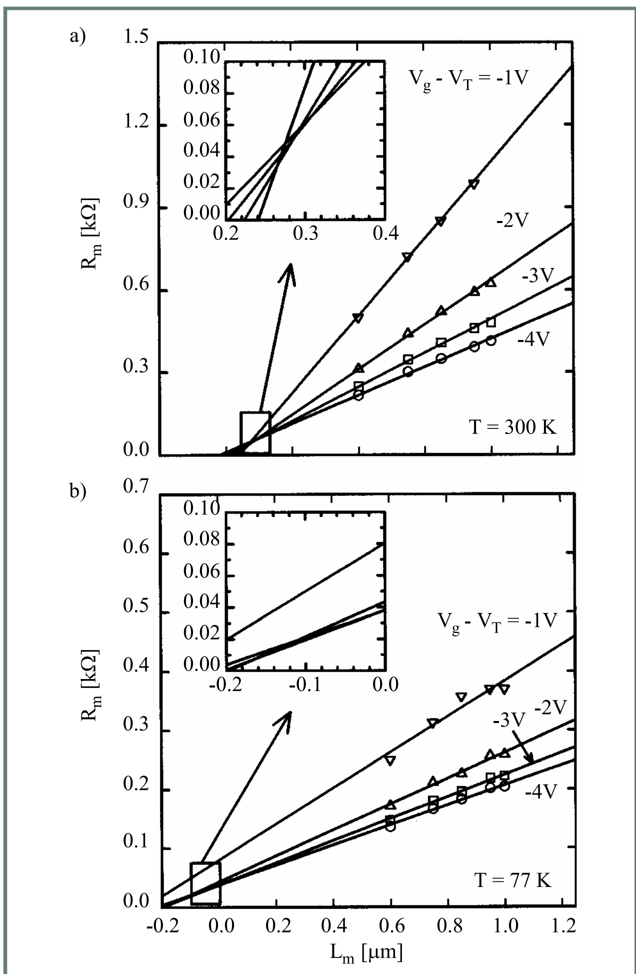

Fig. 7. The total channel resistance versus mask channel length for various gate voltages at (a) 300 K and (b) 77 K. The symbols are the measured data and the lines are the fittings to data using straight lines.

plots of p-channel devices at temperatures of 300 K and 77 K, respectively. At 300 K, the unique intersection of the straight lines yields $\Delta L_{eff} \approx 0.3$ μm on the x axis and $R_{DS} \approx 60\ \Omega$ on the y axis. On the other hand, the analogous procedure at 77 K yields no unique intersection of the straight lines, and even if the intersection of three of lines is used, a negative ΔL_{eff} is obtained, which is physically unsound for the conventional MOSFET under consideration.

The Terada method may also fail [47] at room temperature for MOSFETs having a relatively high doping concentration

in the substrate. The failure of the Terada method can be attributed to the following assumptions used in developing the method: 1) the drain and source series resistances are independent of the gate bias; 2) V_T used in the method, and thus L_{eff} extracted, does not account for the effects of the series resistances; 3) $V_g \approx V_{GS}$; and 4) the free-carrier velocity saturation effect in the channel is negligible.

Recently, Terada and co-workers presented an improved extraction method [48], which proposed that ΔL_{eff} and R_{DS} extracted using their original method can be a function of the gate voltage due to the fact that the R_m versus L_m plot possesses several intersections of the straight lines. From these different intersections, a statistical approach is then used in their new method to determine the correct and unique ΔL_{eff} and R_{DS} based on the concept that the most accurate ΔL_{eff} and R_{DS} give rise to the least dependence of these two parameters on the gate bias.

4.1.2. Shift and ratio method

The shift and ratio (S & R) method, developed by Taur et al. [32], is based on the total channel resistance, which was given in Eq. (28) and can be rewritten as

$$R_m = R_{DS} + \left(L_m - \Delta L_{eff}\right) f\left(V_g - V_T\right) , \qquad (29)$$

where $f(V_g - V_T)$ is a general function describing the MOSFET behavior. The S & R method extracts ΔL_{eff} using at least two devices (i.e., ith and jth devices) having different mask channel lengths (i.e., L_{mi} and L_{mj}, one of which needs to be long), and the following functions S_i and S_j:

$$S_i \equiv \frac{dR_{mi}}{dV_g} \approx \left(L_{mi} - \Delta L_{eff}\right) \frac{df\left(V_g - V_{Ti}\right)}{dV_g} \qquad (30)$$

and

$$S_j \equiv \frac{dR_{mj}}{dV_g} \approx \left(L_{mj} - \Delta L_{eff}\right) \frac{df\left(V_g - V_{Tj}\right)}{dV_g} , \qquad (31)$$

where the assumption that R_{DS} and ΔL_{eff} are independent of V_g has been used. According to these equations, curves of S_i and S_j versus V_g can be constructed. To extract ΔL_{eff}, the S_i curve is first translated („shift”) horizontally in the V_g axis with respect to the S_j curve by the amount

$$\Delta V_{ij} \equiv \left(V_{Ti} - V_{Tj}\right) , \qquad (32)$$

because the threshold voltage is a function of the channel length. Also, the S_i curve is magnified („ratio”) in the S axis, with respect to the curve S_j, by a factor

$$r_{ij} \equiv \frac{L_{mi} - \Delta L_{eff}}{L_{mj} - \Delta L_{eff}} = \frac{S_i\left(V_g - \Delta V_{ij}\right)}{S_j\left(V_g\right)} . \qquad (33)$$

The key here is to find the ΔV_{ij} value for which r_{ij} is a constant. Taur et al. [32] solved ΔV_{ij} and r_{ij} using a statistical approach. Once the values of V_{ij} and r_{ij} are found, L_{eff} can be calculated from Eq. (33).

We have applied this method to n-channel MOSFETs with a channel width of 20 μm and mask channel lengths of 1.75, 2.00 and 20 μm. An increment of 100 mV for the gate voltage and drain voltage of 100 mV were used in the measurements. Figure 8 shows the S function versus V_g characteristics.

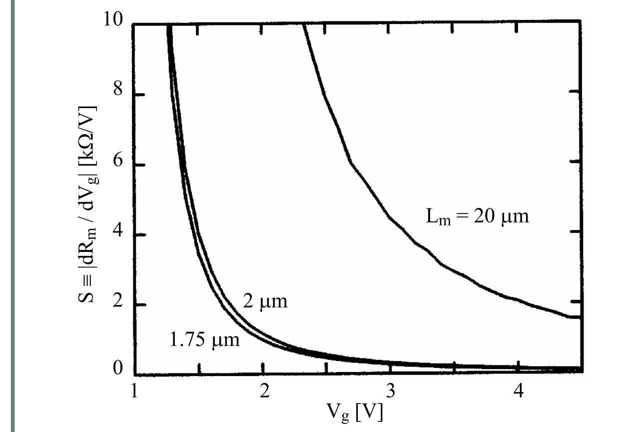

Fig. 8. The function S versus the gate voltage for MOSFETs with three different mask channel lengths.

The problem of a translation and a magnification in the original S & R method can be changed [18] to a more straightforward dual-translation problem by using two new functions:

$$T_i \equiv \ln\left(|S_i|\right) , \ T_j \equiv \ln\left(|S_j|\right) . \qquad (34)$$

Figure 9a shows the T function versus V_g characteristics obtained from the experimental data.

Then, using the plots for $L_m = 2$ and 20 μm and different values of □V_{ij}, we calculated the corresponding ΔT_{ij} by shifting the plot and carrying out a numerical fit for the range 2 V $< V_g <$ 5 V. The range $V_g <$ 2 V was not included in order to avoid moderate and weak inversion. Figure 9b presents ΔT_{ij} and the corresponding error versus □V_{ij} using the 2- and 20- μm MOSFETs. Since the error is minimal at about □$V_{ij} = 0.07$ V, the solution is $\Delta T_{ij} = 2.58$, and we obtained $L_{eff} = 0.53$ μm.

While it is possible to eliminate the translation in the T axis by differentiating T_i with respect to V_g, it is better not to do so because such a mathematical manipulation would increase the effect of the noise on the experimental data.

We conclude that the S & R method is more complex in extracting L_{eff} than the Terada method. In addition, such a method may not be accurate in some cases due to the use of following assumptions: 1) the series resistances are assumed independent of the gate bias; 2) $V_g \approx V_{GS}$; and 3) the effect of drift velocity saturation along the channel is assumed negligible.

4.1.3. Conductance method

This method [36] accounts for the carrier drift velocity saturation effects [4–6] and has been used to extract the parameters at both room and liquid nitrogen temperatures.

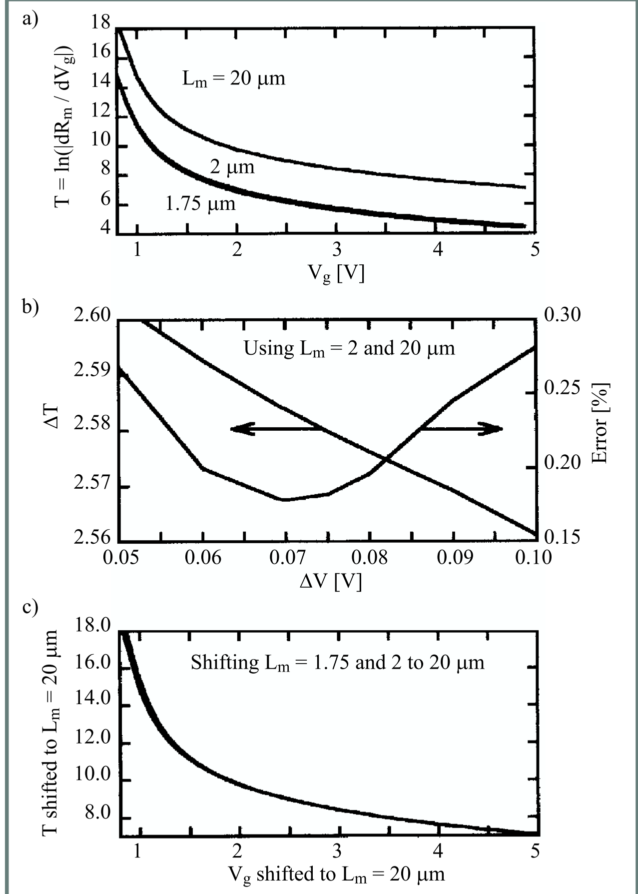

Fig. 9. (a) The function T versus the gate voltage for MOSFETs with three different mask channel lengths. (b) Shift in T versus the shift in gate bias and the corresponding error. (c) The plots for $L_m = 1.75$ and 2 µm shifted to the plot for $L_m = 20$ µm.

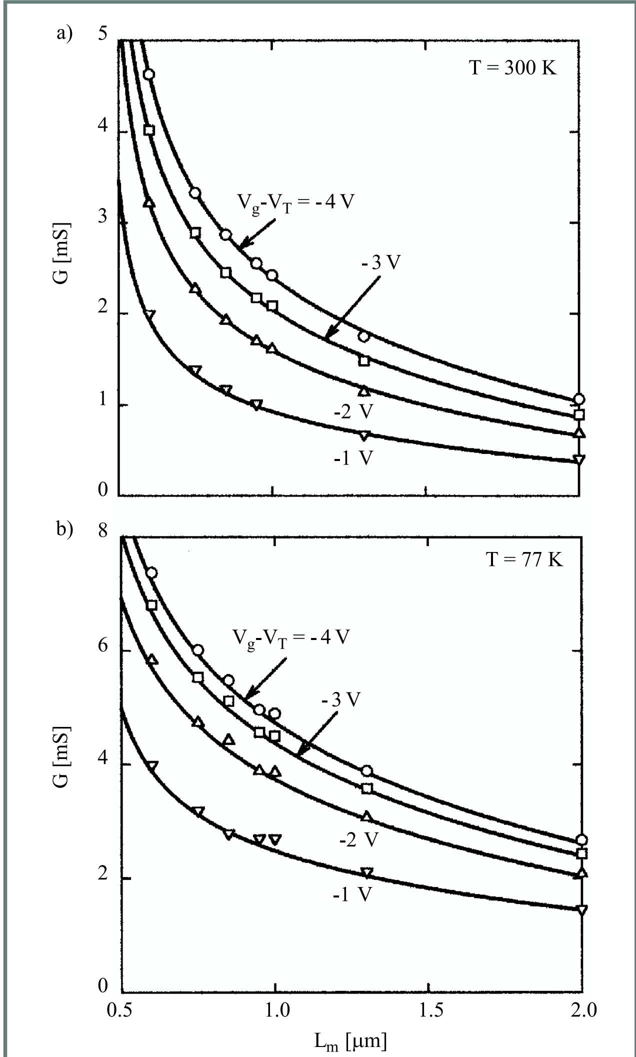

Fig. 10. Total channel conductance versus mask channel length for various gate voltages at (a) 300 K and (b) 77 K. The symbols are the measured data and the lines are the fittings to data using the conductance method.

Following the model proposed by Shur et al. [6, 49] and using the strong inversion condition and the approximation $V_g \approx V_{GS}$, the drain current can be expressed as

$$I_D = \frac{W \mu_{lf} C_o (V_g - V_T) V_{DS}}{L_{eff}\left(1 + \dfrac{V_{DS}}{V_{SATE}}\right)} , \quad (35)$$

where μ_{lf} is the effective free-carrier mobility for low field and V_{SATE} is an effective voltage which accounts for the carrier velocity saturation effect. After some algebraic manipulations and approximations [36], the conductance is obtained

$$G = \frac{1}{2R_{DS}} + C_l L_{eff}^{1/3} + C_2 L_{eff}^{-2/3} , \quad (36)$$

where C_1 and C_2 are two constants governed by the following relationship:

$$\frac{C_2}{C_1} \approx -G_o R_{DS} L_{mo} , \quad (37)$$

where L_{mo} is the mean mask channel length of all the MOSFETs considered, and G_o is the mean conductance of these devices. Equation (36) allows one to determine R_{DS} and L_{eff} from the data of G as a function of V_g and L_m.

Figures 10a and 10b show the conductance versus mask channel length obtained from measurements (symbols) and from fitted model calculations (lines) for various gate voltages at 300 K and 77 K, respectively.

The extracted values of the total series resistance (i.e., drain and source series resistances) at 300 and 77 K are illustrated in Fig. 11. It is shown that R_{DS} decreases with increasing gate voltage (i.e., from 100 Ω to 80 Ω at 77 K, and from 270 Ω to 180 Ω at 300 K).

The extracted values of the effective channel length reduction, $\Delta\Box L_{eff} = L_m - L_{eff}$, for the two temperatures are shown in Fig. 12. The results suggest that ΔL_{eff} depends weakly on V_g but strongly on temperature.

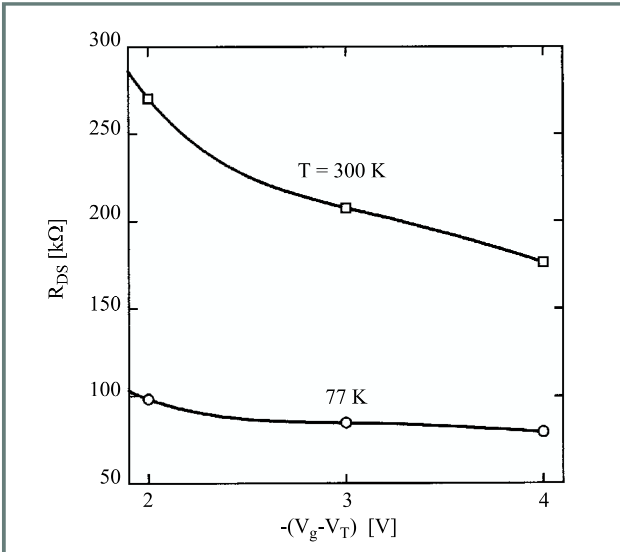

Fig. 11. Extracted values of the total drain and source series resistance versus gate voltages for two temperatures.

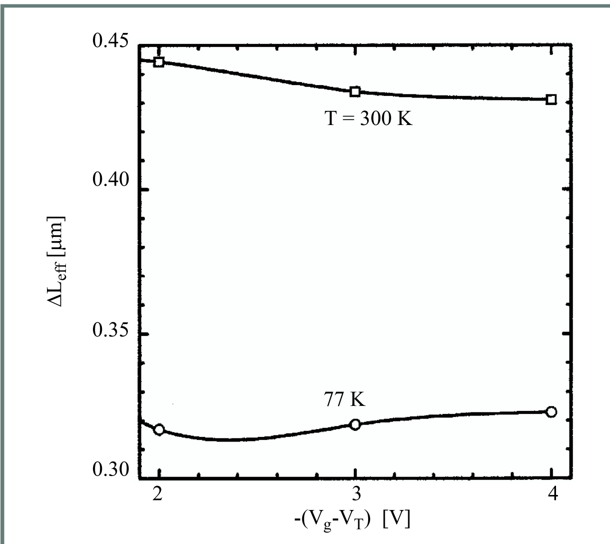

Fig. 12. Extracted values of the difference between the mask channel length and the effective channel length (i.e., $\Delta\Box L_{eff} = L_m - L_{eff}$) for two different temperatures.

4.1.4. Fikry et al. method

The method by Fikry et al. [50] also accounts for the carrier velocity saturation effect in the channel and uses the assumption of $V_g \approx V_{GS}$. The velocity saturation effect is imbedded in the following free-carrier mobility model:

$$\mu = \frac{\mu_o}{\left(1+\Theta\left(V_g - V_T\right)\right)\left(1+\dfrac{\mu_o V_d}{L_{eff}\nu_{sat}}\right)}, \qquad (38)$$

where μ_o is the low-field mobility, Θ is the mobility degradation factor due to the vertical field, and ν_{sat} is the saturation velocity of the carriers.

The following function is then used:

$$\frac{I_D}{g_m^{1/2}} = s^{-1/2}\left(V_g - V_T\right), \qquad (39)$$

where g_m is the transconductance and

$$s = \frac{L_m - \left(\Delta L_{eff} - \dfrac{\mu_o V_d}{\nu_{sat}}\right)}{W\mu_o C_o V_d}. \qquad (40)$$

The above two equations were derived by combining Eqs. (24), (26) and $V_g \approx V_{GS}$. The values of V_T and s are extracted by plotting $I_D/g_m^{1/2}$ versus V_g. Then, the plot of s versus L_m allows one to obtain μ_o from its slope and $\left(\Delta L_{eff} - \mu_o V_d/\nu_{sat}\right)$ from its intercept to the L_m axis. Thus, ΔL_{eff} can be determined from $\left(\Delta L_{eff} - \mu_o V_d/\nu_{sat}\right)$, provided the value of ν_{sat} is calculated from the following equation describing transconductance of the device biased in the saturation region:

$$g_m = W C_o \nu_{sat}. \qquad (41)$$

Alternatively, ΔL_{eff} can also be obtained from the extrapolation of $\left(\Delta L_{eff} - \mu_o V_d / \nu_{sat}\right)$ versus V_d plot, which is a straight line, to the y axis where V_d is zero. Simulations indicate [18] that this method is sensitive to the bias condition and that a small voltage should be used to make sure the MOSFET operated in the linear region.

Figure 13a shows the MEDICI simulation results of $I_D / g_m^{1/2}$ versus V_g for several mask channel lengths and $V_d = -50$ mV. The linear extrapolation of the curves to the V_g axis gives V_T. The corresponding plot of s versus L_m, illustrated in Fig. 13b, yields $W\mu_o C_o V_d = 0.99 \cdot 10^{-6}$ µm/Ω from its slope and $\left(\Box L_{eff} - \mu_o V_d / \nu_{sat}\right) = -0.0134$ µm from its intercept to the L_m axis. Then, using $C_o = 3.45 \cdot 10^{-7}$ F/cm^2, $|V_d| = 0.05$ V, $W = 1$ µm and $\nu_{satn} = \nu_{satp} = 10^6$ cm/s, we obtain $\mu_o = 57$ cm^2/V.s and $\Delta\Box L_{eff} = 0.015$ µm from the Fikry method.

If a larger bias condition of $V_d = -100$ mV is used in simulation, then $W\mu_o C_o V_d = 1.94 \cdot 10^{-6}$µm/Ω, $\left(\Box L_{eff} + -\mu_o V_d / \nu_{sat}\right) = -0.053$ µm, $\mu_o = 56$ cm^2/V.s and $\Delta\Box L_{eff} = 0.042$ µm. The fact that different V_d gives rise to different $\Delta\Box L_{eff}$ suggests that the method is sensitive to the bias condition and that a small voltage should be used to make sure the MOSFET operated in the linear region.

An alternative way to extract $\Delta\Box L_{eff}$ is extrapolating the $\left(\Box L_{eff} - \mu_o V_d / \nu_{sat}\right)$ versus V_d plot to the point of $V_d = 0$ (i.e., y axis), as illustrated in Fig. 14, which gives $\Delta\Box L_{eff} = 0.026$ µm.

4.1.5. Nonlinear optimization method

The nonlinear optimization method [51, 52] extracts ΔL_{eff} based on optimization techniques applied to current-voltage characteristics. This optimization technique, which are frequently implemented using statistical program like Splus [53], present two main advantages: (1) the consistent determination of all the parameters of the model because

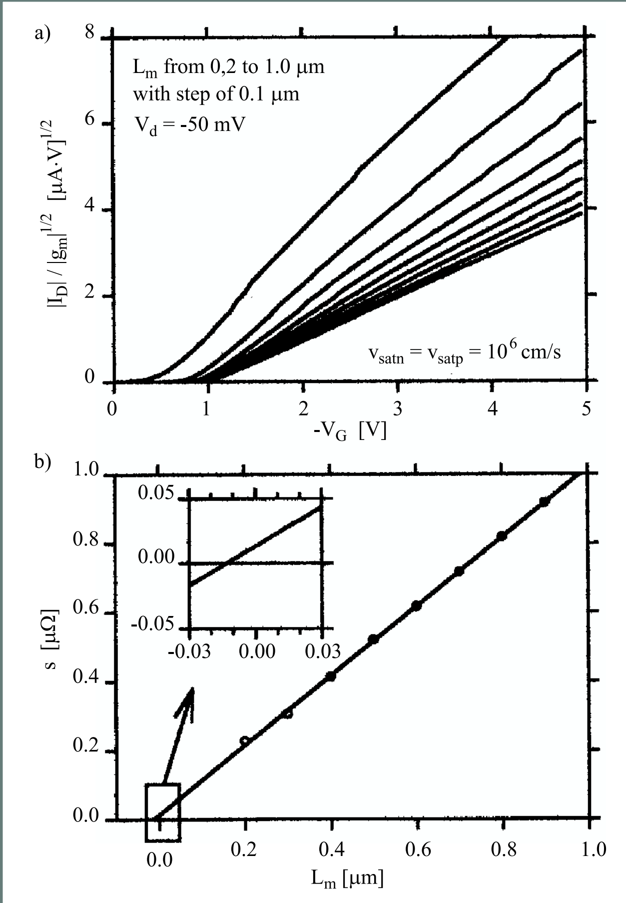

Fig. 13. (a) Calculated values of $I_D / g_m^{1/2}$ versus V_g for several mask channel length and $V_d = -50$ mV. The slopes of these approximate straight lines give the values of s. (b) Calculated values of s versus L_m. The slope of this approximate straight line yields $W\mu_o C_o^a V_d = 0.99 \cdot 10^{-6}$ μm/Ω and the intercept of the line at the L_m axis gives $(\square L_{eff} - \mu_o V_d / v_{sat}) = -0.0134$ μm.

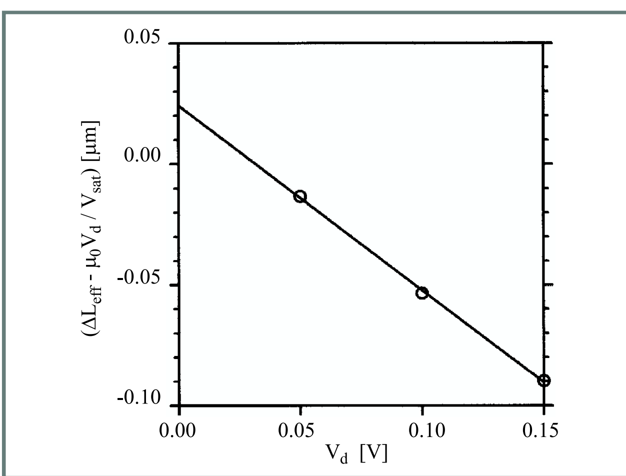

Fig. 14. Extracted values of $(\square L_{eff} - \mu_o V_d / v_{sat})$ (open circles) for three different V_d. The intercept of the straight line passing through these points at the vertical axis (i.e., $V_d = 0$) yields $\square L_{eff} = 0.026$ μm.

of the simultaneous extraction; and (2) the reduction of the effects of the noise on the experimental data due to the optimization techniques. There are two main disadvantages, however: (1) nonphysical parameters values can be obtained because of the pure fitting scheme, and (2) the requirement of a long computational process.

4.2. Capacitance-voltage method

To avoid the effect of the parasitic drain and source series resistances, which is a main mechanism causing the difficulty in the I-V methods, various methods have been developed to extract ΔL_{eff} from the capacitance-voltage characteristics (i.e., C-V methods) [39–44]. The main drawback of the C-V methods is the requirement of high resolution equipment to measure the small capacitances in MOSFETs. Moreover, it is somewhat difficult to correlate the C-V data and L_{eff}.

Among the various C-V extraction methods we find: 1) Sheu's method [40], which is based on the crude assumption that the capacitance between the inverted channel and the substrate is negligible [6]; 2) Vitanov's method [41], which is based on the wrong assumption that the capacitances for the source-body and drain-body junction regions can be neglected; 3) Lee's method [42], which uses various devices (i.e., various L_m) and the determination of the capacitance at which the C-V curves for different L_m start to deviate from each other; 4) Guo's method [43], which is similar to Leet's method; and 5) Latif's method [44] which accounts for capacitances that the Sheu-Ko's method neglected.

4.3. Simulation-based method

4.3.1. Narayanan et al. method

Narayanan et al. [30] estimated the value of ΔL_{eff} through the means of physical insight obtained from device simulation. We show in Fig. 15 the hole concentration at the interface for various V_g for a p-channel device. Based on the concept that the effective channel is the region in which the free-carrier concentration is controlled by the gate voltage. It was then suggested that the two points where the hole concentrations for different V_g start to deviate from each other (indicated by arrows in Fig. 15) are the edges of the effective channel. Such a definition is more accurate because it accounts for the transition regions between the deep channel and source/drain regions and because it is not affected by the gate voltage.

4.3.2. Niu et al. method

Niu et al. [45] also proposed a method to determine L_{eff} through the means of physical insight obtained from simulations. While Niu et al. agreed with the physical reasoning of Narayanan's method [30], they felt that it is somewhat subjective and arbitrary to determine the effective channel based on the two points where the free-carrier concentrations for different V_g start to deviate from each other.

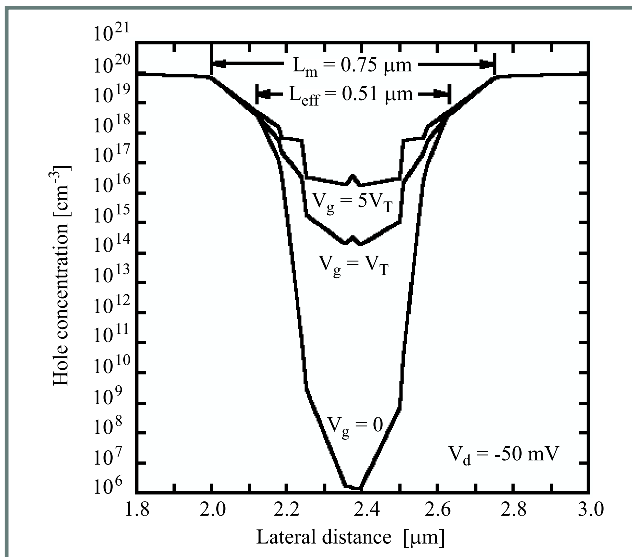

Fig. 15. Hole concentration at the interface of the p-channel MOSFET with $L_m = 0.75$ µm.

Niu's method is based on the assumption that the diffusion current is negligible for a MOSFET biased in strong-inversion. Therefore, the following behavior should be found along the effective channel: 1) the inversion carrier concentration is nearly constant; 2) the lateral electric field (i.e., $-d\Psi/dx$) is also nearly constant to keep a constant drift current; 3) the electrostatic potential Ψ varies linearly with respect to the lateral distance x; and 4) the second derivative of the electrostatic potential with respect to x should be zero (i.e., $d^2\Psi/dx^2 = 0$). Then, Niu proposed that the edges of the effective channel should be defined at the points where $d^2\Psi/dx^2$ are maximum.

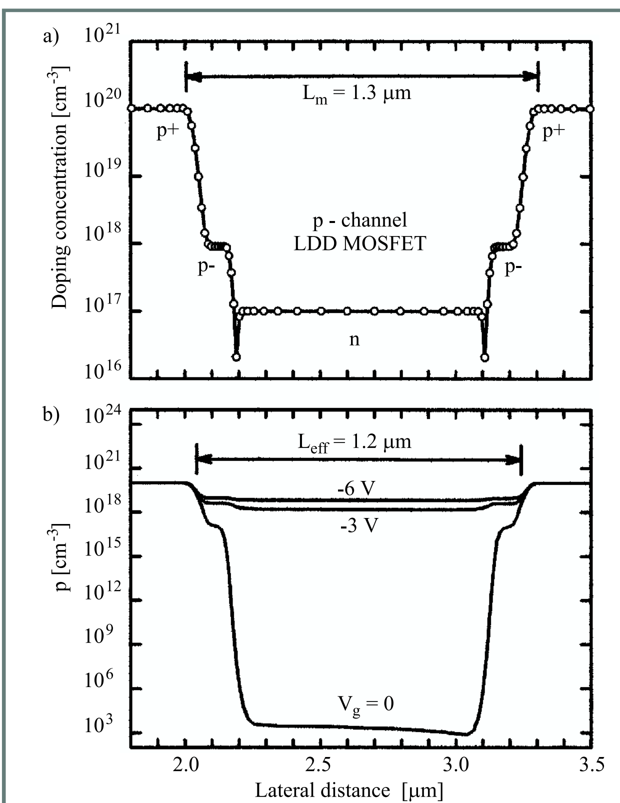

Fig. 16. (a) Impurity doping concentration at the Si-SiO$_2$ interface along the channel of the simulated LDD MOSFET with $L_m = 1.3$ µm. (b) Hole concentration at the interface of the MOSFET for various gate biases.

Figure 16a shows the doping profile along the channel at the interface, and the inversion free-carrier density simulated for different gate voltages are illustrated in Fig. 16b. Based on the Narayanan's method, L_{eff} is found to be about 1.2 µm, and the determination of the boundaries of the effective channel is somewhat subjective because the precise points where the curves start to deviate from each other are not very clear.

Figures 17(a)–(c) show Ψ, $d\Psi/dx$ and $d^2\Psi/dx^2$, respectively, at the interface along the channel for $V_g = -3$ V and $V_d = -0.05$ V. We see in Fig. 17a that Ψ varies approximately linearly with respect to x along the effective channel, but there are two different slopes because of the presence of the LDD regions. Four positive peaks and two negative peaks for $d^2\Psi/dx^2$ are shown in Fig. 17c.

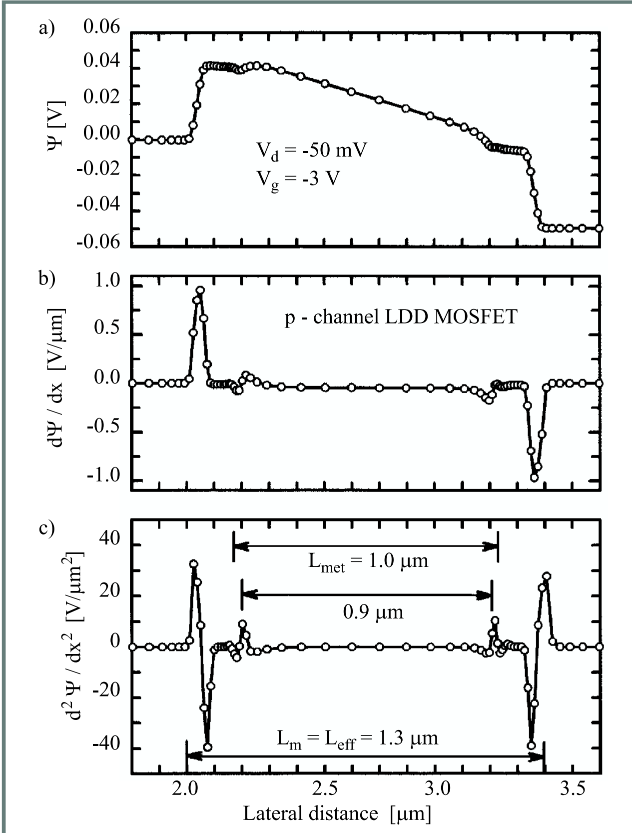

Fig. 17. (a) Electrostatic potential Ψ, (b) first derivative of the electrostatic potential with respect to x (i.e., $d\Psi/dx$), and (c) second derivative of the electrostatic potential with respect to x (i.e., $d^2\Psi/dx^2$) at the interface of the MOSFET with $L_m = 1.3$ µm.

Using the two closest positive peaks to define the effective channel, one will obtain a value of 0.9 µm. This value is incorrect because it is smaller than $L_{met} = 0.93$ µm. A more

reasonable value of $L_{eff} = 1.3\ \mu$m is obtained by using the two farthest positive peaks.

4.4. Comparison of various extraction methods

The Terada-Muta I-V method yielded a value for the effective channel length consistent with that determined from the simulation-based method [30] based on the physics that L_{eff} is the length of a channel region in which the inversion free-carrier density is controlled by the gate voltage. The same effective channel length has also been extracted from the S & R I-V method. In contrast, the C-V methods yield an effective channel length close to L_{met}.

5. Extraction of drain and source series resistance

The extraction of the individual values of the source and drain series resistances require either the knowledge of their sum $(R_D + R_S)$ and difference $(R_D - R_S)$, or the ability to extract the two parameters separately. In this section, we will deal mainly with the extraction of $(R_D - R_S)$.

The most widely method to extract the total drain and source series resistance $(R_D + R_S)$ was presented independently by Terada and Muta [33] and by Chern et al. [34] almost twenty years ago. Several other methods [52, 54–59] have been developed recently.

It is a common practice to assume that the parasitic resistances associated with the drain and source regions of MOSFETs are approximately equal to each other, $R_D \approx R_S$. Therefore, knowing $(R_D + R_S)$, we obtain $R_S \approx R_D \approx (R_S + R_D)/2$. However, this assumption becomes invalid when the drain and source regions of the device are not totally symmetrical. Such an asymmetry results in a difference in the drain and source resistances $(R_D - R_S)$ and can affect considerably the current-voltage characteristics of MOSFETs.

The difference in the drain and source resistances arises mainly from processing, layout, and/or electrical stressing, and it becomes more prominent in the case of deep-submicron devices. This is because the relative importance of the parasitic resistances over the intrinsic components is increased as the geometry of the device shrinks. Previous numerical simulations [57, 60] indicate that the drain and source resistance asymmetry is originated mainly from the difference in the drain and source contact resistances, and not from the gate misalignment, nor from the difference in source and drain doping densities.

An approach frequently used for extracting $(R_D - R_S)$ consist on performing measurements of an MOS device, first connected in the „normal configuration" in which the source and body are grounded, and then measuring it again in the „inverted configuration" in which the source and drain terminals are interchanged, as shown in Figs. 18a and 18b, respectively. It is important to point out that the intrinsic and extrinsic body voltage are related by

$$V_{BS} = V_{bs} - I_d R_S \,. \tag{42}$$

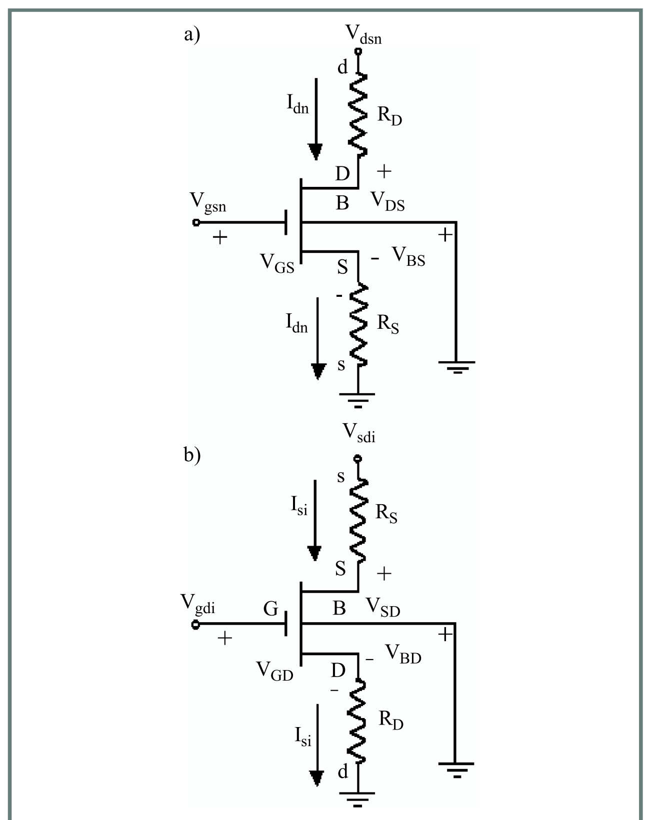

Fig. 18. (a) MOSFET in normal mode of operation with the source and body grounded, and (b) MOSFET in inverse configuration with the drain and body grounded.

Two extraction methods, namely the reciprocal transconductance method and gate-voltage shift method, have been developed based on this approach and are presented below.

5.1. Reciprocal transconductance method

The difference between the drain and source resistances, $(R_D - R_S)$, can be extracted from the extrinsic gate transconductance of a single MOSFET measured under saturation operation at the same drain to source voltage but two different configurations. First, the extrinsic gate transconductance g_{mn} for the normal mode of configuration is measured from the I_{dn} versus V_{gsn} characteristics in the saturation region (i.e., the subscript n represents the normal mode of configuration in which the source and body are grounded (Fig. 18a). This transconductance is given by

$$g_{mn} = \frac{\partial I_{dn}}{\partial V_{gsn}} \,. \tag{43}$$

Second, the gate transconductance g_{mi} for the inverse mode of configuration is measured from the I_{si} vs. V_{gdi} characteristics in the saturation region, (i.e., where subscript i

represents the inverse mode of configuration in which the source and drain functions are interchanged (Fig. 18b). Analogous to Eq. (43), such a transconductance is

$$g_{mi} = \frac{\partial I_{si}}{\partial V_{gdi}} . \tag{44}$$

It should be noted that the intrinsic variables are the same for both modes of configuration, and only R_S and R_D asymmetry is present in the device. After some algebraic manipulations [18, 20, 60–65] we obtain:

$$\left(R_D - R_S\right) = \frac{\frac{1}{g_{mi}} - \frac{1}{g_{mn}}}{1+\frac{g_{b0}}{g_{m0}}} , \tag{45}$$

where g_{b0} and g_{m0} are the intrinsic body and gate transconductance in the normal mode.

We stress that the body effect has been included in the denominator of Eq. (45) by retaining the intrinsic body transconductance.

We conclude from Eq. (45) that, in addition to measuring the normal and inverse extrinsic gate transconductances in saturation, it is necessary to know the ratio of the intrinsic body transconductance to the intrinsic gate transconductance (i.e., g_{b0}/g_{m0} term in the denominator of Eq. (45)) before $(R_D - R_S)$ can be determined. Three different procedures [18, 20, 61–66] to calculate this term have been developed based on adding external resistances and measuring gate transconductances.

5.2. Gate-voltage shift method

This method is also based on measuring a single transistor when it is connected alternatively in the normal and inverse configurations [20, 64, 65]. The difference is that, instead of measuring the difference between normal and inverse reciprocal gate transconductances, it is based on measuring the shift of the gate voltage needed to maintain the same magnitude of drain current when the device is connected in the inverse and normal configurations. Consider a MOSFET in the normal configuration, with the source and body grounded, and also in the inverse configuration, with the drain and source interchanged. The drain current in the normal configuration, can be expressed as a general function of the intrinsic voltages as

$$I_{dn} = f\left[\left(V_{GS} - V_{Tn}\right), V_{DS}\right] , \tag{46}$$

where f is a function defined by a particular MOSFET model, V_{Tn} is the threshold voltage in the normal configuration, and the body voltage dependence has been implicitly incorporated. The function f does not make any other *a priori* assumptions as to the model describing the relationship between drain current and applied voltages. The intrinsic gate-to-source and drain-to-source voltages can be expressed in terms of their extrinsic counterparts as

$$V_{GS} = V_{gsn} - I_{dn} R_S \tag{47}$$

and

$$V_{DS} = V_{dsn} - I_{dn}\left(R_S + R_D\right) , \tag{48}$$

where V_{gsn} and V_{dsn} represent the extrinsic gate-source and drain-source voltages, respectively, in the normal configuration. In a similar manner, the source current in the inverse configuration is given by

$$I_{si} = f\left[\left(V_{GD} - V_{Ti}\right), V_{SD}\right] , \tag{49}$$

where V_{Ti} is the threshold voltage in the inverse configuration, and V_{GD} and V_{SD} are the intrinsic gate-drain and source-drain voltages, respectively. These voltages can be related to their extrinsic counterparts by

$$V_{GD} = V_{gdi} - I_{si} R_D \tag{50}$$

and

$$V_D = V_{sdi} - I_{si}\left(R + R_D\right) , \tag{51}$$

where V_{gdi} and V_{sdi} are the extrinsic gate-drain and source-drain voltages, respectively, in the inverse configuration. If the device in both configurations is biased with the same source-drain voltage (i.e., $V_{sdi} = V_{dsn}$) and V_{gdi} is adjusted until the source current in the inverse configuration is equal to that in the normal configuration (i.e., $I_{si} = I_{dn} = I_d$), then the normal and inverse intrinsic gate voltage overdrive must be the same:

$$\left(V_{GS} - V_{Tn}\right) = \left(V_{GD} - V_{Ti}\right) . \tag{52}$$

Substituting Eqs. (47) and (50) into Eq. (52) yields

$$I_d\left(R_D - R_S\right) = \left(V_{gdi} - V_{gsn}\right) - \left(V_{Ti} - V_{Tn}\right) . \tag{53}$$

The term $(V_{Ti} - V_{Tn})$ in the above equation is small, when the device is biased in the linear region, because $(V_{DB} + -V_{SB})$ is small. Therefore it can be approximated by the first term of its Taylor series expansion as

$$\left(V_{Ti} - V_{Tn}\right) \approx I_d\left(R_D - R_S\right) \frac{dV_T}{dV_{SB}} . \tag{54}$$

Combining Eq. (53) into Eq. (54) gives

$$\left(R_D - R_S\right) = \frac{\left(\frac{V_{gdi} V_{gsn}}{I_d}\right)}{1 + \frac{dV_T}{dV_{SB}}} , \tag{55}$$

where the dependence of the threshold voltage on the source-to-body voltage V_{SB} is accounted for by the term $(1 + dV_T/dV_{SB})$ in Eq. (55).

6. Conclusion

We have presented an overview of the modeling of long-channel bulk MOSFET as a particular case of the long-channel SOI. We have reviewed, compared and scrutinized various methods to extract the threshold voltage, the effective channel and the individual values of drain and source resistances. We have stressed the implicit assumptions and limitations of each method and we have proposed variations in order to improve them.

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Invited paper

Direct extraction techniques of microwave small-signal model and technological parameters for sub-quarter micron SOI MOSFETs

Michël Goffioul, Danielle Vanhoenacker, and Jean-Pierre Raskin

Abstract — Original extraction techniques of microwave small-signal model and technological parameters for SOI MOSFETs are presented. The characterization method combines careful design of probing and calibration structures, rigorous in situ calibration and a powerful direct extraction method. The proposed characterization procedure is directly based on the physical meaning of each small-signal model element. Knowing the qualitative small-signal behavior of each model parameter versus bias conditions, the high frequency equivalent circuit can be simplified for extraction purposes. Biasing MOSFETs under depletion, strong inversion and saturation conditions, certain technological parameters and microwave small-signal elements can be extracted directly from the measured S-parameters. These new extraction techniques allow us to understand deeply the behavior of the sub-quarter micron SOI MOSFETs in microwave domain and to control their fabrication process.

Keywords — microelectronics, microwave devices, SOI MOSFET.

1. Introduction

The boom of mobile communications leads an increasing request of low cost and low power mixed mode integrated circuits. Maturity of silicon-based technology and recent progresses of MOSFET's microwave performances [1–4], explain silicon success as compared to III-V technologies. Silicon-on-insulator-based MOSFETs are very promising devices for multigigahertz applications. Thin-film SOI MOSFETs offer indeed interesting low-voltage performances, higher speed and increased integration density, all with simpler processing than bulk silicon MOSFETs of comparable size [5]. Many recent realizations of logic circuits, memories, and RF circuits [6] have confirmed both the advantages and the viability of thin-film SOI circuits, even in the case of very large systems. To support the development of thin-film SOI circuits, adequate device models and characterization techniques must be available concurrently with the maturation of fabrication processes. In the present paper, we describe direct extraction techniques to accurately characterize sub-quarter micron SOI MOSFETs in the microwave domain. The characterization method combines careful design of probing and calibration structures, rigorous in situ calibration and a powerful direct extraction method. The proposed characterization procedure is directly based on the physical meaning of each small-signal model element. That makes it very useful for controlling the sensitive fabrication steps such as the silicidation process of the gate, source and drain regions. Moreover, due to the physical meaning attributed to each model element through the characterization process, the extracted equivalent circuit is scalable. This last point is crucial for circuits simulation and optimization purposes.

2. Fabrication process

200 nm UNIBOND® wafers with a 400 nm buried oxide were used as the starting material. The silicon thickness was thinned down to 40 nm or 30 nm by a recessed-channel process in the case of the fully depleted (FD) transistors. Gate oxide (4.5 nm) was grown after a LOCOS isolation. A field implant is used to eliminate sidewall leakage. A 200 nm thick polysilicon layer is deposited and patterned by DUV lithography. Source/drain extension implant is followed by formation of a 80 nm spacer oxide after which the source-drain regions are implanted and activated with a 950°C/15 s RTA afterwards. A titanium silicide process is used to reduce the sheet and contact resistances of gate fingers and the elevated 80 nm thick source-drain regions. After the silicide process a gate sheet resistance of about 10 $\Omega/\Box$, instead of 100 $\Omega/\Box$ for a classical doped polysilicon gate, is obtained for a 0.25 μm gate channel length MOSFET. The total S/D series resistance were about 700 $\Omega\mu$m and 1300 $\Omega\mu$m for n- and p-MOSFETs, respectively. The back-end processing includes a three level metal process with tungsten plugs and planarization of intermetal oxides by chemical and mechanical polishing (CMP). SOI MOSFETs composed of 12 gate fingers connected in parallel with various channel lengths (L = 0.25, 0.35, 0.5 and 1 μm) and widths (W = 1, 2, 3.4, 6.6, 9, 15 and 25 μm) were built and measured.

3. Microwave small-signal model

The direct extraction methods developed in the present paper are based on the good knowledge of the measured transistors 3D structure and the physical meaning attributed

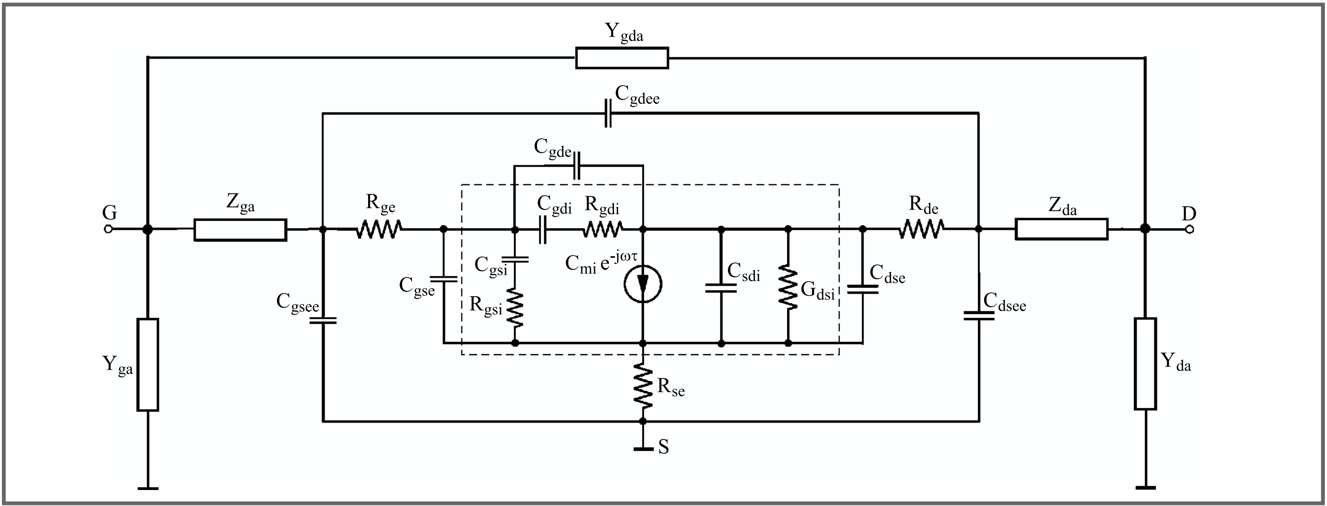

Fig. 1. Small-signal model of a common-source SOI MOSFET.

to the various lumped elements of transistors small-signal equivalent circuit. Figure 1 shows the model used for the common-source SOI MOSFET. According to the physical meaning attributed to the elements, the circuit can be split into three parts:

- Index *i* denotes the intrinsic elements which model the core of the transistor, and are thus dependent on the bias conditions and on the size of the active zone.
- Index *e* denotes the extrinsic elements, which are supposed to be independent of bias, but scale with the active zone.
- Index *a* denotes the shunt and series access parameters caused by the metal connections just outside of (adjacent to) the active zone. The frequency behavior of the series impedances (Z_{ga} and Z_{da}) and shunt admittances (Y_{ga} and Y_{da}) is determined by the propagation characteristics of a coplanar waveguide transmission line (CPW) on SOI substrate. They are constant under normal biasing conditions, and not dependent on the width of the active zone.

Under certain bias conditions, some small-signal elements vanish and then the equivalent circuit presented in Fig. 1 can be simplified. These assumptions can only be done if the physical meaning of each small-signal lumped element of the transistor structure is correctly considered. In the next section, the extraction procedure of technological parameters and microwave small-signal elements based on transistor S-parameters measured under depletion, strong inversion and saturation conditions is explained.

4. Extraction procedure

The main steps of the small-signal model extraction are: the extraction of the CPW feed transmission lines parameters, the determination of the extrinsic parasitic capacitances, the extraction of the extrinsic resistances, and finally, the determination of all intrinsic elements for a given bias point. Following the same philosophy, it has been shown that certain technological parameters such as the effective channel length, the gate, source and drain silicide resistivities and the effective gate oxide thickness can be directly extracted from the measured high frequency S-parameters.

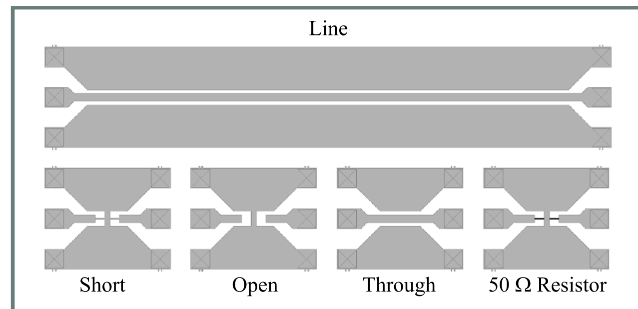

Fig. 2. Calibration kit allowing to perform a TRL calibration and to determine the reference impedance.

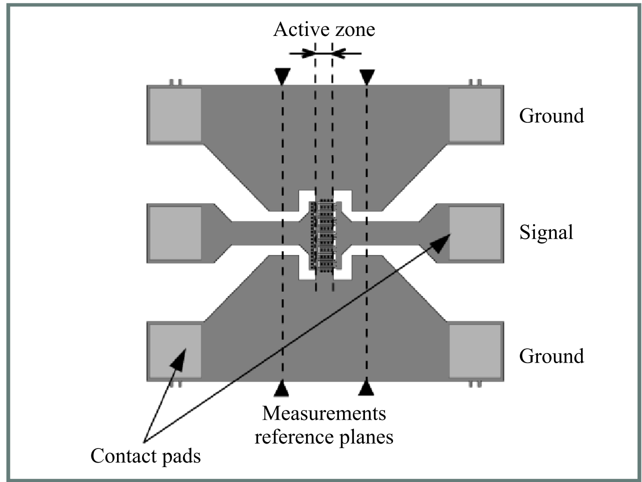

Fig. 3. Top view of on-wafer MOSFET test structure showing the measurements reference planes and the active zone.

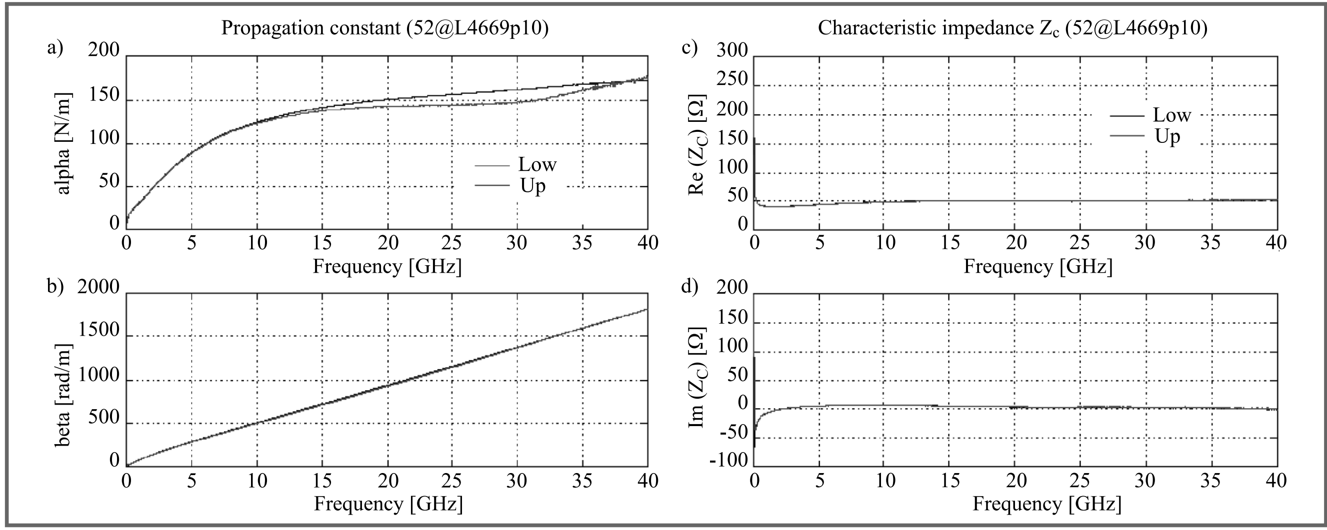

Fig. 4. Extracted complex propagation coefficient ($\gamma = \alpha + j\beta$) (a), (b) and complex characteristic impedance (Z_c) (c), (d) by considering the measured S-parameters of the short line (Up, called „through" in Fig. 2) and the long line (Low, called „line" in Fig. 2) in the calibration procedure.

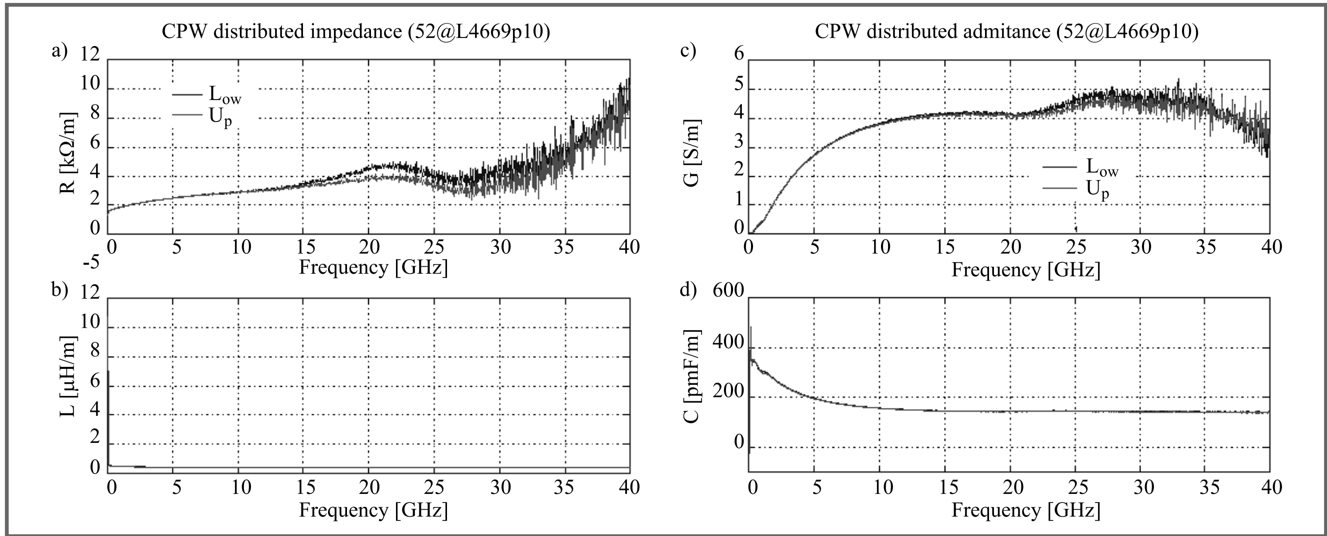

Fig. 5. Extracted series (*R* and *L*) (a), (b) and shunt (*G* and *C*) (c), (d) equivalent parameters per unit length for a CPW line on standard SOI substrate (20 Ωcm).

4.1. Extraction of the CPW feed lines parameters

Using standards implemented on the SOI wafer (Fig. 2), a through-reflect-line (TRL) calibration is performed as described in [7] for defining the S-parameters reference planes close to the input and output of measured transistors. Figure 3 shows the position of the measurements reference planes after calibration. It appears that there is a short residual length of CPW metallic line (approximately 50 µm) at the transistor input and output between the measurements reference planes and the beginning of the transistor active zone. After the extraction of the transmission line characteristics Z_c and γ (Fig. 4) from the measured calibration kit (Fig. 2) built on SOI substrate, the series and shunt parameters per unit length of the line are obtained. Figure 5 presents the extracted impedance and admittance values per unit length for a CPW line implemented on standard SOI substrate (20 Ωcm). Knowing the exact distance between the measurements reference planes and the beginning of the transistor active zone (l_{ga} and l_{da}, the CPW line access lengths at the input and output of the transistor, respectively) the residual access lines can be then estimated by:
Series impedances:

$$Z_{ga} = l_{ga}(R + j\omega L) , \quad (1)$$

$$Z_{da} = l_{da}(R + j\omega L) . \quad (2)$$

Shunt admittances:

$$Y_{ga} = l_{ga}(G + j\omega C) , \quad (3)$$

$$Y_{da} = l_{da}(G + j\omega C) . \quad (4)$$

The parasitic admittance Y_{gda} represents mainly the parasitic coupling between gate and drain metallic interconnec-

tions outside the active zone. As explained in [8], Y_{gda} can be extracted from the measured S-parameters for the transistor biased in depletion. It is obtained by the intercept at the origin of the linear regression on measured data points plotted in a two dimensional plane defined by $[W, Y_{12}]$ or $[W, Y_{21}]$, with W being the transistor total width and Y_{ij} the Y-matrix elements of the transistor measured under depletion bias condition $(V_{gs} << V_{th})$ and V_{ds} = 0 V. It is important to note that due to the design of the metallic access CPW lines (high frequency interconnections) this parasitic element is mainly capacitive and has a very small value (around 1 fF).
Using the extracted values $(Z_{ga}, Z_{da}, Y_{ga}, Y_{da}$ and $Y_{gda})$ the residual series and shunt parasitic access elements are withdrawn by simple matrix manipulations.

4.2. Extraction of the extrinsic capacitances

Figure 6 shows the cross-section of a fully depleted SOI MOSFET with its metallic drain and source interconnections. The physical origins of the parasitic extrinsic capacitances indicated in Fig. 1 are multiple.

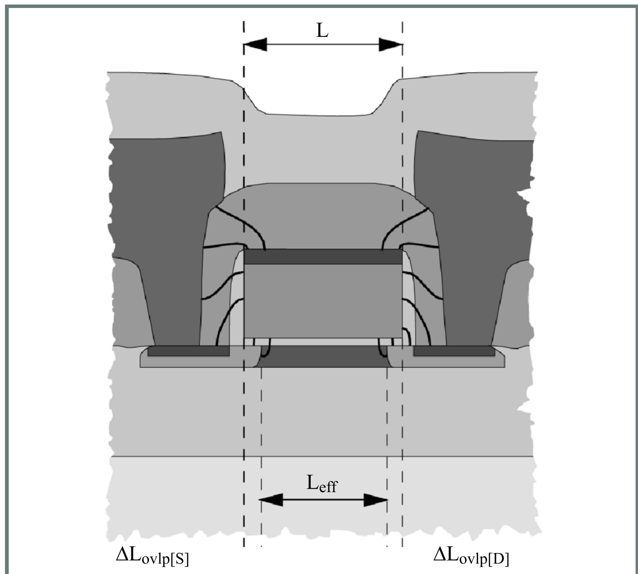

Fig. 6. Cross-section of a fully depleted SOI MOSFET with its metallic drain and source interconnections.

We have the overlap gate-to-drain and gate-to-source capacitances $(C_{gse} = \varepsilon_{ox}\Delta L_{ovlp[S]}/d_{ox}, C_{gde} = \varepsilon_{ox}\Delta L_{ovlp[D]}/d_{ox})$. We can limit these parasitic capacitances by controlling the thermal diffusion of doping atoms from the source and drain regions into the transistor channel. The extrinsic capacitance C_{dse} corresponds to the proximity parasitic capacitance between drain and source diffusion regions. That parasitic capacitance can be quite important for sub-quarter micron MOSFETs.
C_{gsee}, C_{gdee} and C_{dsee} are the extrinsic capacitances due to parasitic couplings between metallic interconnection lines outside the transistor active zone between gate-source, gate-drain and drain-source, respectively. The values of these capacitances are independent with bias conditions and depend on the transistor size and also on the design of the transistor metallic interconnection structure. In order to extract the extrinsic capacitances the transistor S-parameters are measured in deep depletion $(V_{gs} << V_{th})$ and V_{ds} = = 0 V. Under these bias conditions, the equivalent circuit of the MOSFET is simplified, as shown in Fig. 7. As

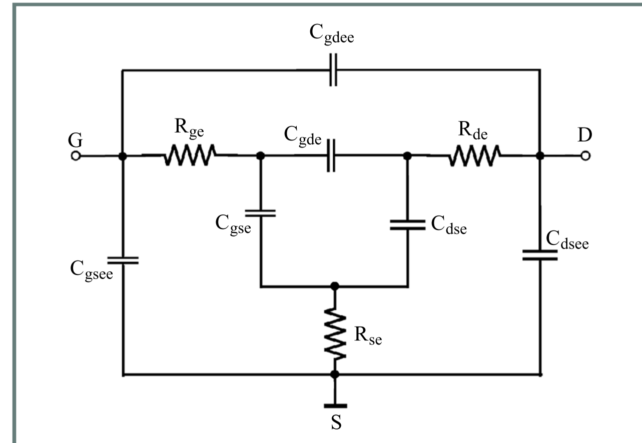

Fig. 7. Simplified small-signal equivalent circuit for a common source SOI MOSFET in deep depletion $(V_{gs} << V_{th})$ and V_{ds} = 0 V.

explained in [9], at relatively low frequencies the effects of the extrinsic resistances can be neglected and therefore, the extrinsic capacitances are directly obtained from the imaginary part of the measured Y-parameters. However, due to the dimension shrinkage of the recent transistors (channel length < 0.25 μm), the parasitic capacitances between transistor fingers and metallic connection vias along the active region of the transistor structure become non-negligible. Because all of those parasitic extrinsic capacitances are connected in parallel with the extrinsic overlap and drain-

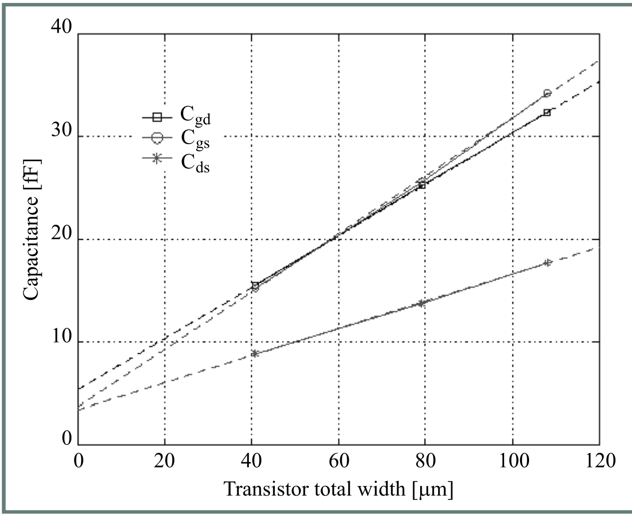

Fig. 8. Evolution of the total extrinsic capacitances measured in deep depletion at V_{ds} = 0 V for various total active zone widths (W).

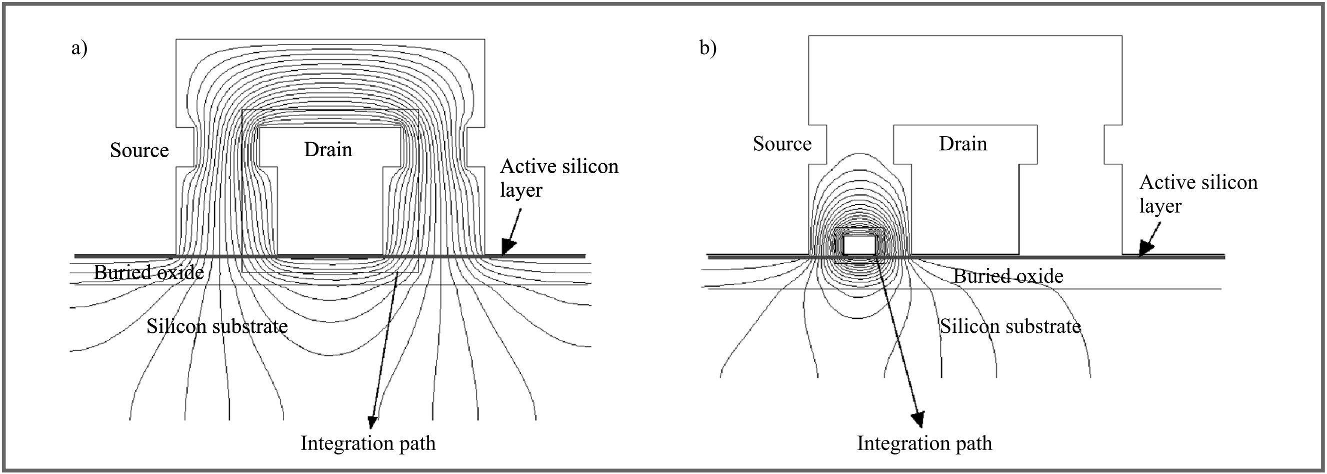

Fig. 9. 2D electrostatic simulations for the estimation of the parasitic source-to-drain (C_{dsee}) (a), gate-to-drain (C_{gdee}) and gate-to-source (C_{gsee}) (b) coupling capacitances.

-to-source proximity capacitances $((C_{gse}, C_{gsee}), (C_{gde}, C_{gdee})$ and $(C_{dse}, C_{dsee}))$ as shown in Figs. 1 and 7, their extraction is not straightforward.

Figure 8 represents the evolution of the total capacitances ($C_{gs} = C_{gse} + C_{gsee}, C_{gd} = C_{gde} + C_{gdee}$ and $C_{ds} = C_{dse} + C_{dsee}$) measured in deep depletion at V_{ds} = 0 V for various total active zone widths (W).

In order to dissociate the different extrinsic capacitances, we have used a 2D electrostatic simulator for estimating the parasitic coupling effects existing between the gate, drain and source metallization levels (C_{gsee}, C_{gdee} and C_{dsee}). Figure 9 shows the equipotential lines calculated by the 2D electrostatic simulation software for two different boundary conditions. The capacitances are obtained by integrating the electric field along the integration path as indicated in the schemes. From the calculated capacitance values C_{gsee}, C_{gdee} and C_{dsee} and the measured imaginary part of Y-parameters (C_{gs}, C_{gd} and C_{ds}) for the transistor biased in deep depletion (Fig. 8), the extrinsic capacitances $C_{gde} (= C_{gd} - C_{gdee}), C_{gse} (= C_{gs} - C_{gsee})$, respectively, the gate-to-drain and gate-to-source overlap capacitances, and $C_{dse} (= C_{ds} - C_{dsee})$, the source-to-drain proximity capacitance, are extracted.

4.3. Extraction of the extrinsic resistances

After removing the parallel extrinsic capacitances (C_{gsee}, C_{gdee} and C_{dsee}) by simple matrix manipulations, we consider the parametric curves defined in a two dimensional plane $[x_1, x_2]$ by $[\mathrm{Re}(Z_{\sigma\pi ij}(\omega)), \mathrm{Re}(Z_{\sigma\pi kl}(\omega))]$, where $\{i, j\} \neq \{k, l\}$, for the transistor biased in saturation ($V_{ds} > V_{gs} - V_{th}$). It has been demonstrated that these curves are straight lines and from their slope and intercept at the origin the extrinsic resistances (R_{ge}, R_{de} and R_{se}) are directly extracted [9]. Figures 10 and 11 represent the parametric plot of resistances in the 0.5÷40 GHz band at $V_{gs} = 1$ V and $V_{ds} = 2$ V for 12 x (6.6/0.35) μm^2 and 10 x (24/0.75) μm^2 SOI n-MOSFETs, respectively. The

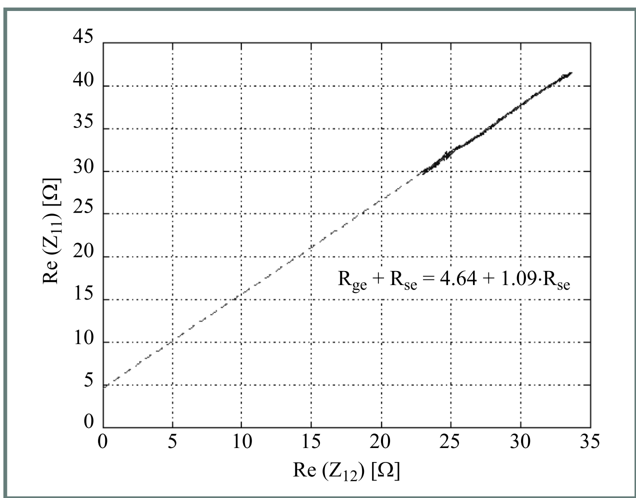

Fig. 10. Parametric plot of resistances in the 0.5÷40 GHz band for 12 x (6.6/0.35) μm^2 SOI n-MOSFET at V_{gs} = 1 V and V_{ds} = 2 V.

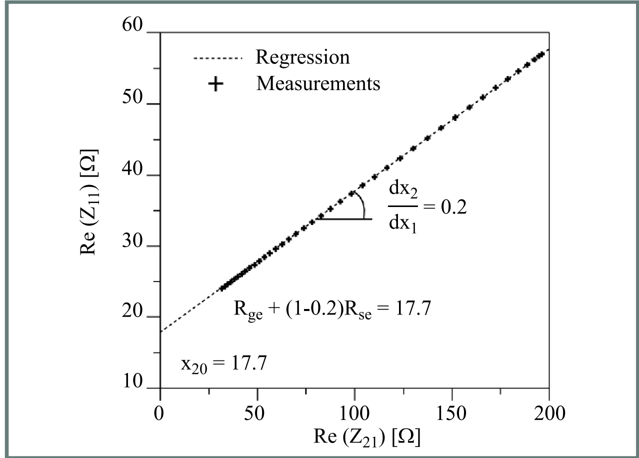

Fig. 11. Parametric plot of resistances in the 0.5÷40 GHz band for 10 x (24/0.75) μm^2 SOI n-MOSFET at V_{gs} = 1 V and V_{ds} = 2 V.

accuracy of the extracted resistance values is related to the precision with which the slope and the intercept at the origin can be determined by linear regression from the measured Z-parameters. By comparison of Figs. 10 and 11, it appears that higher accuracy on the extracted resistance values is reached if the measurements frequency band includes the cut-off frequency of the measured transistor. The current gain cut-off frequency (f_T) for the measured 12 x (6.6/0.35) μm^2 and 10 x (24/0.75) μm^2 SOI n-MOSFETs are 40 and 14 GHz, respectively.

In order to overcome that lack of accuracy on the extrinsic resistances extraction for sub-quarter micron MOSFETs, we have defined one additional linear relationship involving the summation of extrinsic resistances R_{se} and R_{de}. In fact, it can be demonstrated that at low frequencies (from 1 to 5 GHz) and for bias points chosen in linear region ($V_{gs} = > V_{th}$ and $V_{ds} << V_{gs}$) the real part of Z_{22} parameters are given by:

$$\text{Re}(Z_{22}) = R_{de} + R_{se} + f(intrinsic\ elements)\ . \quad (5)$$

Figure 12 presents the real part of Z_{22} measured in linear region from 1 to 5 GHz versus the layout channel length for 160 μm width SOI n-MOSFETs. A linear function is observed. By definition for a channel length equal to zero all of the intrinsic elements vanish, and therefore, from Eq. (5) and the intercept at the origin obtained from a linear regression on the measured data points (Fig. 12), the value of $R_{se} + R_{de}$ is extracted.

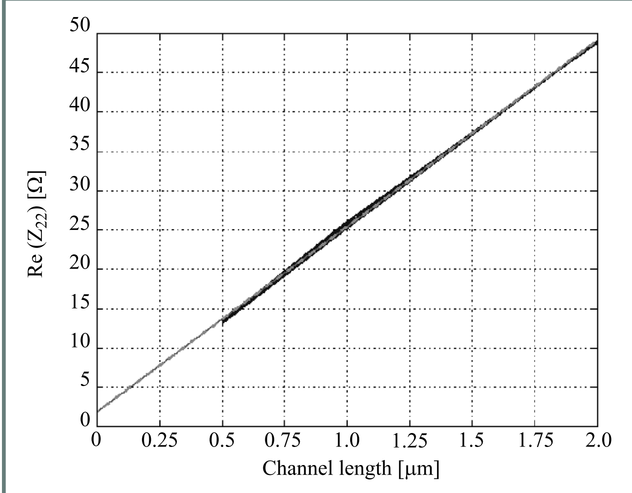

Fig. 12. Evolution of the Z_{22} parameter real part versus the layout channel length.

Table 1 shows all of the extrinsic elements values extracted for 12 x (6.6/0.35) μm^2 by using the characterization procedure explained in this section.

4.4. Determination of all intrinsic parameters

After subtracting the extrinsic resistances and capacitances from the measured S-parameters, all of the intrinsic elements ($C_{gsi}, C_{gdi}, C_{sdi}, R_{gsi}, R_{gdi}, G_{mi}, G_{dsi}$, and τ) for an arbitrary bias condition can be directly extracted by using simple matrix manipulations on the intrinsic Y-matrix [10]. Figure 13 presents the evolution of the different intrinsic elements versus frequency for $V_{gs} = V_{ds} = 0.9$ V. Except for the frequencies below 3 GHz, where the deviations from the horizontal are attributed to the low frequency limit of the TRL calibration, the values of the extracted intrinsic parameters remain fairly constant up to 40 GHz. The flatness of the extracted intrinsic elements curves over a wide frequency band is directly related to the completeness of the model used, the validity of the assumptions considered and the quality of the extraction procedure itself. In fact, all of the lumped elements of the small-signal SOI MOSFET model presented in Fig. 1 are considered by definition frequency independent.

Table 1
Extracted extrinsic capacitances and resistances for a 12 x (6.6/0.35) μm^2 SOI n-MOSFET

C_{gsee}	C_{gdee}	C_{dsee}	C_{gse}	C_{gde}	C_{dse}
[fF]					
5.77	5.77	10.4	16.5	14	6.5
R_{ge}	R_{de}	R_{se}			
[Ω]					
5	13.7	4			

The direct extraction method described above has been successfully applied to both SOI p- and n-MOSFETs of various sizes (W and L) up to 40 GHz.

Figure 14 presents the good agreement between measured and simulated S-parameters magnitudes and phases for a 12 x (6.6/0.35) μm^2 SOI n-MOSFET at $V_{gs} = = V_{ds} =$ 0.9 V.

5. Technological parameters extraction

Based on the same concept, technological parameters can be extracted from the S-parameters measurements. In fact, the transistor effective channel length (L_{eff}) can be obtained from the intercept at the origin of the linear regression on the data points plotted in a two dimensional plane $[x_1, x_2]$ by $[C_{gdi}, L]$, C_{gdi} being obtained by subtracting Y_{12} in depletion from Y_{12} in strong inversion ($V_{gs} >> V_{th}$ and $V_{ds} =$ 0 V). In fact, when the intrinsic gate-to-drain capacitance C_{gdi} equal to zero the residual channel length corresponds to the total overlap length ($\Delta L = \Delta L_{ovlp[S]} + \Delta L_{ovlp[D]}$). The effective channel length is then defined as $L_{eff} = L - \Delta L$.

Figure 15 shows the extracted intrinsic capacitance C_{gdi} for SOI n-MOSFETs composed of 12 gate fingers connected in parallel with a total width of 80 μm and a channel length of 0.25, 0.35, 0.5 and 1 μm.

¿From the extracted value of L_{eff}, the gate oxide thickness (t_{ox}) is obtained by $t_{ox} = \varepsilon_{ox}\ WL_{eff}/2C_{gdi}$.

For the measured transistors described above in this section, the extracted gate oxide thickness is 5.48 nm.

Fig. 13. Evolution of the intrinsic lumped extracted values (i.e. conductance (a), delay (b), capacitance (c), intrinsic non-quasi-static resistance (d)) versus frequency for a 12 x (6.6/0.35) μm^2 SOI n-MOSFET at $V_{gs} = V_{ds} = 0.9$ V.

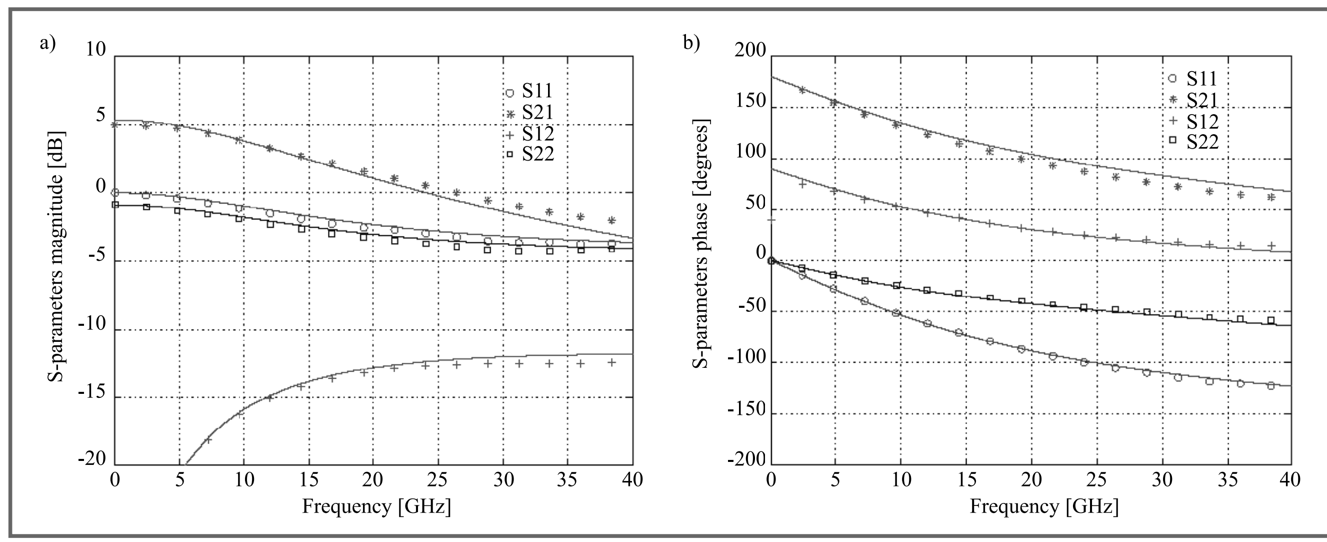

Fig. 14. Measured (lines) and simulated (symbols) S-parameters magnitudes (a) and phases (b) for a 12 x (6.6/0.35) μm^2 SOI n-MOSFET at $V_{gs} = V_{ds} = 0.9$ V.

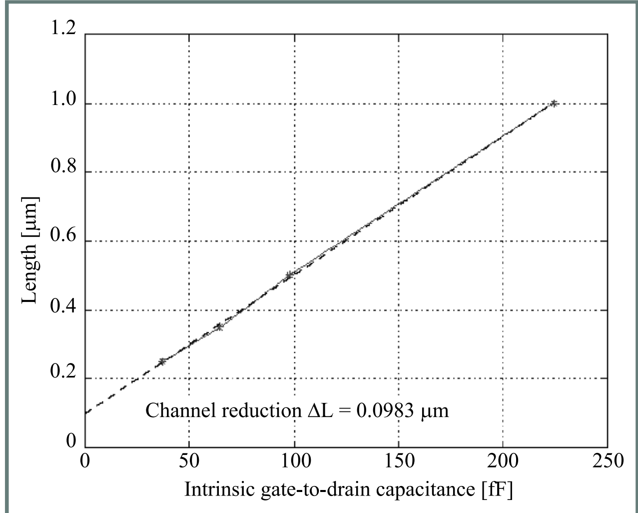

Fig. 15. Parametric curve defined in a two dimensional plane by $[C_{gdi}, L]$.

6. Conclusion

Direct extraction techniques based on measured S-parameters at different bias conditions are presented for determining technological parameters and microwave small-signal model of MOSFETs. This characterization procedure has been used to control and optimize the different steps of the fabrication process. The extracted equivalent circuits have been introduced in commercial simulators for successfully designing microwave SOI CMOS functionalities such as LNA, mixer and oscillators at 1.8 and 5.8 GHz.

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Paper

An impact of frequency on capacitances of partially-depleted SOI MOSFETs

Daniel Tomaszewski, Lidia Łukasiak, Agnieszka Zaręba, and Andrzej Jakubowski

Abstract — A non-quasi-static model of partially-depleted SOI MOSFETs is presented. Phenomena, which are particularly responsible for dependence of device admittances on frequency are briefly described. Several C-V characteristics of the SOI MOSFET calculated for a wide range of frequencies, preliminary results of numerical analysis and of measurements and brief analysis of the results are presented. Methods of model improvement are proposed.

Keywords — SOI MOSFET, small-signal models, non-quasi-static analysis, admittances.

1. Introduction

One of the main advantages of silicon-on-insulator (SOI) CMOS circuits is their speed, which results mainly from the reduced parasitic capacitances of SOI MOSFETs. However the C-V characteristics of partially-depleted (PD) SOI MOSFETs exhibit a relevant dependence on frequency. This effect results from the floating-body phenomena, which are due to the fact, that thin active film of the PD SOI MOSFET is surrounded by dielectric layers and junctions. A detailed numerical analysis of the physical phenomena in the PD SOI MOSFETs for small-signal excitation consitions was presented in [1], where a new mixed quasi-static (QS) / non-quasi-static (NQS) scheme of transient phenomena treatment was used. The main conclusions resulting from this work confirm the above mentioned features of the PD SOI MOSFETs and their C-V characteristics.

The reliable models of the PD SOI MOSFETs admittances, which account for the floating-body phenomena may be useful for characterization and CAD purposes. However, analytical models of the PD SOI MOSFETs admittances derived so far are based primarily on the QS aproach [2, 3], which does not allow to obtain frequency dependence of device capacitances. Such analysis is possible using the NQS methods, but there are only very few models of this category [4]. Moreover they are represented in AC domain not by appropriate set of equations, but rather by equivalent circuits. Small-signal current equations and admittances result from these circuits. Thus it is very difficult to ensure consistency between DC models and their small-signal counterparts.

In this work some results of analysis of frequency effect upon C-V curves of PD SOI MOSFETs are presented. They were obtained using the recently derived NQS model of the PD SOI MOSFETs in the strong inversion range [5]. This model is formulated as a set of current equations in the complex numbers domain. In case of conduction currents their AC components were obtained through linearization of the appropriate DC currents expressions. In case of displacement currents they were obtained as derivatives of the appropriate charges. Thus the AC and DC models of the PD SOI MOSFETs are fully compatible.

2. Small-signal currents components in the PD SOI MOSFET

The general Eq. (1), which describes transistor behaviour in the AC domain represents obviously condition of balance of all currents flowing into the device:

$$i_s^* + i_{gf}^* + i_d^* + i_{gb}^* = 0\,. \qquad (1)$$

All the components of formula (1) denote phasors (complex amplitudes of the small-signal components) of the source, front gate, drain and back gate currents, respectively. The Eq. (1) is linear in terms of v_{bs}^*, i.e. phasor of the time-dependent body-source voltage $v_{bs}(t)$. With the given v_{bs}^* AC components of all currents in the device may be determined. Then the small-signal admittances may be obtained using the following formula

$$Y_{xy} = G_{xy} + j\omega C_{xy} = \left.\frac{i_x^*}{v_y^*}\right|_{v_z^* = (0,0),\, z \neq y}\,. \qquad (2)$$

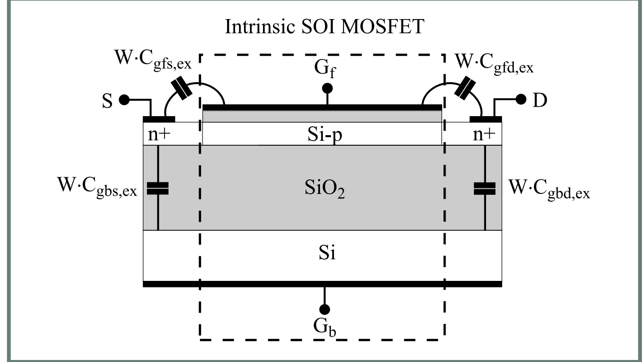
Below these current components are briefly described.

3. AC components of gates currents

Small-signal currents flowing into both gates consist of intrinsic and extrinsic, parasitic components

$$i_{gf(b)}^* = i_{gf(b),i}^* + i_{gf(b)s,ex}^* + i_{gf(b)d,ex}^*\,. \qquad (3)$$

Intrinsic components $i_{gf(b),i}^*$ result from charging/discharging of gates electrodes associated with the so-called „ideal" (intrinsic) MOSFET. They contain also currents $i_{sb,f(b),displ}^*$, $i_{db,f(b),displ}^*$, related to inner fringing field, which will be described in the next section. Extrinsic components $i_{gf(b)s,ex}^*$ and $i_{gf(b)d,ex}^*$ are related to overlap and outer fringing capacitances [6]. They are shown in Fig. 1.



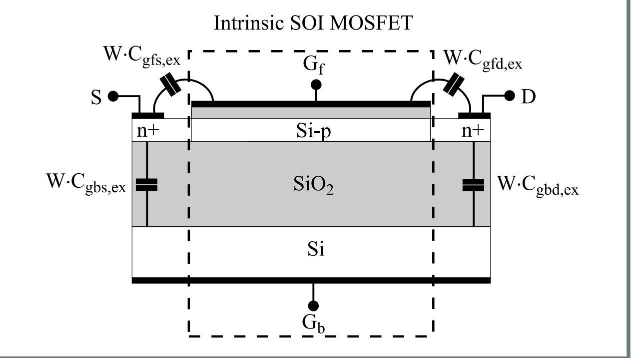


Fig. 1. Parasitic front/back gate-source/drain capacitances in PD SOI MOSFET.

These currents can be approximately considered as purely capacitative ones, because they depend only on voltages of the electrodes. They do not depend on spatial distribution of AC component of surface potential, so they do not exhibit additional phase shift relative to electrodes voltages.

4. AC components of source and drain currents

AC currents flowing into the source and drain are expressed as superpositions of several components, which are related to different phenomena at source and drain boundaries respectively.

$$i_s^* = i_{sb,diff+rec+displ}^* + i_{sb,f,displ}^* + i_{sb,b,displ}^* - i_{gfs,ex}^* + - i_{gbs,ex}^* - i_{drift,f}^*(0) - i_{drift,b}^*(0)\ , \tag{4}$$

$$i_d^* = -i_{db,diff+gen+aval+displ}^* - i_{db,f,displ}^* - i_{db,b,displ}^* + - i_{gfd,ex}^* - i_{gbd,ex}^* + i_{drift,f}^*(L) + i_{drift,b}^*(L)\ . \tag{5}$$

The variables in the above formulae have the following meaning:

$i_{drift,f(b)}^*(0)$, $i_{drift,f(b)}^*(L)$ – AC components of the channel drift currents at the front (back) Si-SiO_2 interfaces, which flow through the source (y = 0) or drain (y = L) contacts; they are determined by the approximate solution of current continuity equation; method of solution was adapted from [7] and generalized in order to account for body voltage variations; in the saturation range AC currents at the drain contact account for avalanche ionization in the „pinch-off" region;

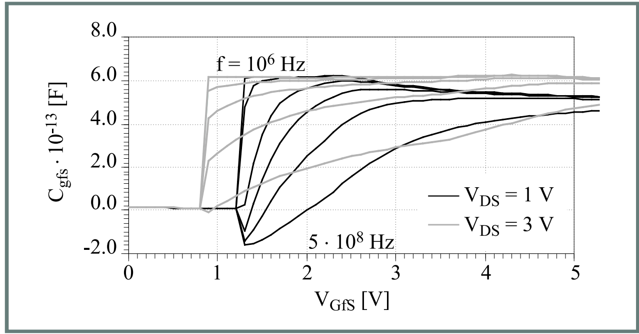
$i_{sb,diff+rec+displ}^*$ – total AC current, which flows through the bulk part of the source-body junction, which consists of two conduction components: diffusion and recombination currents and of displacement current;

$i_{db,diff+gen+aval+displ}^*$ – total AC current, which flows through the bulk part of the drain-body junction, which consists of two conduction components: diffusion and recombination currents and of displacement current; conduc-

tion currents are multiplied by avalanche ionization in the depletion region of the junction;
$i^*_{sb,f(b),displ}$, $i^*_{db,f(b),displ}$ – displacement currents (mentioned in the previous section), which are related to the inner fringing fields between the source (drain) and front (back) gate; in the presente model they result from the modulation of the widths of the source (drain) controlled space-charge areas by the appropriate gate DC bias;
$i^*_{gf(b)s,ex}$, $i^*_{gf(b)d,ex}$ – displacement currents related to overlap and outer fringing capacitances (described in the previous section).
The AC components of drift, diffusion, generation/recombination and avalanche ionization currents are described by the NQS models, so they exhibit dependence on frequency. Thus the admittances of the PD SOI MOSFETs should also be frequency dependent. In the next section this effect will be briefly described and illustrated by simulated data. Also preliminary results of numerical analysis and of measurements will be presented.

5. Effect of frequency on selected C-V curves

C-V characteristics of the PD SOI MOSFET were calculated using the model presented in the previous sections. Parameters of this device are listed in Table 1.
In Fig. 2 $C_{gfs}(V_{GfS})$ characteristics obtained for a range of frequencies and for two drain-source voltages are shown. A strong influence of frequency on these curves is evident. The main feature of these data is decrease of the C_{gfs} value in the strong-inversion range, when frequency increases to hundreds of megahertz. This means, that at high frequency a phase shift between voltage and current AC components significantly changes. Due to the non-quasi-static behaviour gate capacitor properties are changed. More detailed analysis could be done using conductances behaviour at high frequencies. Another feature is that at the boundary between the subthreshold and saturation ranges a decrease of C_{gfs} below zero Farads can be observed. This effect is rather not induced by strong field effects, because it diminishes when drain voltage increases. This effect requires further investigation. One of the possible approaches could be improvement of small-signal model of drift current in high-frequencies range. It would require accounting for higher-order terms in solution of integral equation [7].
Figure 3 shows influence of frequency on C_{gfd} capacitances. Weaker dependence of C_{gfd} on frequency (than in case of C_{gfs}) is probably due to the fact that C_{gfd} increases in non-saturation range, when channel is shortly connected to the drain electrode.
Figure 4 shows very strong influence of frequency on C_{gfgb}, which can be observed particularly at the border between subthreshold and saturation ranges (like in case of $C_{gfs}(V_{GfS})$ data). At higher frequencies the influence of gate bias on the capacitance diminishes.
Figures 5 and 6 show influence of frequency on C_{ds} and C_{sd} capacitances and non-symmetric (non-reciprocal) character of these curves. Very strong influence of frequency on C_{ds}



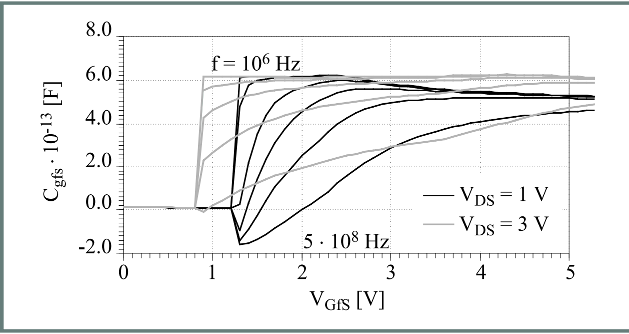
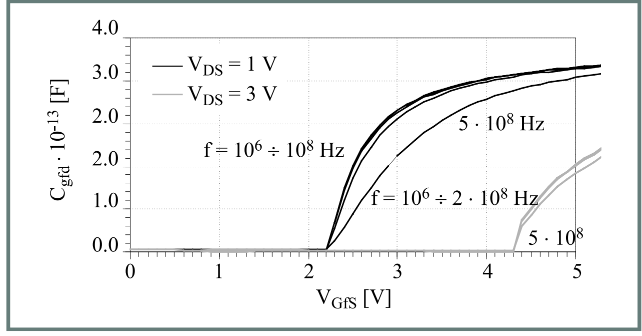


Fig. 2. Simulated $C_{gfs}(V_{GfS})$ characteristics of the PD SOI MOSFET ($V_{GbS} = 0$ V) for frequencies: 10^6, 10^7, $5 \cdot 10^7$, 10^8, $2 \cdot 10^8$, $5 \cdot 10^8$ Hz.



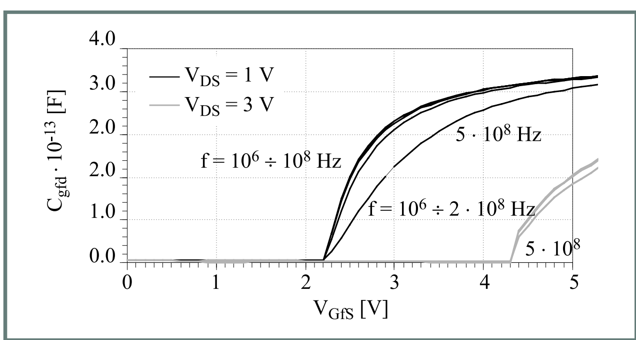
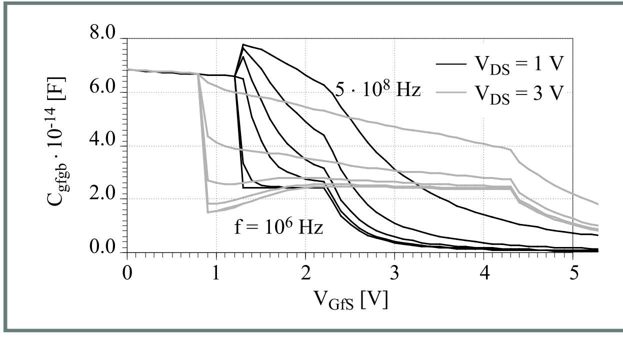


Fig. 3. Simulated $C_{gfd}(V_{GfS})$ characteristics of the PD SOI MOSFET for the range of frequencies.

Table 1
Parameters of the simulated PD SOI MOSFET

Parameters	Value
Width (W)	100 μm
Length (L)	9.4 μm
Front gate oxide thickness (T_{Oxf})	32.8 nm
Back gate oxide thickness (T_{Oxb})	400 nm
Si film thickness (T_{Si})	150 nm
Doping conc. In the Si film (N_B)	9×10^{16} cm^{-3}
Fixed charge density at the front Si-SiO$_2$ interface (N_{ssf})	3×10^{10} cm^{-2}
Fixed charge density at the back Si-SiO$_2$ interface (N_{ssb})	10^{11} cm^{-2}
Mobility in the front channel (μ_f)	318 cm^2/Vs
Mobility in the back channel (μ_b)	318 cm^2/Vs
Recombination life-time in the body (τ_B)	10^{-6} s
Recombination/generation life-time in the junctions (τ_J)	10^{-7} s
Temperature	22° C



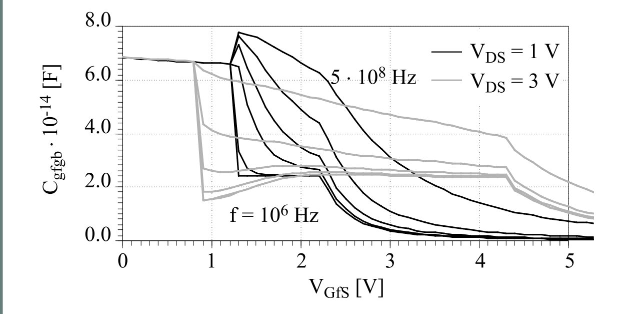
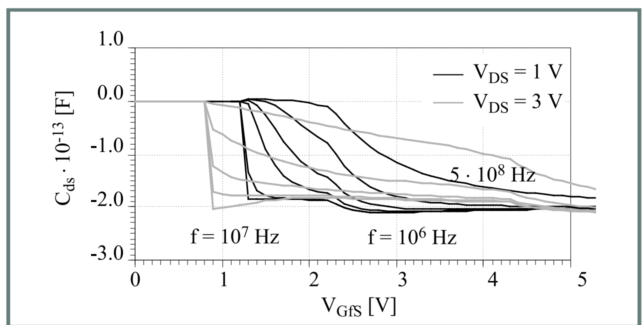


Fig. 4. Simulated $C_{gfgb}(V_{GfS})$ characteristics of the PD SOI MOSFET for the range of frequencies.

can be observed in the saturation range, when the drain current flows through the „pinch-off" region, where avalanche multiplication dominates. Much more weak influence of frequency on C_{sd} (as compared to C_{ds}) can be observed. Then the channel is shortly connected to the source node. It is analogous to the C_{gfs}, C_{gfd} pair of capacitances, which were compared above.

6. Experimental and numerical data (preliminary results)

In order to support the need of non-quasi-static modelling of SOI MOSFETs preliminary measurements of the PD SOI MOSFETs capacitances were done using the HP5275A LCR-meter. Figure 7 shows two $C_{gfs}(V_{GfS})$ curves of the MOSFET (device parameters are in the figure caption) obtained for two frequencies of measurement signal: 10^5 Hz, 10^6 Hz. The results of the measurement are not clear. In this range of frequencies there is only a slight difference between both curves. It is in agreement with the results presented earlier, where the relevant variations of capacitances were observed at much higher frequencies. Thus using these experimental data it is difficult to make conclusions about the correctness of the model and about the



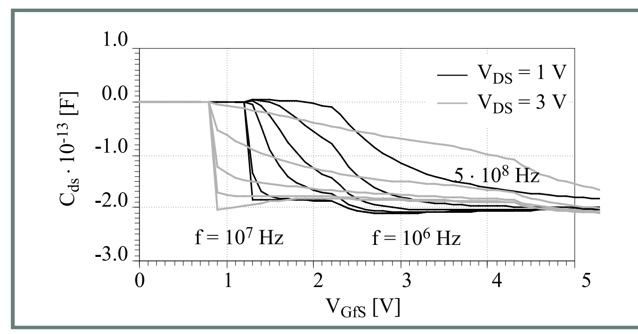
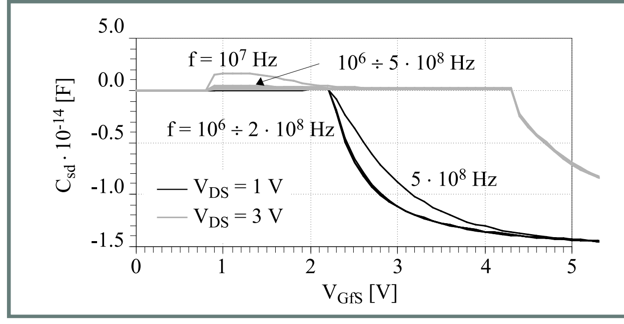


Fig. 5. Simulated $C_{ds}(V_{GfS})$ characteristics of the PD SOI MOSFET for the range of frequencies.



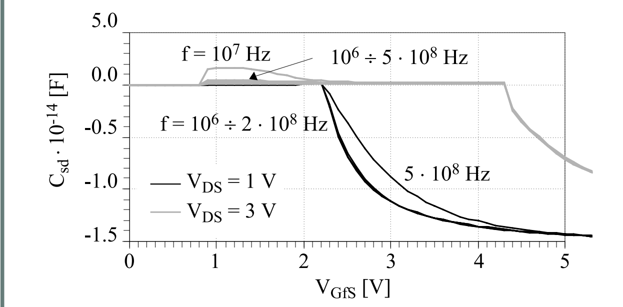
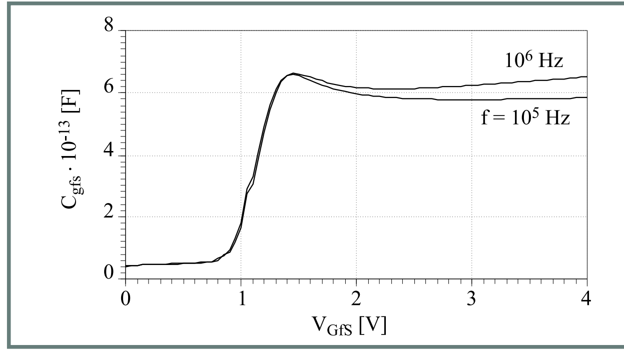


Fig. 6. Simulated $C_{sd}(V_{GfS})$ characteristics of the PD SOI MOSFET for the range of frequencies.



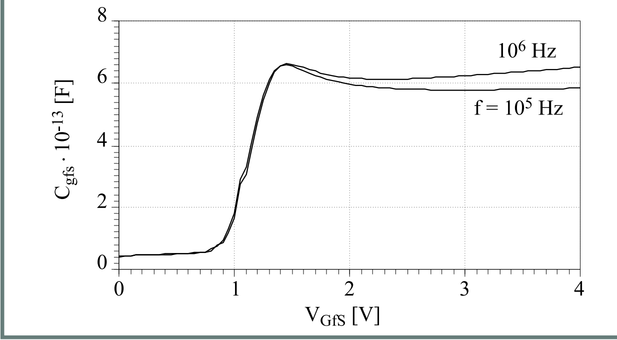
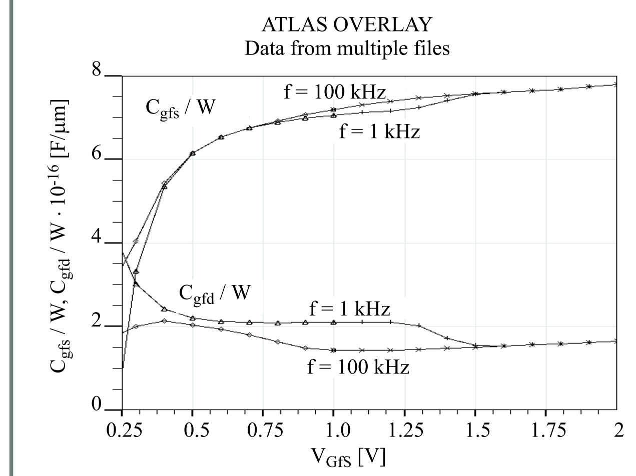


Fig. 7. $C_{gfs}(V_{GfS})$ determined experimentally. Device data: $W = 100$ µm, $L = 10$ µm, $t_{\mathrm{Si}} \approx 0.2$ µm, $t_{ox,b} \approx 0.4$ µm, $t_{ox,f} \approx 30$ nm, $N_B \approx 5 \cdot 10^{16}$ cm^{-3}.

experimentally observed effect of frequency variation. Such measurement in wider range of frequencies and for the set of devices should be done.

Preliminary numerical simulations of PD SOI MOSFET for varying frequencies (1 kHz, 100 kHz) were also done [8]. Figure 8 shows the obtained results. The parameters of the



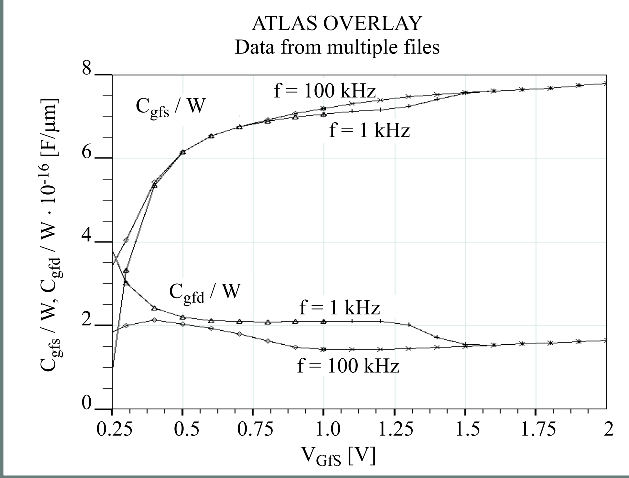


Fig. 8. $C_{gfs}(V_{GfS})$ determined numerically [8]. Device data: $L = 0.6$ µm, $t_{\mathrm{Si}} \approx 0.2$ µm, $t_{ox,b} \approx 0.4$ µm, $t_{ox,f} \approx 30$ nm, $N_B \approx 5 \cdot 10^{16}$ cm^{-3}.

simulated device are shown in the figure caption. The C_{gfs} and C_{gfd} data exhibit sensitivity to frequency variations in the saturation range, although the frequency range is much lower than above. However the data were obtained for the short-channel device. Thus phenomena in „pinch-off" region play much more important role, than in case of long-channel devices.

Both experimental and numerical data presented above confirm the need of accounting for frequency effect on C-V models of PD SOI MOSFETs.

7. Conclusions

The presented AC model of the PD SOI MOSFETs shows significant effect of frequency on device capacitances in strong inversion. Thus non-quasi-static approach to SOI MOSFETs small-signal modelling can be relevant for CAD of SOI CMOS analog and analog-digital circuits.

More general analysis of effect of frequency on MOSFETs admittances requires also accounting for transistors conductances.

The model should be extended towards higher frequencies range and improved in the subthreshold range.
In order to prove validity of the model extensive measurements and numerical simulations of PD SOI MOSFETs for wide range of frequencies should be done.

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Agnieszka Zaręba, **Andrzej Jakubowski** – for biography, see this issue, p. 18.

Paper

Comparison of microwave performances for sub-quarter micron fully- and partially-depleted SOI MOSFETs

Michaël Goffioul, Gilles Dambrine, Danielle Vanhoenacker, and Jean-Pierre Raskin

Abstract — The high frequency performances including microwave noise parameters for sub-quarter micron fully- (FD) and partially-depleted (PD) silicon-on-insulator (SOI) n-MOSFETs are described and compared. Direct extraction techniques based on the physical meaning of each small-signal and noise model element are used to extract the microwave characteristics of various FD and PD SOI n-MOSFETs with different channel lengths and widths. $TiSi_2$ silicidation process has been demonstrated very efficient to reduce the sheet and contact resistances of gate, source and drain transistor regions. 0.25 μm FD SOI n-MOSFETs with a total gate width of 100 μm present a state-of-the-art minimum noise figure of 0.8 dB and high associated gain of 13 dB at 6 GHz for V_{ds} = 0.75 V and $P_{dc} < 3$ mW. A maximum extrapolated oscillation frequency of about 70 GHz has been obtained at V_{ds} = 1 V and J_{ds} = 100 mA/mm. This new generation of MOSFETs presents very good analogical and digital high speed performances with a low power consumption which make them extremely attractive for high frequency portable applications such as the wireless communications.

Keywords — microelectronics, microwave devices, SOI MOSFET.

1. Introduction

The boom of mobile communications leads an increasing request of low cost and low power mixed mode integrated circuits. Maturity of silicon-based technology and recent progresses of MOSFET's microwave performances, explain the silicon success as compared to III–V technologies [1–4]. Silicon-on-insulator-based MOSFETs are very promising devices for multigigahertz applications. Especially low microwave noise at low drain voltage bias condition is one of very interesting high frequency characteristics of such devices. Moreover, due to the reduction of channel length dimension and the improvement of electrode processes (silicidation or metal T-gate processes), very low noise integrated circuits operating beyond 10 GHz and more are realizable. The main goal of this paper is to present state-of-the-art high frequency performances of sub-quarter micron gate length FD and PD SOI MOSFETs fabricated with a CMOS-compatible process on low-resistivity (20 Ωcm) SIMOX wafers.

Accurate knowledge of MOSFET noise parameters is required in performing realistic and reliable design of low noise amplifier (LNA), key element of high sensitive microwave receiver. In the present paper, we intend to accurately determine noise parameters of MOSFETs and to evaluate their dependence with the fabrication technology (fully versus partially depleted transistors).

In Section 2, bulk and SOI MOSFET's technologies are briefly described and compared. Details about the LETI SOI MOSFET's fabrication process are given in Section 3. Characterization techniques for the small-signal and high frequency noise model extractions are briefly described in Section 4. The measurement results of high frequency gains and noise parameters are presented in Sections 5 and 6, respectively.

2. MOSFET's technologies

The competing device technologies for the emerging mass-market applications are bipolar, CMOS, and mixed bipolar-MOS (BiCMOS). Bulk-silicon and silicon-on-insulator options are available for all three. Bipolar-only processes, and SiGe bipolar in particular, are high-performance technologies which are probably shooting too high with respect to the needs of the mobile communication market in the near future [5]. Bipolar-only processes target high-speed applications and are in particular not well suited for the implementation of the low-power digital base-band part of portable communication terminals. CMOS and BiCMOS are thus the best candidates for the single chip integration of mobile communication transceivers. High performance sub-micrometer-channel MOSFETs are capable of analogue operation at microwave frequencies [5]. The record transition frequencies of 150 GHz recently attained with experimental nanometer MOSFETs show that present-day MOS technology still has potential for improvement [6]. Using a SOI substrate, circuit speed can be substantially improved, but the ultimate advantage of SOI CMOS circuits is to be expected in low-power applications when using thin-film, FD SOI MOSFETs [7].

2.1. Bulk MOSFET

Characteristic of bulk technologies is that the transistors are fabricated directly on monocristalline silicon wafers and are thus all in contact with the substrate material. Bulk has been the main-stream technology for years, but SOI has now evolved into a mature contender [8]. A specific advantage of bulk technology is that the substrate acts as an efficient heat-sink, thanks to the high thermal conductiv-

ity of silicon. Bulk technology is however confronted with isolation problems. Bulk MOS transistors suffer from high parasitic capacitances – diffusion capacitances, body effect – and require special techniques for sub-micrometer scaling. Figure 1 shows the cross-section of a high-performance

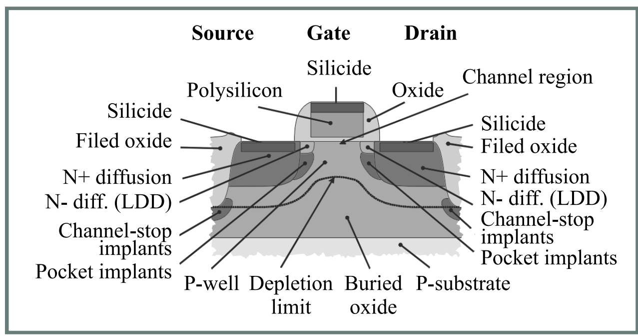

Fig. 1. Cross-section of a short-channel bulk-silicon MOSFET.

bulk MOSFET. The standard isolation technique in bulk technology is the use of reverse-biased junctions. This technique is only efficient at low frequencies and at moderate operating temperatures. Indeed, high-frequency signals may easily cross reverse-biased junctions because of the finite capacitance, while leakage currents increase rapidly with temperature up to a point where reverse biased junctions have little blocking effect. Junction isolation may even fail catastrophically when neighboring p- and n-wells combine to form a thyristor-like structure which can be triggered by a transient injecting a sufficient amount of current in any of the wells. These issues can be partly resolved by increasing the inter-well spacing, at the cost of a lower integration density, or by using advanced techniques such as trench isolation.

At low frequencies, when the substrate is essentially conductive, bulk MOSFETs are loaded by large capacitances due to the depletion region associated with the source and drain diffusions as well as with the inversion channel. The lower limit of the depletion region is represented in Fig. 1 by the dashed line. The presence of a large depletion region underneath the gate reduces the effective control of the gate on the channel. The off-state performance of bulk MOSFETs is also affected, as the gate voltage must be driven lower below threshold to restrain the leakage current below a specified level. Bulk MOSFETs must therefore be designed with higher threshold voltages.

The large depletion zones associated with the source and drain diffusions of bulk MOSFETs are also an obstacle to the sub-micrometer scaling of the channel length. Indeed, the finite width of these depletion zones set a lower bound on the channel length. Below this limit, the source and drain depletion zones overlap, creating a region where a strong electric field can sweep electrons directly from source to drain independently of the gate voltage. Even, at channel lengths above this punch-through limit, the source and drain depletion zones have a detrimental impact on scaling, as they contribute to lower the threshold voltage [7]. Present-day sub-micrometer MOSFET technologies compensate the punch-through and threshold voltage roll-off effects using special pocket implants, which are designed to locally divert the electric field [9]. These pockets must be very precisely located at the lower tip of the diffusions. To achieve the proper doping profile, a tilted implantation technique is used where the wafer is tilted at an angle with respect to the ion-beam. Four of these implants are required to provide pockets at the drain and source of MOSFETs aligned in two orthogonal directions. Specific masks are also required to select the implantation regions.

2.2. Partially depleted SOI MOSFET

Silicon-on-insulator technology can be used to enhance the performances of bulk MOSFETs, particularly speed and packing density. The latter is increased on SOI essentially thanks to the very efficient isolation of individual devices by the field and buried oxides. This all-round isolation alleviates the need for diffused wells which require specific contacts and careful spacing and are limiting the integration density in bulk technology. The buried oxide layer, with its low dielectric constant, contributes to significantly reduce the parasitic capacitances loading the source and drain diffusions, allowing SOI designs to book speed gains with respect to their bulk counter-parts [8, 10].

The partially depleted device shown in Fig. 2 is a rather conservative SOI MOSFET design: it is merely a bulk MOSFET transposed onto a SOI substrate. In particular,

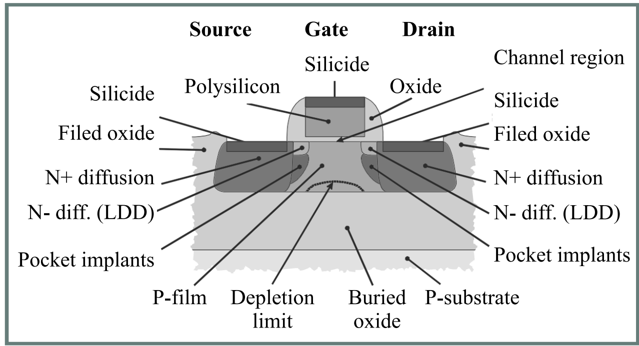

Fig. 2. Cross-section of a short-channel partially-depleted SOI MOSFET.

the existence of a quasi-neutral region below the depletion zone associated with the transistor ensures that the body effect in the partially depleted SOI MOSFET is identical to that of the bulk MOSFET, so that the SOI device shows no improvement in the subthreshold characteristics [7] which are essential for low-voltage applications.

2.3. Fully depleted SOI MOSFET

It has been shown in the last subsection that SOI technology remedies elegantly to the isolation problems of conventional bulk technologies and even contributes to circuit speed improvements. The use of fully depleted SOI MOSFETs extends the advantages of SOI even further to

easier down-scaling and nearly optimal low-voltage performances. Fully depleted SOI devices are obtained by using silicon film thicknesses thinner than the depth of the depletion zone, typically below 100 nm. Figure 3 represents the cross-section of a short-channel FD SOI MOSFET.

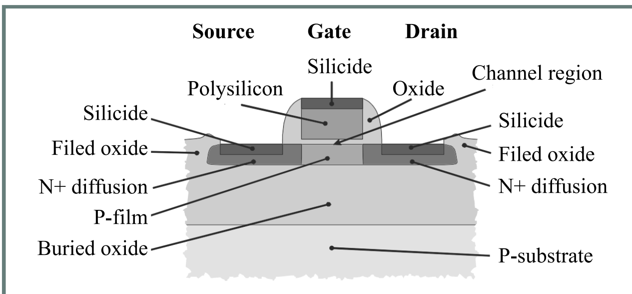

Fig. 3. Cross-section of a short-channel fully-depleted SOI MOSFET.

The very small body effect of fully depleted SOI MOSFETs is the key to their outstanding low-voltage performances and their good high-frequency performances. Interestingly, the fabrication of these devices is less complicated than that of bulk MOSFETs of comparable channel lengths, notwithstanding their better performances. The comparison of Figs. 1 and 3 shows indeed that the SOI MOSFET structure is inherently simpler than that of the bulk device.

In FD SOI MOSFETs, the small thickness of the silicon film strongly limits the extent of the depletion zones associated with source and drain, so that the risk of punch-through and the threshold-voltage roll-off are strongly attenuated. This feature alleviates the need for complex pocket implants, allowing to reach smaller channel lengths with a simpler fabrication process, comparatively to bulk technology. Even other short-channel effects such as channel-length modulation and drain-induced barrier lowering have been shown to be less severe in fully depleted SOI MOSFETs.

3. Fabrication process

200 nm UNIBOND wafers with a 400 nm buried oxide are used as the starting material. The silicon thickness is thinned down to 100 nm and 30 nm by a recessed-channel process, for partially- and fully-depleted SOI MOSFETs, respectively. Gate oxide of 4.5 nm is grown after a LOCOS isolation. A field implant is used to eliminate sidewall leakage. A 200 nm thick polysilicon layer is deposited and patterned by DUV lithography. A medium doped drain implant is followed by formation of a 80 nm spacer oxide after which the source-drain regions are implanted and activated with a 950°C/15 s RTA. A titanium silicide process is used to reduce the sheet and contact resistances of gates and the elevated 80 nm thick source-drain regions. After the silicide process a gate sheet resistance of about 10 $\Omega/\Box$, instead of 100 $\Omega/\Box$ for a classical doped polysilicon gate, is obtained for a 0.25 μm gate channel length MOSFET. The back-end processing includes a three level metal process with tungsten plugs and planarization of intermetal oxides by chemical and mechanical polishing (CMP).

Figures 4 and 5 represent, respectively, the cross-section pictures of a PD and FD 0.25 μm SOI MOSFETs.

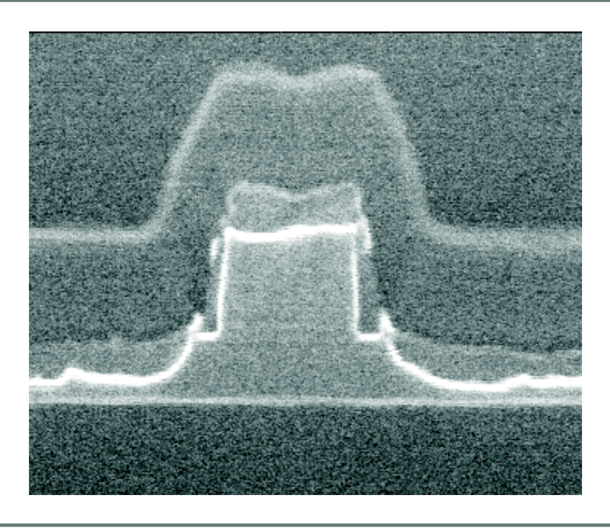

Fig. 4. Cross-section of a 0.25 μm PD SOI MOSFET (active silicon film of 100 nm) with a $TiSi_2$ silicidation process for the gate, drain and source areas.

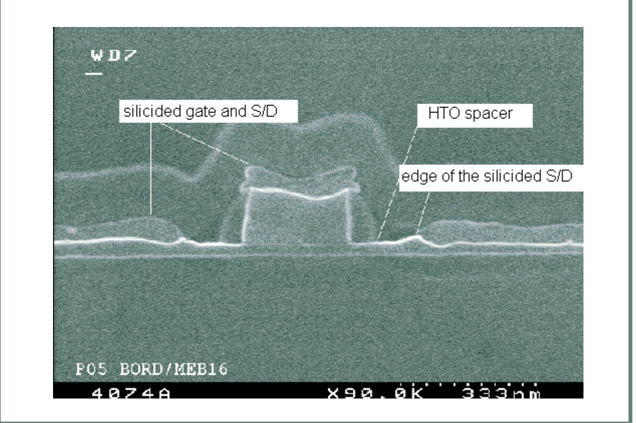

Fig. 5. Cross-section of a 0.25 μm FD SOI MOSFET (active silicon thin-film of 30 nm) with a recessed-channel process.

4. High frequency characterization techniques

The S-parameters were measured on-wafer up to 40 GHz (HP8510 network analyzer) and the noise figures in the $1 \div 18$ GHz frequency range (HP8971 noise measurement set-up).

The direct extraction methods presented in [11] have been applied to de-embed the transistors microwave performances from the on-wafer S-parameters measurements. This characterization procedure combines careful design of

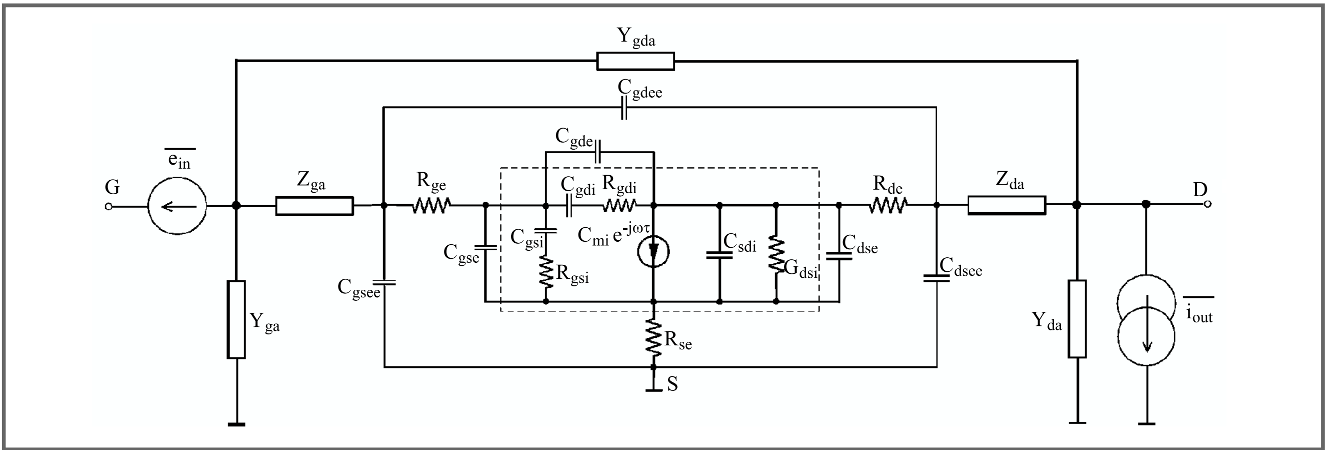

Fig. 6. Small-signal model including the input and output equivalent high frequency noise sources of a common-source SOI MOSFET.

probing and calibration structures, rigorous *in situ* calibration and a powerful direct extraction method. The extraction procedure is directly based on the physical meaning of each small-signal model element (Fig. 6). Knowing the qualitative small-signal behavior of each model parameter versus bias conditions, the high frequency equivalent circuit can be simplified for extraction purposes. Biasing MOSFETs under depletion, strong inversion and saturation conditions, the microwave small-signal elements and certain technological parameters can be extracted directly from the measured S-parameters. These new extraction techniques allow us to understand deeply the behavior of the sub-quarter micron SOI MOSFETs in microwave domain and to control their fabrication process. Moreover, due to the physical meaning attributed to each model element through the characterization process, the extracted equivalent circuit is scalable. This last point is crucial for circuits simulation and optimization purposes.

The four noise parameters are deduced from noise figures (NF_{50}), with a single 50 Ω generator impedance measured versus frequency [12] and the use of a two uncorrelated noise parameters model (e_{in} and i_{out}) represented in Fig. 6. Indeed, it can be shown that NF_{50} (in linear), in the case of FET, is a linear function versus frequency square in broadband. We can, then, obtain two independent noise parameters from the slope and the origin intercept of this linear function. By addind a two-uncorrelated noise sources model, all the FET's noise parameters (NF_{min}, $R_n, |\Gamma_{opt}|$ and $\arg(\Gamma_{opt})$) can be deduced. This noise model presented in Fig. 6 is a Pospieszalski based model applied to the extrinsic device. As shown Fig. 6, two noise uncorrelated noise sources are used: an input noise voltage source e_{in} and an output noise current source i_{out}. From these noise sources, two equivalent noise temperatures T_{in} and T_{out} are defined as follows:

$$T_{in} = \frac{\overline{e_{in}^2}}{4\,\mathrm{k}\,\mathrm{Re}\left(\frac{1}{Y_{11}^E}\right)\Delta f}\,, \tag{1}$$

$$T_{out} = \frac{\overline{i_{out}^2}}{4\,\mathrm{k}\,\mathrm{Re}\left(\frac{1}{Z_{22}^E}\right)\Delta f}\,, \tag{2}$$

$$\overline{e_{in}\, i_{out}^*} = 0\,, \tag{3}$$

where k is the Bolzmann constant, Δf is the bandwidth over which the noise is measured, $\mathrm{Re}\left(1/Y_{11}^E\right)$ is the input Thevenin equivalent resistance while $\mathrm{Re}\left(1/Z_{22}^E\right)$ is the output Norton equivalent conductance. It should be noted that experimental results [13] and models [14] show that the value of T_{in} is close to the ambient temperature and almost independent of the drain current while T_{out} is strongly dependent of the drain current and its value can be as high as 1000÷2000 K due to the hot electrons effect. These experimental and modeling studies have shown that the assumption of uncorrelated noise sources remains valid for drain current density less than 200/300 mA/mm. Using this noise measurement technique, the uncertainty of the extracted noise parameters depends both on the accuracy of the noise figure measurement with a 50 Ω generator impedance (about ±0.1 dB in the 2÷12 GHz frequency range) and on the validity domain of the noise model. This noise measurement technique has been compared [12] in many cases with commonly used the „multi-impedance" noise measurement method. This comparison has shown a good agreement between the four noise parameters obtained using our noise measurement method and commercially available system (based on the „multi-impedance" approach).

5. Small-signal high frequency performances

Table 1 shows the extracted values for extrinsic and intrinsic lumped small-signal elements for FD and PD SOI n-MOSFETs. These transistors have a gate channel length of 0.35 μm and are composed of 12 gate fingers of 6.6 μm connected in parallel, i.e. a total channel width of approximately 80 μm. A $TiSi_2$ silicidation process has been used

Table 1
Extracted values of extrinsic and intrinsic elements for FD and PD SOI n-MOSFET with a channel length of 0.35 μm and a total channel width of 80 μm at $V_{gs} = V_{ds}$ = 0.9 V

	C_{gsee}	C_{gdee}	C_{dsee}	C_{gse}	C_{gde}	C_{dse}	R_{se}	R_{de}	R_{ge}	C_{gsi}	C_{gdi}	G_{mi}	G_{dsi}	τ	R_{gsi}
	[fF]						[Ω]			[fF]		[mS]		[ps]	[Ω]
FD	5.77	5.77	10.4	14	16.5	6.5	4	13.7	5	90	12.5	22	1.1	0.75	7
PD	5.77	5.77	10.4	12.8	21.1	14	6.75	13.5	3.6	100	7	20	1.9	1	5

to reduce the gate, drain and source sheet resistivities and contact resistances.

The parasitic capacitive couplings between metallic interconnection located outside the active zone of the transistor (C_{gsee},C_{gdee} and C_{dsee}) are assumed identical for both types of SOI transistor (FD and PD). All of the extrinsic capacitances and resistances present extracted values fairly similar for both technologies, except for the extrinsic proximity drain-to-source capacitance C_{dse}. The augmentation of C_{dse} for the PD SOI MOSFET can be explain by the increase of the effective area of that parasitic capacitance due to the thicker active silicon film.

Better G_{mi} (10% more) and channel time delay τ (25% less) are observed for FD SOI MOSFET compared to the PD one. These improvements are explained by the better control of the channel region by the gate contact in the case of the FD structure. A reduction of the output conductance by approximately 42% is measured for the FD SOI MOSFET. The decrease of the output conductance indicates the reduction of the short channel effects with FD SOI MOSFETs.

The designers of RF circuits have defined some figures of merit for microwave transistors. If devices be used for RF applications, the aim has to be at maximizing the transit frequency (f_T) and maximum oscillation frequency (f_{max}), achieving a small minimum noise figure (NF_{min}) with a sufficiently high associated gain (G_{ass}), and reducing the $1/f$ noise.

Frequencies f_{max} and f_T are defined respectively as the cut-off frequency of unilateral gain (*ULG*) and the cut-off frequency of the current gain (H_{21}), i.e. f_{max} and f_T are the frequency points when, respectively, the *ULG* and H_{21} equal to 1 (i.e. 0 dB).

The maximum available gain (*MAG*) can be achieved for a stable device when we have simultaneously a complex-conjugate matched load and complex-conjugate matched source. The unilateral gain is defined by Mason [15] as the maximum available gain when a lossless feedback is used to cancel the transmission of power from the output to the input (S_{12}) of the device. *ULG* is derived from the S-parameters of the measured device as follows:

$$ULG = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{k\left|\frac{S_{21}}{S_{12}}\right| - \mathrm{Re}\left(\frac{S_{21}}{S_{12}}\right)} , \tag{4}$$

where

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

with

$$\Delta = S_{12}S_{21} - S_{11}S_{22} ,$$

and k is the Rollett stability factor. The active device is unconditionally stable if $k > 1$ and potentially unstable if $k < 1$.

The current gain H_{21} is derived from the S-parameters of the measured device by

$$\left|H_{21}\right| = \frac{|i_2|}{|i_1|} = \left|\frac{-2S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}\right| . \tag{5}$$

¿From the small-signal equivalent circuit presented in Fig. 6, H_{21} and f_T can be expressed by the following simple equations:

$$\left|H_{21}\right| = \frac{G_{mi}}{\omega(C_{gs} + C_{gd})} \tag{6}$$

and then

$$f_T = \frac{G_{mi}}{2\pi(C_{gs} + C_{gd})} , \tag{7}$$

where G_{mi},$C_{gs}(= C_{gsi} + C_{gse})$ and $C_{gd}(= C_{gdi} + C_{gde})$ are, respectively, the intrinsic gate transconductance, the gate-to-source and gate-to-drain capacitances.

Sze defines a very useful relationship between f_{max} and f_T in [16]:

$$f_{max} = \frac{f_T}{2\sqrt{2\pi f_T R_{ge}(C_{gdi} + C_{gde}) + G_{dsi}(R_{ge} + R_{se} + R_{gsi})}} . \tag{8}$$

Approximate expressions (7) and (8) show that while f_T can simply be increased by scaling down the devices, f_{max} depends strongly on the parasitics, as well as on G_{mi} and G_{dsi} which are very sensitive to the drain current and thus V_{gs}.

Figure 7 presents the evolution of f_{max} and f_T as a function of the bias conditions ($V_{ds} = V_{gs}$) for silicided and non-silicided 12 x (6.6/0.35) μm^2 SOI n-MOSFETs. f_T and f_{max} of, respectively, 26 and 56 GHz are reached at $V_{ds} = = V_{gs} = 1$ V for the silicided 0.35 μm SOI n-MOSFET. These results render this type of devices suitable for low-voltage, low-power RF applications.

Cut-off frequencies f_T and f_{max} versus bias conditions curves reach a plateau above $V_{ds} = V_{gs} = 1.2$ V. This saturation characteristic can be explain by the saturation carrier velocity. In fact, for high values of longitudinal electric

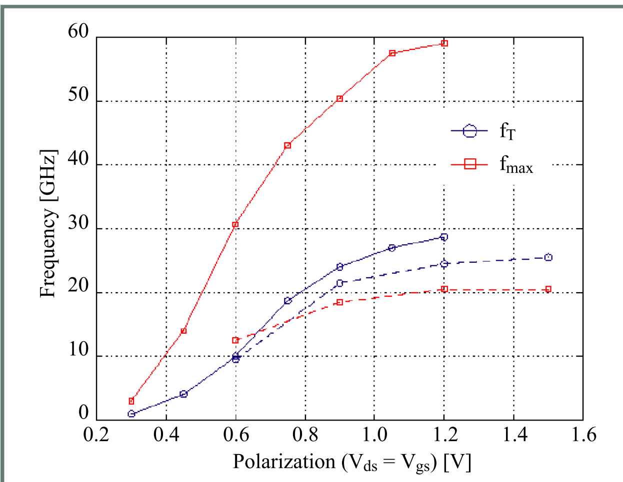

Fig. 7. Cut-off frequencies f_T and f_{max} as a function of supply voltage ($V_{ds} = V_{gs}$) for silicided (solid line) and non-silicided (dashed line) 12 x (6.6/0.35) μm^2 SOI n-MOSFETs.

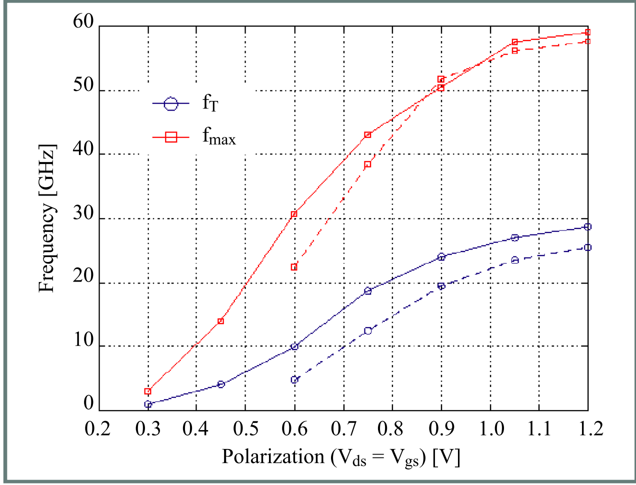

Fig. 8. Cut-off frequencies f_T and f_{max} as a function of supply voltage ($V_{ds} = V_{gs}$) for silicided FD (solid line) and PD (dashed line) 12 x (6.6/0.35) μm^2 SOI n-MOSFETs.

field between the source and drain electrodes, the velocity of the carriers in the thin inversion layer tends to saturate due to important collisions between them. These effects lead to an important degradation of the effective surface mobility of carriers in the channel. It is easy to understand that these effects are mainly observed in devices with small channel lengths. The saturation velocity of carriers in a MOSFET is reached for a longitudinal electric field between the source and drain, called critical electric field, of about 1 V/µm for electrons and about 3 V/µm for holes [17]. These values are in accordance with the measured characteristics presented in Fig. 7. We see that the velocity saturation effect is a very important limiting parameter in the design of small devices and thus particularly for microwave applications. Therefore, the study of the velocity saturation effect on the small-signal microwave performances of SOI MOSFETs is absolutely necessary to establish accurate and physical models.

Figure 7 shows clearly also the great interest of the silicidation process in order to improve the maximum oscillation frequency by reducing the parasitic extrinsic resistances R_{ge}, R_{de} and R_{se}. After silicidation, the parasitic extrinsic gate resistance is approximately reduce by a factor 10 and f_{max} is triple.

Figure 8 presents the evolution of f_T and f_{max} versus bias conditions for silicided FD and PD 12 x (6.6/0.35) μm^2 SOI n-MOSFETs. The slight improvement of cut-off frequencies obtained with FD SOI n-MOSFETs can be related to the improvement of the gate transconductance and the reduction of the ouput conductance and channel time delay previously mentionned in Table 1. The frequency band of the network analyzer being limited up to 40 GHz, the cut-off frequencies above that limit are determined by simple linear extrapolation of the corresponding gains in logarithmic graphs. Due to the measurements and extrapolations inaccuracies, an error of around 15% can be attributed to these extrapolated cut-off frequencies. That inacurracy can explain the similar values of f_{max} obtained for FD and PD SOI n-MOSFETs at higher bias conditions ($V_{ds} = V_{gs} > 0.7$ V).

Figure 9 presents the evolution of f_T and f_{max} versus the channel length of various silicided SOI n-MOSFETs having a total gate width (W) of 80 µm and biased at

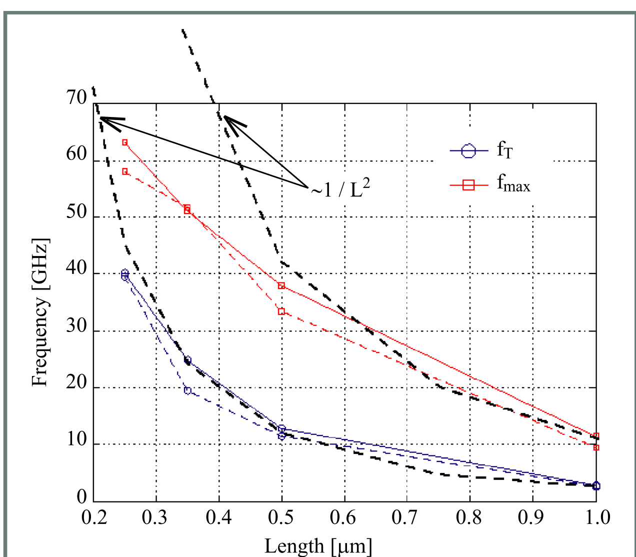

Fig. 9. Cut-off frequencies f_T and f_{max} versus channel gate length for 0.35 µm FD (solid line) and PD (dashed line) SOI n-MOSFETs at $V_{ds} = V_{gs} = 0.9$ V.

$V_{ds} = V_{gs} = 0.9$ V. The cut-off frequencies increase with the reduction of the channel length. The dependence in $1/L^2$ of f_T is in accordance with the simplified expression Eq. (7). In fact, G_{mi} being proportional to W/L and $(C_{gs}+C_{gd})$ to WL, f_T is a function of $1/L^2$. f_{max} presents also a dependence in $1/L^2$ for large channel lengths but this increase rate decreases for L smaller than 0.5 µm because of the R_{ge} increase with the reduction of the channel length (L) becomes dominant in Eq. (8).

6. High frequency noise characteristics

Accurate knowledge of transistor noise parameters ($NF_{min}, R_n, |\Gamma_{opt}|$ and $\arg(\Gamma_{opt})$) is required in performing realistic and reliable design of low noise amplifier (LNA), key element of high sensitive microwave receiver.

The main objective of this section is to compare the high frequency noise parameters for FD and PD SOI MOSFETs. More details about the physical interpretations of the measured high frequency noise parameters, but also the general interests and the limitations of SOI MOSFET technology for the realization of ultra-low-noise circuits can be found in [12].

Figure 10 represents the cut-off frequencies (f_T and f_{max}) and the minimum noise figure (NF_{min}) for a 0.25 μm FD SOI n-MOSFET with a current density of 100 mA/mm.

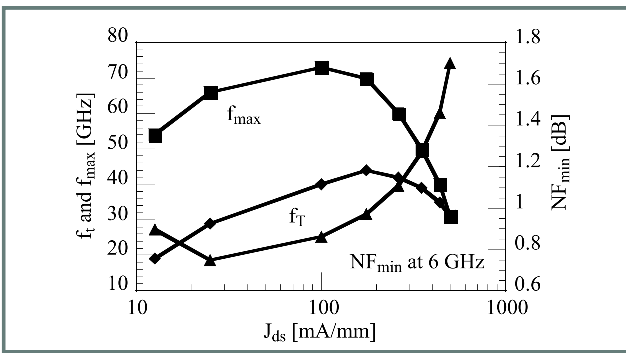

Fig. 10. Cut-off frequencies (f_T, f_{max}) and minimum noise figure NF_{min} versus current density at $V_{ds} = 1$ V for a 12 × (6.6/0.25) μm^2 FD SOI n-MOSFET.

A current gain cut-off frequency f_T and an extrapolated maximum oscillation frequency f_{max} of 40 GHz and 70 GHz, respectively, are reached at $V_{gs} = V_{ds} = 1$ V for a NF_{min} less than 1 dB.

Figure 11 shows the variation, at 6 GHz, of the NF_{min} and G_{ass} as a function of the drain current density ($V_{ds} = 1$ V).

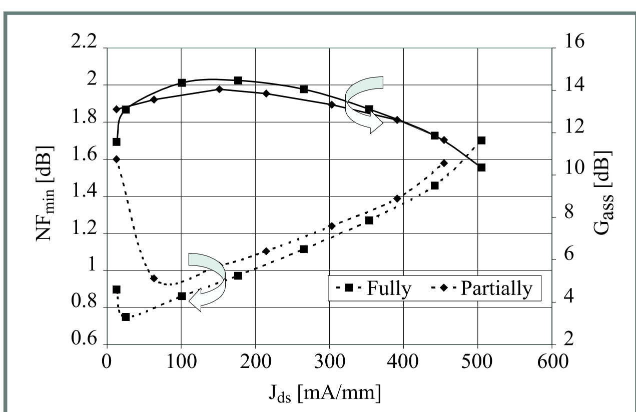

Fig. 11. Comparison between 12 x (6.6/0.25) μm^2 FD and PD SOI n-MOSFETs: evolution of NF_{min} and G_{ass} as a function of the drain current density at 6 GHz and $V_{ds} = 1$ V.

For a drain current density close to 75 mA/mm, the NF_{min} is 0.8 dB with G_{ass} of 13 dB. This result is one of the best reported in the literature. It shows that LNA could be designed with a power consumption of less than 35 mW/mm. Figure 12 presents the evolution, at 6 GHz, of the NF_{min} and G_{ass} as a function of the drain voltage for a constant drain current density of 75 mA/mm.

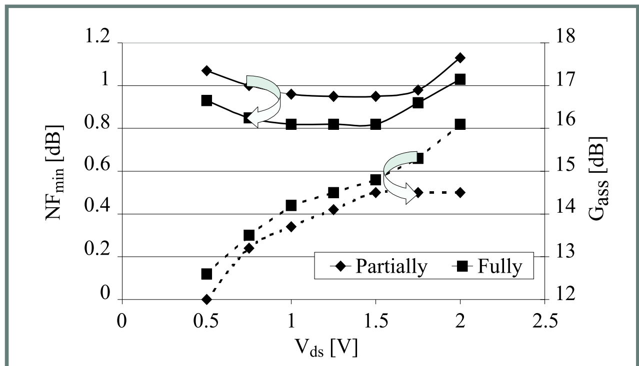

Fig. 12. Comparison between FD and PD SOI n-MOSFETs: evolution of NF_{min} and G_{ass} as a function of the drain bias voltage at 6 GHz; $J_{ds} = 75$ mA/mm; 12 x (6.6/0.25) μm^2.

Figure 13 shows the evolution of Γ_{opt} as a function of the drain current density at 2 GHz and $V_{ds} = 1$ V for 12 x (6.6/0.25) μm^2 FD and PD SOI n-MOSFETs.

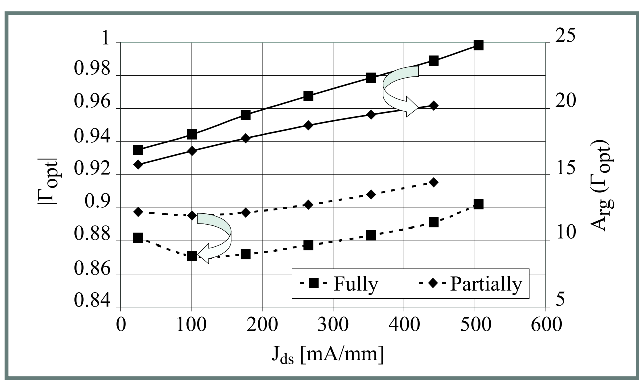

Fig. 13. Comparison between FD and PD SOI n-MOSFETs: evolution of Γ_{opt} as a function of the drain current density at 2 GHz; $V_{ds} = 1$ V; 12 x (6.6/0.25) μm^2.

By considering the very low value of NF_{min} at 6 GHz and its estimated measurement accuracy (±0.1 dB), the values and evolutions of NF_{min} for both FD and PD SOI transistors are similar. However, the extracted equivalent noise resistance R_n, which measures the sensitivity of the noise figure to change in the generator impedance, is slightly higher for PD SOI MOSFET (Fig. 14). More the value of R_n is low, more the minimum noise condition is easy to obtain in the case of LNA's design. As compared with a 0.6 μm channel length device [12], the value of R_n in Fig. 14 is three times lower.

Figure 15 represents the state-of-the-art results for different kinds of MOSFETs technologies. Low noise microwave performances of FD SOI MOSFETs appear to be ones of the best results reported in the literature.

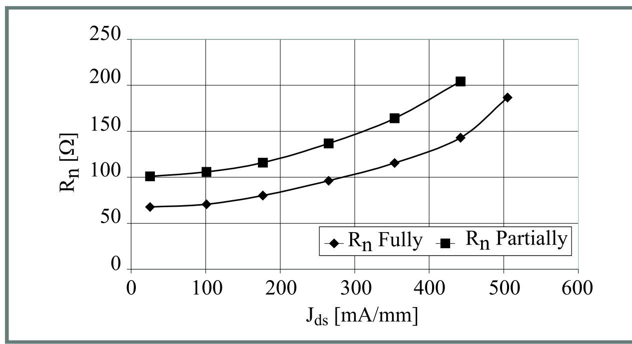

Fig. 14. Comparison between 12 x (6.6/0.25) µm² FD and PD SOI n-MOSFETs: evolution of R_n as a function of the drain current density at 6 GHz and $V_{ds} = 1$ V.

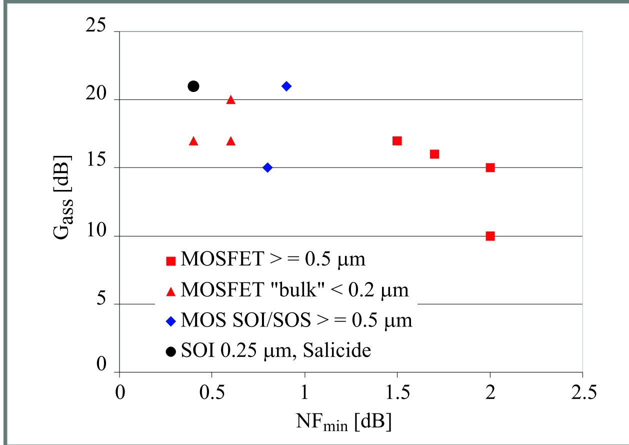

Fig. 15. State-of-the-art high frequency NF_{min} and G_{ass} for different published results of MOSFET technologies. Black dot corresponds to this work.

7. Conclusion

The microwave small-signal characteristics and the high frequency noise parameters for fully- and partially-depleted sub-quarter micron silicon-on-insulator MOSFETs are reported and compared. Slight improvements of nearly all small-signal and high frequency noise parameters are obtained with FD technology. Excellent microwave performances including high frequency noise have been obtained for 0.25 µm gate channel length FD SOI MOSFETs: a maximum extrapolated oscillation frequency (f_{max}) of 70 GHz and the state-of-the-art minimum noise figure (NF_{min}) of 0.8 dB with high available associated gain (G_{ass}) of 13 dB at 6 GHz, $V_{ds} = 0.75$ V, $P_{dc} < 3$ mW, have been measured.

These results render this type of devices suitable for low-voltage, low-power RF communication applications.

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Paper

Characterization of SOI fabrication process using gated-diode measurements and TEM studies

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Abstract — SOI fabrication process was characterized using electrical and TEM methods. The investigated SOI structures included partially and fully depleted capacitors, gated diodes and transistors fabricated on SIMOX substrates. From C-V and I-V measurements of gated diodes, the following parameters of partially depleted structures were determined: doping concentration in both n- and p-type regions, average carrier generation lifetimes in the region under the gate and generation velocity at top and bottom surfaces of the active layer. Structures with short lifetime were studied using a transmission electron microscope. TEM studies indicate that the quality of the active layer in the investigated structures is good. Moreover, these studies were used to verify the thicknesses determined by means of electrical characterization methods.

Keywords — microelectronics, SOI technology, characterization.

1. Introduction

The idea of the investigations was to use nondestructive electrical methods for determining the areas with the highest density of defects and then use TEM to determine the type of the defects. The carrier generation-recombination lifetime is the most sensitive indicator of semiconductor quality. Defects and impurities reduce carrier lifetime, therefore the structures with low lifetime were studied by TEM. The software developed by the authors enables not only carrier lifetime to be extracted from C-V and I-V characteristics but also layer thicknesses and doping concentration.

In our investigations we have used structures from two SIMOX wafers, **A** and **B**, differing in the thickness of the active layer. In both cases the gates were made of poly-Si. The structures fabricated on wafer **A** were partially depleted, while those fabricated on wafer **B** – fully depleted.

2. Electrical measurements

Initially the basic parameters of SOI structures were determined using C-V and I-V characteristics. The characteristics were measured simultaneously in order to reduce temperature related errors. Software with statistical methods implemented was used to reduce noise and disturbances for currents as low as 10^{-13} A.

Using the method described in [1] the thicknesses of the layers were calculated from C-V characteristics. The results are presented in Table 1.

The doping concentration versus depth for partially depleted SOI devices, calculated from C-V characteristics, is presented in Figs. 1 and 2. The dotted lines are placed

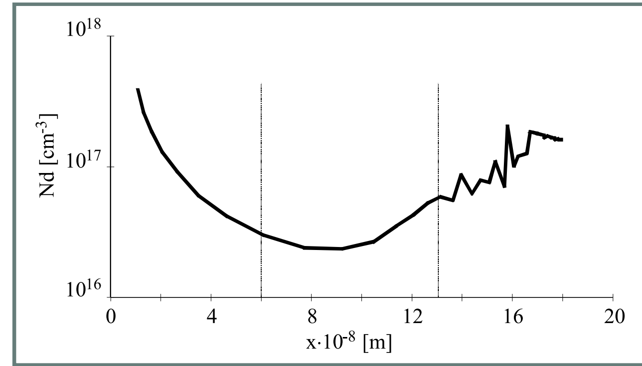

Fig. 1. Typical doping concentration versus depth for n-type area.

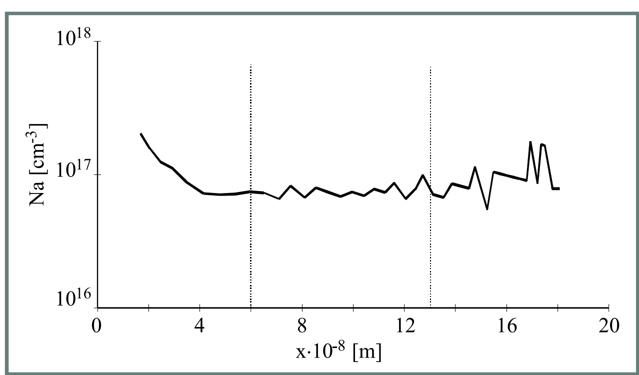

Fig. 2. Typical doping concentration versus depth for p-type area.

at the distance of three Debye lengths from top and bottom interface, therefore the results from the region within these lines should be correct. Also the average doping concentration was calculated. The following results were obtained: $Nd = 5.5 \div 8.6 \cdot 10^{16}$ [cm^{-3}] for n-type area and $Na = 7.3 \div 9.3 \cdot 10^{16}$ [cm^{-3}] for p-type area.

Using the method described in [2–4] the generation carrier lifetime and surface generation velocity in partially depleted structures were extracted from I-V characteristics measured

Table 1
The thicknesses calculated from C-V characteristics

Wafer	A [μm]	B [μm]
Gate oxide over the n-type region	0.031 ÷ 0.0325	0.0161 ÷ 0.0179
Gate oxide over the p-type region	0.032 ÷ 0.033	0.0175 ÷ 0.0177
Active layer of the n-type region	0.178 ÷ 0.185	0.080 ÷ 0.090
Active layer of the p-type region	0.184 ÷ 196	0.0776 ÷ 0.98

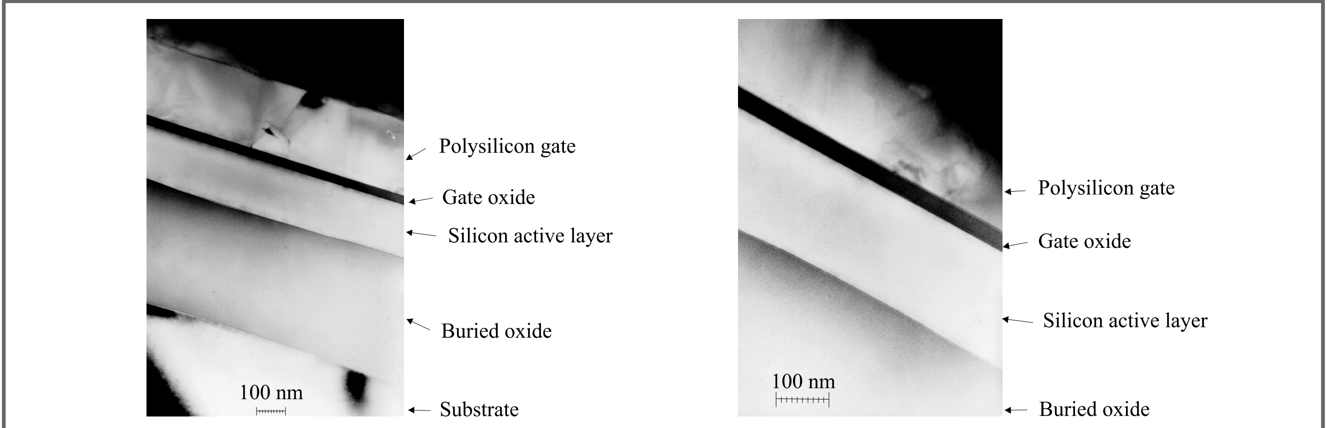

Fig. 3. Cross sectional TEM micrographs of type A SOI structures for two different magnification.

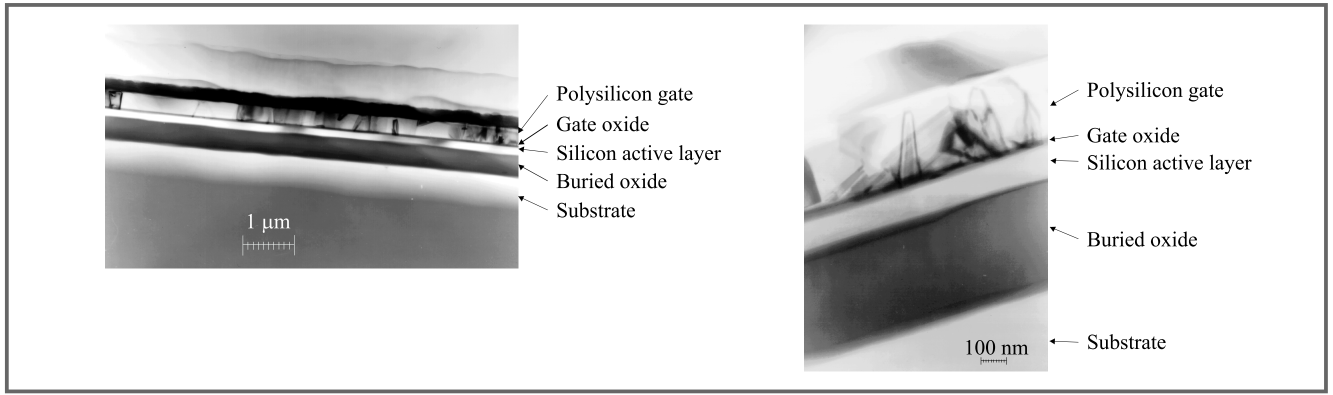

Fig. 4. Cross sectional TEM micrographs of type B SOI structures for two different magnification.

versus front gate voltage and back gate voltage. The calculation yielded generation lifetime $\tau_g = 0.45\ \mu s \div 0.6\ \mu s$ and the generation velocity at the front surface $s_g = 5.6 \div 9.1$ [cm/s] and the back surface $s_b = 5.1 \div 8.4$ [cm/s].

For fully depleted structures carrier recombination lifetime was calculated using the model described in [5]. The recombination time values ranged from 0.45 μs to 0.94 μs.

3. TEM studies

The structures with the minimum values of generation and recombination lifetime were investigated using TEM. The cross sectional TEM micrographs of both types of the structures A and B are presented in Figs. 3 and 4.

Although the investigated samples were prepared specifically to facilitate the observation of defects, no defects were observed in the active silicon layer. Only poly-Si grains were visible. Thickneses of the layers were determined from TEM micrographs. The results are presented in Table 2.

Table 2
The thicknesses determined from TEM micrographs

Wafer	A [μm]	B [μm]
Gate oxide	0.030 ÷ 0.032	0.0178 ÷ 0.018
Active silicon layer	0.18 ÷ 0.19	0.11 ÷ 0.12
Buried oxide	0.40 ÷ 0.42	0.35 ÷ 0.42

In case of partially depleted structures the agreement between the thicknesses determined electrically and those determined with TEM is excellent. However, in case of fully depleted devices the thickness of active layer measured electrically is too low. It is possible that for this case the thicknesses of accumulation and inversion layers must be

taken account. Gate oxide thickness obtained from TEM is probably too high because of the difficulties with precise determination of the layer edges.

4. Conclusions

The developed methods may be used to monitor the SOI fabrication process. The fundamental parameters of SOI devices are determined including the carrier lifetime – a comprehensive indicator of process quality. The software enabling very low currents to be measured and the whole measurement system may be used in many research areas. The developed method of preparing SOI samples for TEM studies at precisely determined locations of test structures increases the probability of observing defects in which the experimenter is interested. The method may be efficiently used to examine semiconductor materials.

Acknowledgement

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Andrzej Jakubowski – for biography, see this issue, p. 18.

Lidia Łukasiak, **Daniel Tomaszewski** – for biography, see this issue, p. 71.

Regular paper

Characterization of the indoor radio propagation channel at 2.4 GHz

Tadeusz A. Wysocki and Hans-Jürgen Zepernick

Abstract — The unlicensed industrial, scientific, and medical (ISM) band at 2.4 GHz has gained increased attention recently due to the high data rate communication systems developed to operate in this band. The paper presents measurement results of fading characteristics, multipath parameters and background interference for these frequencies. Some statistical analysis of the measured data is presented. The paper provides information that may be useful in design and deployment of communication systems operating in the 2.4 GHz ISM band, like those compliant with IEEE 802.11 standard and Bluetooth open wireless standard.

Keywords — indoor radiocommunication, microwave propagation, fading channels, jamming.

1. Introduction

Recently a number of data communication systems has been developed to utilize the unlicensed industrial, scientific, and medical band at 2.4 GHz [1]. The two most prominent examples of such systems are IEEE 802.11 wireless LAN [2], and personal area network employing Bluetooth enabled devices [3]. To assist in deploying of those systems, characterization of the indoor radio propagation channel at 2.4 GHz is essential. Measurement results for the indoor radio propagation channel have been presented in various publications. However, they tend rather to focus on a single characteristic, e.g. pulse propagation characteristic, as in [4], or temporal fading caused by motion of people and other objects within the channel [5], or simply deal with different frequency bands, like in [6].

In this paper, we present measurement results for the three major channel characteristics in the 2.4 GHz ISM band, i.e. temporal fading, channel impulse response, and background noise. The paper is organized as follows. Section 2 deals with the temporal fading characteristics. Example measurement results together with the cumulative distribution functions for typical measurements fitted to those of Rician distributions [7] are presented there. Level crossing rates and average duration of fades extracted from the measurements are included, too. Section 3 is devoted to the measurements of multipath channel parameters for the 2.4 GHz ISM indoor channel. In Section 4, the results of background interference measurements are shown, with microwave ovens indicated as major sources of an electromagnetic pollution in this band. Section 5 concludes the paper.

2. Fading characteristics

The measurements reported here were conducted at a laboratory of the Cooperative Research Centre for Broadband Telecommunications and Networking, Curtin University of Technology, Perth, Western Australia. The room topology is shown in Fig. 1. This environment was of relatively small dimensions being rectangular in size 7.8 m by 9.95 m within a three-metre ceiling. The ceiling was located 1.5 m below the steel reinforced concrete floor for the second storey of the four-storey building. The laboratory had two doorways and no windows. It had steel-framed walls clad with plaster-glass, a dropped ceiling constructed with non-metallic acoustic tiles, and a carpeted concrete floor. The laboratory was heavy cluttered with test and measurement equipment located on the benches.

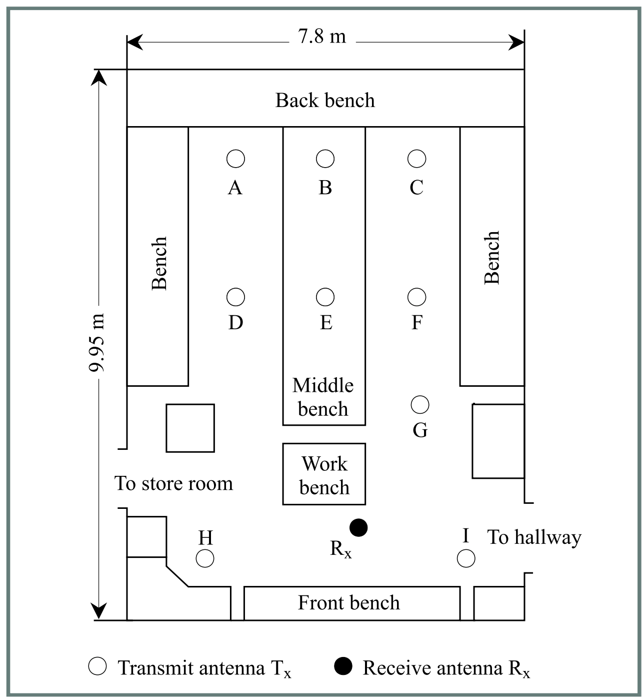

Fig. 1. Antenna placements for fading measurements.

2.1. Measurement procedure

We used the Hewlett Packard HP89441A to feed a quarter wave monopole antenna designed for the frequency range $2.3 \div 2.5$ GHz. The transmitter and the identical receiv-

ing antennas were mounted on two separate identical PVC pipes of heights adjustable in the range 1.0 to 2.0 m. At the receiver, a Marconi TF2300A modulation analyzer was applied to perform an envelope detection of the down converted baseband signal. The resultant signal was sampled, and the results stored on a hard disk for post-processing.

For all fading measurements, receive antenna R_x remained fixed and transmit antenna T_x was moved to different placements (Fig. 1). For each T_x placement and with no movement of people, the received signal was calibrated to -65 dBm. This receive level provided a signal to measurement system noise ratio of 35 dB, thus allowing fade depths of this order to be identified. To determine impairments caused by sources from outside the laboratory, we initially kept all motion in the room at zero. The variations of the received signal amplitude were less than ± 0.2 dB and could be regarded as insignificant. Then, we collected measurements for nine different transmit antenna locations with three people moving around the receive antenna only, keeping them within a two metre radius. The duration of measurements for each pair of antenna locations was twenty seconds. As an example, Fig. 2 shows a typical fading pattern observed with transmitt antenna T_x at the placement C.

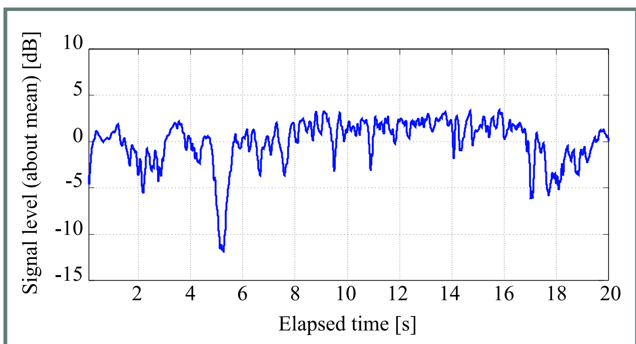

Fig. 2. Fading for transmit antenna at position C.

2.2. Fading distributions

In an indoor environment, we expect a line-of-sight path between transmit and receive antenna. Hence, the probability density function of the fast varying amplitude of the received instantaneous signal can be described by a Rician distribution. The probability that the received amplitude does not exceed a given threshold r is given by integration of the probability density function and is called cumulative distribution function $C(r)$. For curve fitting purposes, it is convenient to use the complementary cumulative distribution function $\overline{C}(r)$, which for a Rician distribution is given by [7]

$$\overline{C}(r) = 1 - C(r) =$$
$$= \exp\left[-\left(K + \frac{r^2}{2\sigma^2}\right)\right] \sum_{m=0}^{\infty} \left(\frac{\sigma\sqrt{2K}}{r}\right) I_m\left(\frac{r\sqrt{2K}}{\sigma}\right), \quad (1)$$

where $I_m(r)$ denotes the modified mth order Bessel function of the first kind, σ^2 is the local-mean scattered power, and K is called Rician factor specifying the ratio of power in the dominant path to power in the scattered path.

In calculating the empirical distribution functions, the measured data was classified into $\beta = 1.87(v-1)^{2/5}$ bins [8] where v is the number of samples collected in a measurement period. Then, a set of hypotheses for $\overline{C}(r)$ with $K = 0$ to $K = 15$ in 0.1 increments were tested to match the measured function. We applied the Kolmogorov-Smirnov goodness-of-fit technique for testing the relevance of match between measurement and hypothesis. Since the power level was normalized about median, a respective Rician factor K fully specifies a particular fading distribution. Table 1 shows the obtained Rician factors K.

Table 1
The Rician factors at various transmit antenna placements

Placement	A	B	C	D	E	F	G	H	I
K [dB]	2.79	8.19	9.86	5.95	8.80	3.80	8.26	7.85	5.79

Figure 3 shows curve fitting results for T_x at C. The large Rician factor of K = 9.86 dB indicates a strong line-of-sight path. Note also that the deviation between measured and matched distribution appears large for small power levels but is actually small due to scaling.

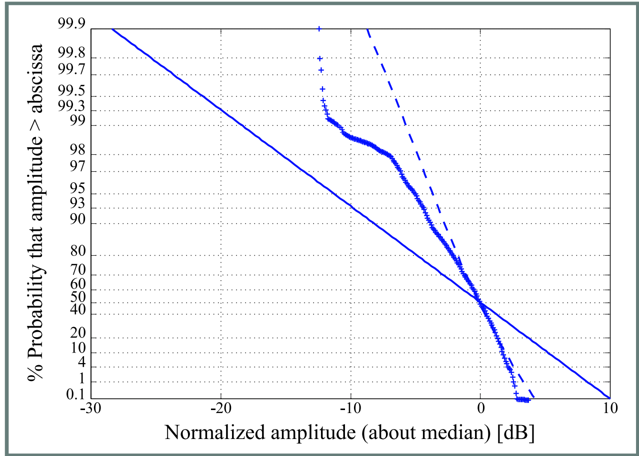

Fig. 3. Complementary cumulative distribution function $\overline{C}(r)$ for transmit antenna T_x at placement C; „+" fading measurement, „- -" Rician fading with K = 9.86 dB, „—" Rayleigh fading as reference.

2.3. Fading statistics

To design data and signaling formats for a wireless system, we require statistics which quantify the number of times a given threshold is crossed and the duration of time for which the signal is below that threshold. By counting all N crossings with positive slope at a given level L for mea-

surement period T, the level crossing rate can be computed as [9]

$$N_L = \frac{N}{T}. \qquad (2)$$

The average duration of fades $\bar{t}_L$ in respect to level L and measurement period T is given by [9]

$$\bar{t}_L = \sum_{i=1}^{N} \frac{t_i}{N}, \qquad (3)$$

where t_i is an ith fade duration, i.e. time for which the received signal is below a given level L. Table 2 displays fading statistics of selected fading measurements. Obviously, the average duration of very deep fades is rather short.

Table 2
Fading statistics for transmit antenna at selected placements

L [dB]	N_L [s^{-1}]			$\bar{t}_L$ [s]		
	C	E	I	C	E	I
6			0.101			9.868
3	0.554	2.195	2.526	1.765	0.363	0.290
0	1.308	2.147	3.183	0.295	0.141	0.118
-3	0.755	0.927	1.768	0.150	0.161	0.080
-6	0.151	0.781	0.859	0.158	0.121	0.092
-9	0.050	0.488	0.354	0.275	0.129	0.143
-12	0.050	0.439	0.303	0.008	0.092	0.131
-15		0.293	0.202		0.085	0.147
-18		0.195	0.202		0.091	0.110
-21		0.195	0.152		0.062	0.115
-24		0.098	0.152		0.069	0.079
-27		0.049	0.051		0.032	0.079

3. Multipath channel parameters

Delay profile measurements were conducted in the same laboratory as the fading measurements. However, this time the location of transmit antenna T_x remained fixed for all measurements, and the receive antenna R_x was placed at different locations within the laboratory. A plan view of the laboratory with the four antenna positions used for delay profile measurements is depicted in Fig. 4.

3.1. Delay profile measurements

Because of the confined environment, we could use the standard channel impulse response measurement system [10] based on the vector network analyzer HP 8753C equipped with an S-parameter test set HP 85046A. We used the same antennas as for the fading measurements. The results were recorded using HP VEE user interface and stored on a hard drive for post-processing. Albeit the 2.4 GHz ISM band spans from 2.4 to 2.485 GHz, we performed measurements in the band 2.1 to 2.8 GHz which gave us

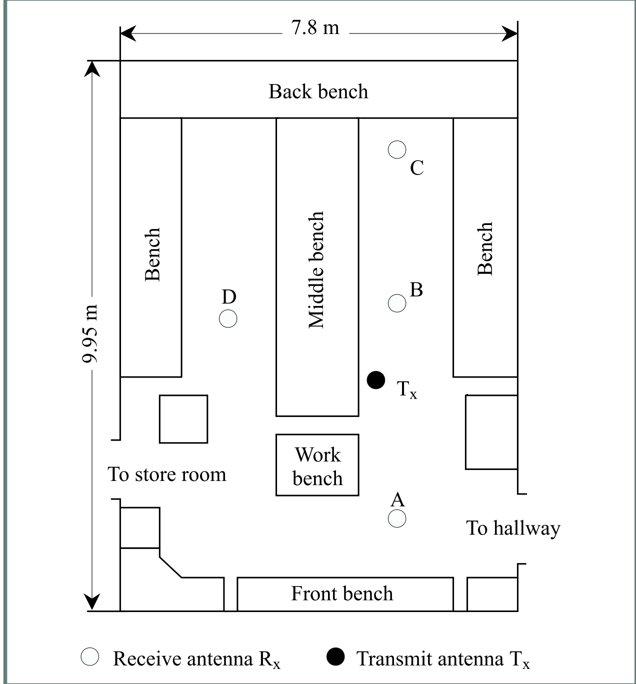

Fig. 4. Antenna placements for delay profile measurements.

a resolution of 837.05 mm, when normal window [11] was used. This translates into time resolution of 2.7921 ns.

During the measurement periods, three people kept moving in a similar manner around the receive antenna R_x, staying all the time within a two metre radius. Receive positions A, B and C were located within the left-hand aisle of the laboratory but with different distances to transmit antenna T_x. The specific characteristic of the receive position A was its direct vicinity to the nearby hallway which could cause additional scattering. In other words, time dispersion parameters at location A were expected to be of higher value than those observed at the three other locations. The particular feature of the receive location D was that the direct line-of-sight to the transmit antenna T_x did not exist because of the middle bench obstruction.

Figures 5 to 8 show the measured power delay profiles for the receive antenna R_x located at positions A, B, C, and D. The largest amplitude of each profile has been normalized to 0 dB.

3.2. Time dispersion parameters

It can be seen from the plots presented in Figs. 5 to 8 that a received wide-band signal will suffer spreading in time compared to the transmitted signal. This effect is called delay spread. Several delay-related parameters used for channel classification can be extracted from the measured power delay profile $P(\tau_\nu)$ where τ_ν denotes νth time instant.

The most commonly used time dispersion parameters are [12]:

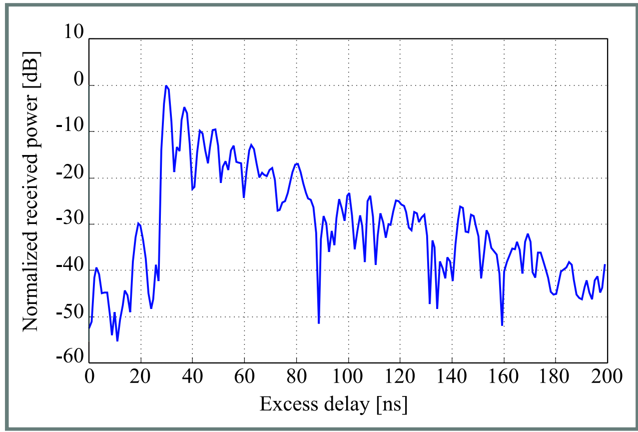

Fig. 5. Power delay profile for receive position A.

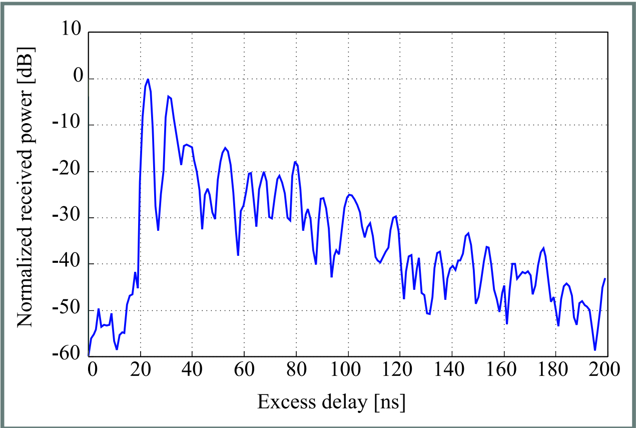

Fig. 6. Power delay profile for receive position B.

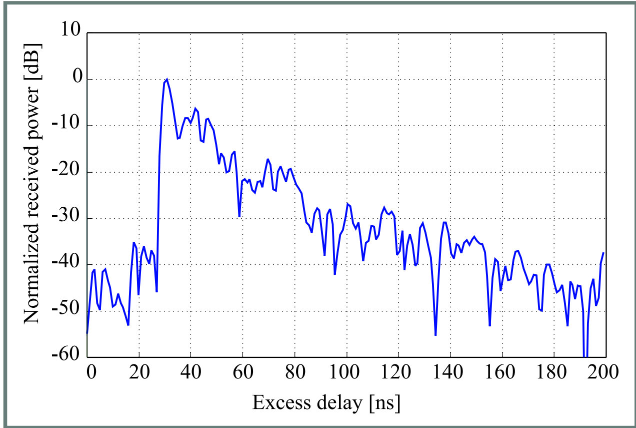

Fig. 7. Power delay profile for receive position C.

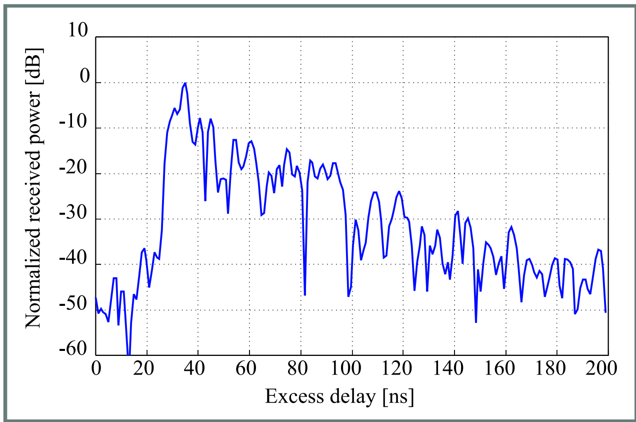

Fig. 8. Power delay profile for receive position D.

- Mean excess delay, which is the first moment of the power delay profile defined by:

$$m_\tau = \frac{\sum_\nu P(\tau_\nu)\tau_\nu}{\sum_\nu P(\tau_\nu)} \, . \tag{4}$$

- Root mean square (rms) delay spread, which is the square root of the second central moment of the power delay profile and is given by:

$$\sigma_\tau = \sqrt{\frac{\sum_\nu \left[\tau_\nu - m_\tau\right]^2 P(\tau_\nu)}{\sum_\nu P(\tau_\nu)}} \, . \tag{5}$$

- Maximum excess delay X [dB], defined as the time period during which the power delay profile falls to X [dB] below its maximum [10].

Note that mean excess delay and rms delay spread have to be computed with respect to a reasonable threshold for the multipath noise floor. If this threshold were set too low, it would result in too high values for these dispersion parameters. Our statistical analysis is based on a noise threshold set to four times of the noise standard deviation, which is known as a rule of thumb (as used in [13]). Numerically, the noise threshold was set to -34 dB with respect to the normalized receiver power.

A dual representation of delay spread in terms of a frequency domain parameter is given by the coherence bandwidth B_c. This parameter specifies the frequency range over which a transmission channel affects the signal spectrum nearly in the same way, giving an approximately constant attenuation and a linear change in phase. The coherence bandwidth is inversely proportional to rms delay spread. Assuming frequency correlation between amplitudes of frequency components being above 0.9, the coherence bandwidth can be approximated by [9]

$$B_c \approx \frac{1}{50\sigma_\tau} \, . \tag{6}$$

The time dispersion parameters extracted from the measured power delay profiles are summarized in Table 3. As we expected, the mean excess delay at receive position A is higher than at B and C which was assumed to be caused by multipath scattering into the nearby hallway. It is interesting to note that at the receive position D, we obtained the highest value of maximum excess delay in respect to 20 dB threshold from 0 dB power level. This is likely a result of the missing line-of-sight path at receive position D.

Table 3
Time dispersion parameters for receive antenna at various placements

Placement	A	B	C	D
Mean excess delay [ns]	57.04	43.40	49.10	54.85
Rms delay spread [ns]	30.55	24.12	22.19	26.82
Max excess delay 20dB [ns]	53.73	59.73	50.74	66.67
Coherence bandwidth [kHz]	654.66	829.19	901.31	745.71

4. Background interference

One of the important aspects of channel characterization is classification of noise and interference sources that need to be taken to account in the given bandwidth. This is particularly important in the case of unlicensed bands, as is the case of the 2.4 GHz ISM band, where users of wireless technologies operating in these bands are not required to obtain operating licenses provided that higher gain antennas are not used. On the other hand, there are no guarantees that the band is free of interference.

To identify the possible noise and interference sources that can affect use of the 2.4 GHz ISM band for communication purposes, we performed a series of measurements in some typical operating environments, including a university campus, a large shopping centre, and an industrial workshop. We used Hewlett Packard Spectrum Analyzer HP 8595E with a colinear antenna for omnidirectional measurements and a corner reflector antenna for directional measurements, i.e. when the particular source had been identified.

After conducting those measurements, we identified one major class of interference sources radiating in the 2.4 GHz ISM band, which were microwave ovens. Apart from that, the band was almost clear. The only other interference sources were building alarms as those used typically in businesses. Although only discovered in two cases from various measurement sites, they were found to output discrete frequency signals of moderate to low levels. The radiation came from the alarm units themselves (the most likely from oscillator circuits), and not the sensors, as they operated at infrared frequencies. A typical spectrum analyzer trace taken at a distance of 1 m from the alarm unit, with the directional corner reflector antenna is given in Fig. 9. The reading was obtained at Wilson's Engraving Works in Perth, Western Australia.

Microwave ovens were identified as major sources of interference at both the university environment and the shopping mall. The spectrum analyzer trace obtained from the 2 m measurements, using the directional corner reflector antenna and „peak-and-hold" function of the analyzer, is shown in Fig. 10. The plot presents raw data only. To derive the exact values of interference level from the trace it is necessary to account for system gains and losses.

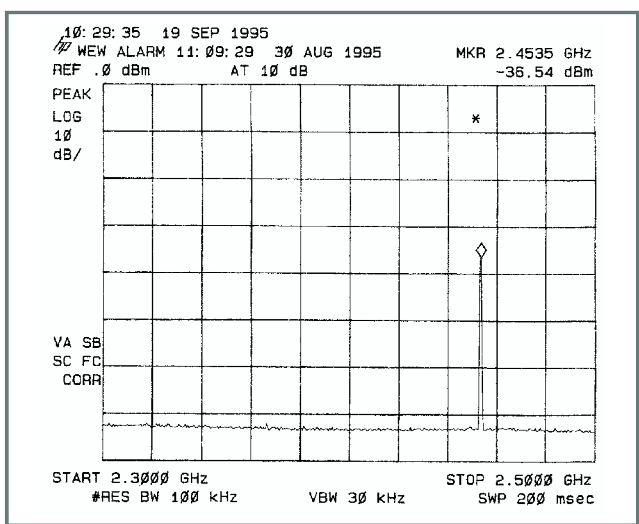

Fig. 9. Sample spectrum analyzer output for an alarm unit.

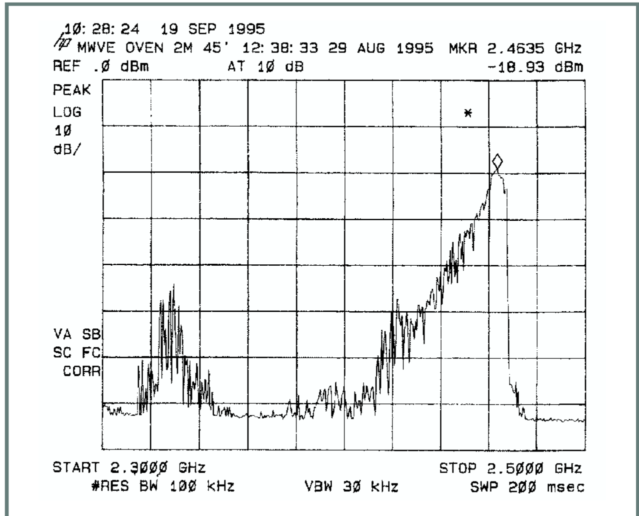

Fig. 10. Sample spectrum analyzer output for a single microwave oven at 2 m using the corner reflector antenna.

The plot of Fig. 10 shows a typical signature of the leakage output spectrum for a microwave oven. Brief analysis of two other microwave ovens, demonstrated that they at least (and presumably most others) share a similar signature of leakage output spectrum, both in intensity (related to efficiency and sealing of microwave) and spectrum occupation. Considering microwave ovens operating in multiplicity, the omnidirectional measurements were taken. This was deemed so, because of the multitude of signals and many reflective surfaces from which they could bounce in the Whitford City Shopping Centre Food Hall. It was impossible to selectively determine the source of any one signal since there were many food outlets operating microwave ovens simultaneously. Rather, the various microwave oven output signals combined producing a composite interference environment, that could only be measured with relevance with an omnidirectional antenna.

Figure 11 shows a typical output trace for the food hall environment. Once again, the trace provides us with a spectral

signature of the environment. It has the usefulness of providing a good indication of what spectrum one can expect in such a topology, with respect to frequency variation and interference intensity. The trace is actually similar to the one presented in Fig. 10, except that the noise is spread more evenly over the entire ISM band, as a result of the differing characteristics of the various microwave ovens. However, it is still possible to notice the peak in noise power between $2.4 \div 2.47$ GHz, which is directly coincident with the band of interest for microwave wireless LAN's.

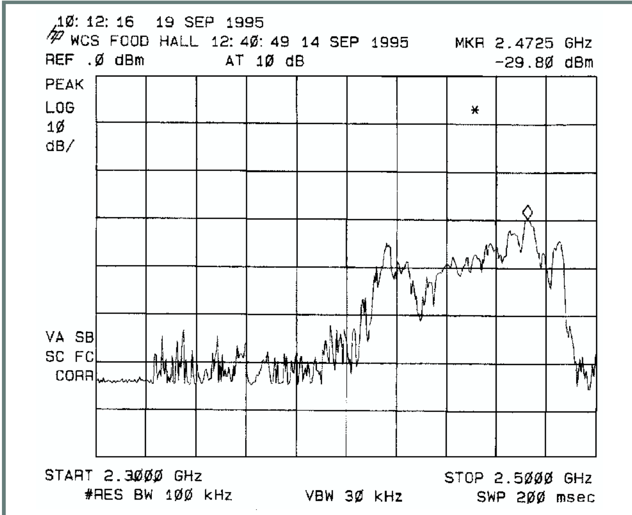

Fig. 11. Sample spectrum analyzer output for multiple microwave oven environment using omnidirectional antenna.

Both plots presented in Figs. 10 and 11 indicate that microwave ovens generate interference of a considerable level in the whole 2.4 GHz ISM band. The plots were obtained using „peak-and-hold" function of the analyzer. The instantaneous output of the analyzer revealed that the single operating microwave oven generated a single tone signal with the frequency hopping within the whole bandwidth. Therefore, one can expect the direct sequence (DS) spread spectrum (SS) devices, like DS mode of IEEE 802.11 wireless LAN, should perform quite well even in the close proximity to operating microwave ovens. On the other hand, the frequency hopping (FH) SS devices, like the Bluetooth compliant ones might experience difficulties in such an environment.

5. Conclusions

In this paper, we presented the measurement results, which can be used to characterize the 2.4 GHz unlicensed ISM band from the viewpoint of its usefulness for high data rate communications. The reported measurements deal with characteristics of fades and multipath channel parameters. In addition, special considerations are given to identifying possible sources of interference present in this band. The fading characteristics as well as multipath parameters were measured at one location that was a heavy cluttered laboratory. Thus, the presented results can be used to characterize indoor environment. The background interference measurements were performed at several different locations. The only major source of interference identified were microwave ovens, which based on the results, can have significant impact even on some SS systems. Because of the nature of this interference, it can be expected to particularly impair signal quality in FH SS systems, like Bluetooth enabled devices.

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