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**Part II**

# *Editorial Board*



# *Editorial Advisory Board*




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# *Preface*

Rumors about forthcoming twilight of silicon-based microelectronics seem to be exaggerated. Microelectronics has been continuously developing for the past three decades – for instance every three years a new generation of memories becomes available on the market with the capacity four times larger than that of the previous generation. The current „official" development forecast published by SIA (Semiconductor Industry Association) reaches ahead to the years 2012-2015. There are, however, more aggressive forecasts available that reach even as far as the year 2020.

While the development of silicon microelectronics in the past could be attributed mostly to the reduction of the feature size (progress in lithography), today it relies more on new material solutions, such as SOI, SiGe or SiC. The combination of this trend with continuous miniaturization provides the opportunity of moving into the range of very high frequencies.

Silicon microelectronics for fast analog and RF circuits, as well as for mainstream wireless and computational applications – these are the new application areas in telecommunications, which is one of the most powerful drivers of microelectronics product development. It is clear that with the anticipated $f_{max} \approx 50$ GHz and $f_T = 40$ GHz to be reached by RF transistors in 2005, according to the International Technology Roadmap for Semiconductors (SIA, 1999), a lot of effort must be put into the development of appropriate material, processing, characterization and modeling. However, such an outstanding progress will not happen without increased speed offered by new material solutions. As is generally known, carrier mobility in SiGe is several times higher than in silicon due to internal strain. On the other hand, higher speed of operation in SOI devices is achieved mainly due to the reduction of parasitic capacitances.

High-speed is, however, not everything. Portable wireless products push, for obvious reasons, for low-power solutions. This trend, too, requires new material, such as SOI where current drivability is higher than in conventional devices due to reduced thickness of the active region.

In this volume the Reader will find a selection of papers and lectures (part II of two parts) presented during the conference „Advanced Silicon Devices and Technologies for ULSI Era", which took place in Museum of Earth, Warsaw, Poland on 28–30 June 2000. A number of these papers are devoted to the performance of state-of-the-art semiconductor devices and sensors, in certain cases intended for highly-specialized applications, e.g. Atomic Force Microscopy. A lot of attention is also paid to the studies of the physical properties of such materials as e.g. porous silicon or amorphous silicon. The much-investigated subject of ultrathin gate dielectrics is covered, too. Finally, there are several papers devoted to device modeling.

We hope that Readers will find these Proceedings useful and interesting.

Guest editors: Andrzej Jakubowski, Aleksander Werbowy, Lidia Łukasiak

*Invited paper*

# SiGe field effect transistors – performance and applications

Terrence E. Whall and Evan H. C. Parker

**Abstract — Recent and encouraging developments in Schottky and MOS gated Si/SiGe field effect transistors are surveyed. Circuit applications are now beginning to be investigated. The authors discuss some of this work and consider future prospects for the role of SiGe field effect devices in mobile communications.**

***Keywords — SiGe, FETs, epitaxy, circuits.***

## 1. Introduction

SiGe heterostructures are now firmly established in bipolar technologies, with a current market value of £30M per annum rising to £1.83B by 2005, driven by the wireless and optical communications sector [1]. SiGe also offers the exciting prospect of similar or even bigger commercial benefits in Si field effect transistors. The reasons for this optimism are based on the substantial gains in room temperature effective mobilities, shown in Figs. 1, 2 and 3, which accrue from strain-induced band structure modifications [2–4] in silicon, SiGe alloy and germanium epilayers. In this article, we examine the resulting performance gains in a number of devices based on these heterostructures, discuss some other potential benefits of a SiGe technology, and briefly survey some circuit applications.

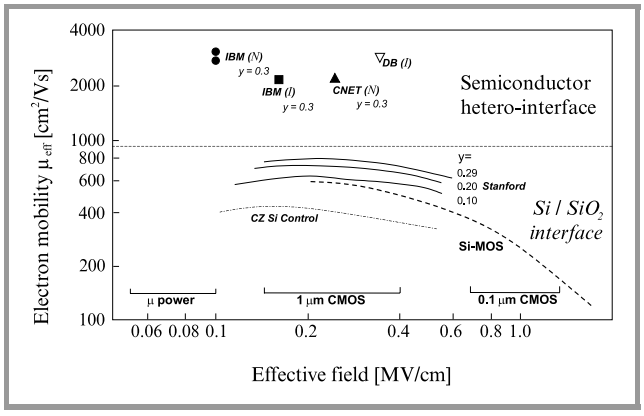


***Fig. 1.*** Available experimental data on 300 K electron mobilities in strained Si grown on virtual substrates with terminating composition $Si_{1-x}Ge_y$ versus the effective field $E_{eff}$ [2, 3]. $E_{eff} = \frac{e}{\varepsilon_s}\left[N_{depl} + \frac{1}{\beta}n_s\right]$ where $\varepsilon_s$ is the absolute permittivity of Si, $N_{depl}$ is the depletion charge density, and $n_s$ is the carrier density. The upper section shows mobilities at remote doped hetero-interfaces and the lower section refers to oxide-gate/(tensile strained) Si interfaces. *I* denotes „inverted" modulation-doped structure (doping supply layer below strained silicon) and *N* denotes „normal" interface case (doping above silicon). The oxide-gated structures are operated in the inversion mode. Here $\beta = 2$.

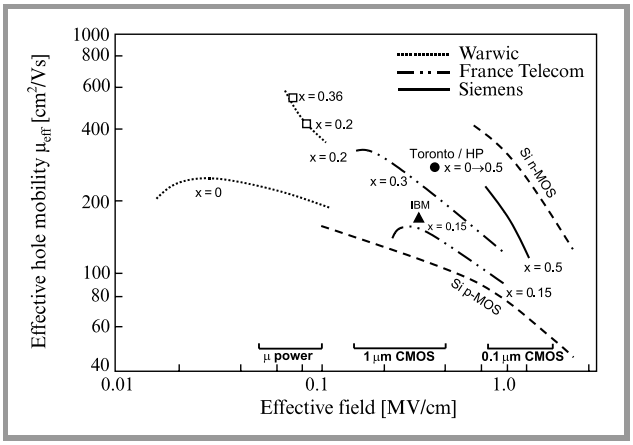


***Fig. 2.*** Available experimental data on 300 K hole effective mobilities obtained in pseudomorphic $Si/Si_{1-x}Ge_y/Si$ structures plotted against effective field ($E_{eff}$), all data refer to buried SiGe channels except for the IBM sample where the gate dielectric was produced by plasma oxidation. The alloy composition in the Toronto/HP sample was graded. The squares refer to modulation-doped structures. The bars indicate the range of $E_{eff}$ values present in micropower, 1 and 0.1 $\mu$m CMOS technologies. $\beta$ is usually taken as 3 for holes [6], in order to obtain an universal curve independent of doping specifications. That practice is followed here, but we note that this tends to over-emphasise the superiority of the electron channel where $\beta$ is chosen as 2.

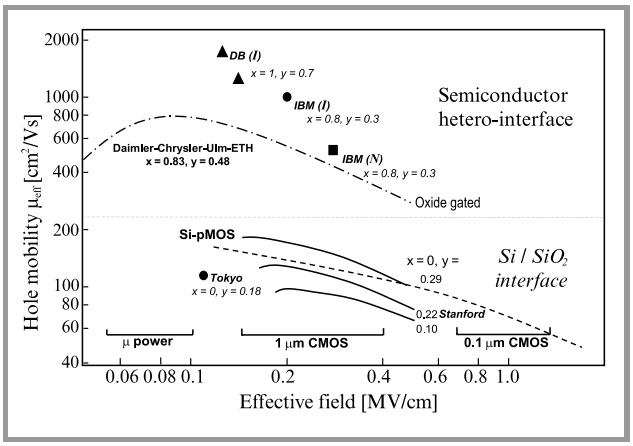


***Fig. 3.*** Available experimental data on 300 K hole mobilities obtained in compressively strained $Si_{1-x}Ge_y$ and tensile strained Si grown on virtual substrates with terminating composition structures $Si_{1-x}Ge_y$. The upper section shows mobilities for remote doped hetero-interfaces and the lower section refers to oxide-gate/(tensile strained) Si interfaces. *I* denotes „inverted" and *N* denotes „normal" interface. The oxide-gated data refer to inversion layers. $\beta = 3$.

## 2. Strained silicon n-channel devices

Ismail et al [5] have fabricated an 0.4 $\mu$m gate length Schottky gated modulation doped FET or n-MODFET with a peak transconductance of 420 mSmm$^{-1}$, an $f_T$ of 40 GHz and an $f_{max}$ of 56 GHz, comparable to GaAs/AlGaAs HEMTs of the same gate length. Figure 4 shows a typical Si/SiGe n-MODFET, designed and fabricated by the Daimler-Chrysler group [6]. The strained Si is supplied

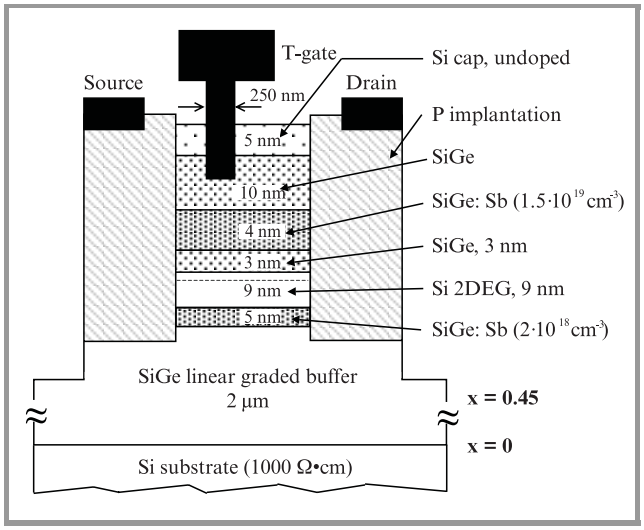


***Fig. 4.*** Schottky gated modulation doped n-channel FET (n-MODFET). The conduction band offset in the strained Si layer confines electrons. The T gate recess determines the threshold voltage, allowing either d-mode or e-mode operation (*after Glück et al. [6]*).

with carriers by SiGe:Sb doped layers above and below the quantum well. The device can operate in either depletion or enhancement mode depending on the depth of the Pt/Au Schottky gate recess, with a deeper recess in the latter case. An 0.25 $\mu$m d-mode device gives a measured $f_T$ of 70 GHz and an $f_{max}$ of 120 GHz (*U. König, private communication*). Simulations [7] suggest transconductances up to 1000 mSmm$^{-1}$ and transit frequencies $f_T$ above 200 GHz in self aligned layouts with gate lengths $< 0.1$ $\mu$m. Figure 5 shows the simulations of $f_T$. It is apparent that velocity overshoot plays an important role at gate lengths of 0.1 $\mu$m and below, particularly in the heterostructure.

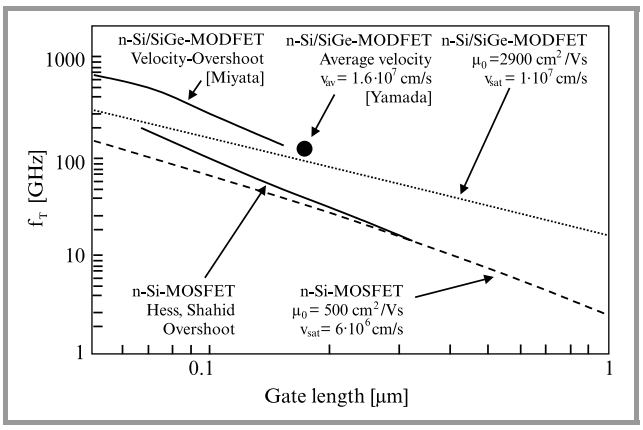


***Fig. 5.*** Simulated transit frequencies of SiGe n-MODFETs compared to ordinary SiGe n-MOS (*after König et al. [7]*).

The Stanford group have used CVD at 750°C to grow a strained Si channel on a relaxed $Si_{0.8}Ge_{0.2}$ strain-tuning virtual substrate (VS), and have fabricated an n-MOSFET of channel length 0.1 $\mu$m [8]. This is illustrated in Fig. 6a. The VS is in-situ boron-doped to create a punchthrough stopper doping profile surrounded by $Si_{0.8}Ge_{0.2}$ of lower doping. A very steep profile is possible because the boron diffusivity in both strained and relaxed $Si_{0.8}Ge_{0.2}$ is 8 times lower than in bulk Si. In the unstrained Si control sample SiGe boron diffusion barriers are placed either side of the p-layer, as shown in Fig. 6b. The doping profiles obtained

give comparable short channel behaviour in heterostructure and control with a DIBL value of approx 0.8, threshold voltage shift of approx 0.1 V and subthreshold slope of 103 ÷ 110 mV per decade. Transconductance enhancement in the heterostructure device is 60%, and average velocity (a measure of $f_T$) 67% as shown in Fig. 7. This improved performance [9] corresponds to a mobility enhancement of 70% at an effective field as high as 1 MV/cm and substantial velocity overshoot associated with a 100% increase in the energy relaxation time.

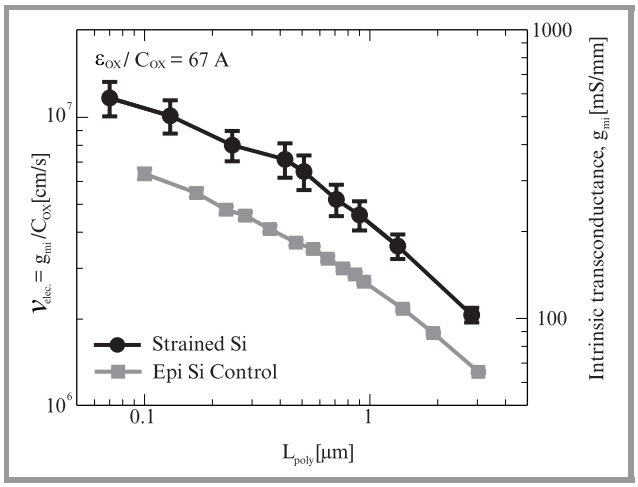


***Fig. 7.*** Average channel velocities and intrinsic transconductances of the devices shown in Fig. 6 (*after Rim et al. [8]*).

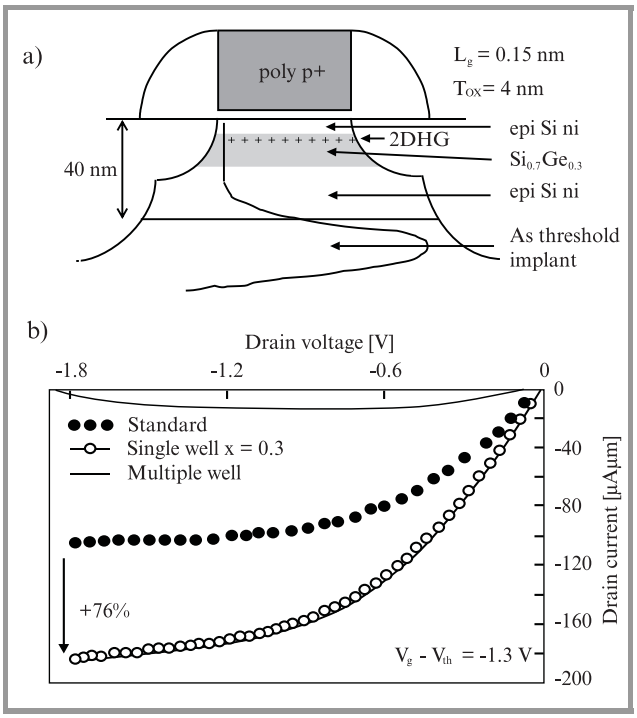


***Fig. 8.*** Device architecture (a) and current drive capability (b) of fully pseudomorphic $Si/Si_{0.7}Ge_{0.3}$/Si p-MOSFET. The valence band offset relative to silicon confines the carriers in the alloy. Also shown is the current drive enhancement as compared to silicon for a Si/SiGe multi quantum well structure (*after Alieu et al. [11]*).

## 3. Strained $Si_{1-x}Ge_x$ ($0 \leq$ and $\leq 1$) p-channel devices

Modern circuits for analogue and digital performance demand both n- and p-channel devices but the poor performance of the latter is an impediment to even better circuitry. Indeed, a major theme at the recent (December 1999) *International Electronic Devices Meeting (IEDM)* concerned the Si p-MOS device, which is the Achilles heel of Si CMOS. Factors of two or more reduction in current drive or transconductance as compared to Si n-MOS were reported in about a dozen papers concerned with deep submicron devices (50 nm $< L_{eff} \lesssim$ 100 nm) and theoretical work [10] indicated that the factor of two represented a lower limit. SiGe offers a unique opportunity to obtain matching n- and p-channel performance for the first time.

The fully pseudomorphic Si/SiGe/Si sandwich structure, because of its simplicity, has received a lot of attention for enhanced p-channel performance. It is a relatively defect-free structure which avoids the problems associated with the $Si_{1-y}Ge_y$ virtual substrate of long growth times and comparatively poor thermal conductivity. The CNET group have fabricated [11] such a device within an 0.15 $\mu$m CMOS process and this is sketched in Fig. 8a. It uses a $p^+$ poly-gate with a 4 nm gate oxide, and In or As implants for threshold voltage adjustment. They obtain a 76% improvement in current drive compared to a bulk silicon standard, as shown in Fig. 8b. The Cornell group report an $f_T$ of 23 GHz and an $f_{max}$ of 35 GHz in $Si/Si_{0.6}Ge_{0.4}$/Si 0.2 $\mu$m gate length p-MOS device [12]. They compare their $f_T$ value with measurements on a bulk Si n-MOSFET of similar geometry, which gave 32 GHz. A novel solid-phase epitaxy process has been used [13] to form an ultra thin body SOI p-channel $Si/Si_{0.7}Ge_{0.3}$ MOSFET, which is shown in Fig. 9a. Negligible threshold voltage roll-off and a subthreshold slope of 100 mV/dec is obtained for a channel length of 50 nm. The incorporation of SiGe in the channel (graded from 0 at the bottom to 30% at the top) results in a 70% enhancement in drive current, Fig. 9b. The authors note that further increases in drain current can be expected if the series resistance is reduced by process optimisation.

A Glasgow/Loughborough/Warwick team have been investigating the factors which limit current drive and transconductance in SiGe p-MOS devices. Measurements on an $x = 0.5$ structure of uniform composition, fabricated at Infineon (Munich), Fig. 10, have been compared with theory by Kearney et al. [14] and it is concluded that interface roughness rather than alloy scattering dominates the mobility at both 4 K and 300 K. Further arguments in favour of this viewpoint are given by Whall and Parker [15]. Figure 11 shows measurements of effective mobility by Palmer

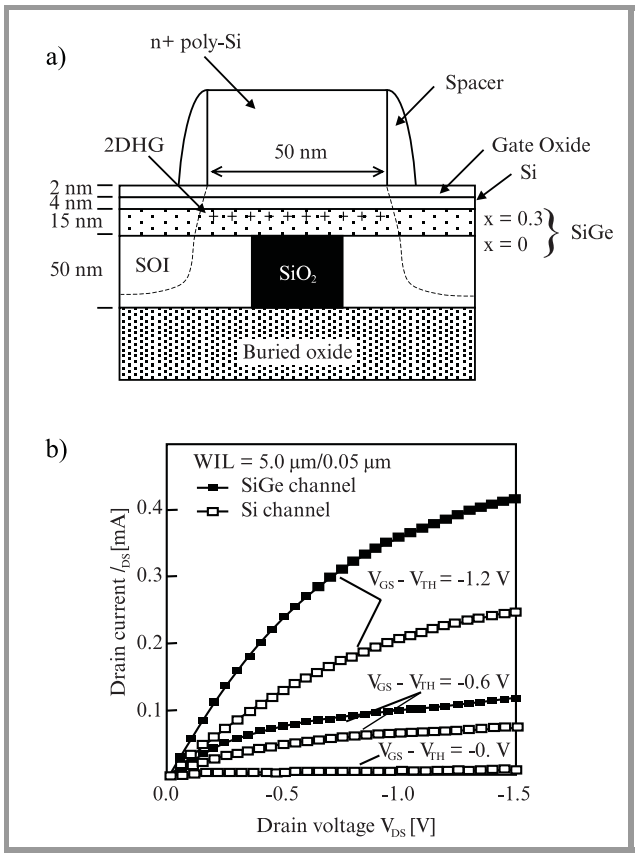


***Fig. 9.*** (a) Ultra-thin-body silicon on insulator MOSFET incorporating SiGe strained layer. A trench is formed in the SOI wafer, $Si0_2$ is deposited by low-pressure CVD and then SiGe is deposited and crystallised by solid-phase epitaxy. The broken lines indicate the boundaries of the source and drain islands. (b) Showing 70% enhancement in current drive as compared to silicon (*after Yee Chia Yeo et al. [13]*).

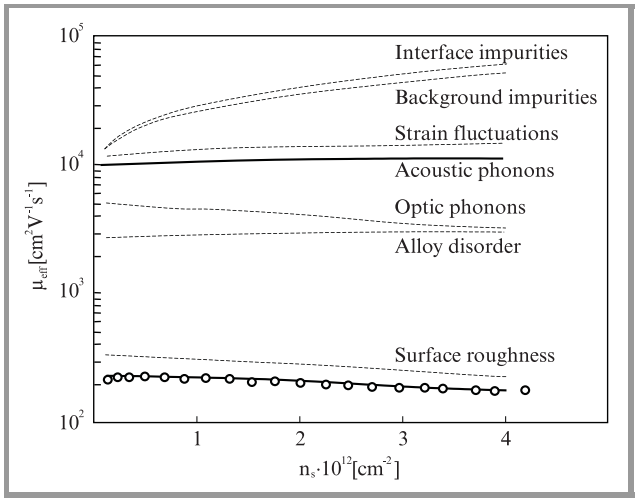


***Fig. 10.*** Room temperature effective mobility of a $Si/Si_{0.5}Ge_{0.5}/Si$ p-MOSFET versus carrier density. O experiment: broken lines theory, continuous line resultant theoretical mobility (*after Kearney et al. [14]*).

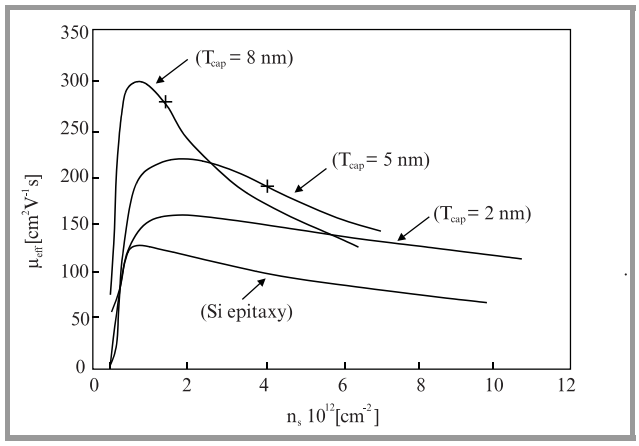


***Fig. 11.*** Measurements of effective mobility versus carrier density in $Si/Si_{0.64}Ge_{0.36}/Si$ p-MOSFETs of various Si cap thicknesses, compared with a Si control. The crosses indicate the onset of parasitic conduction in the Si cap (*after Palmer et al. [16]*).

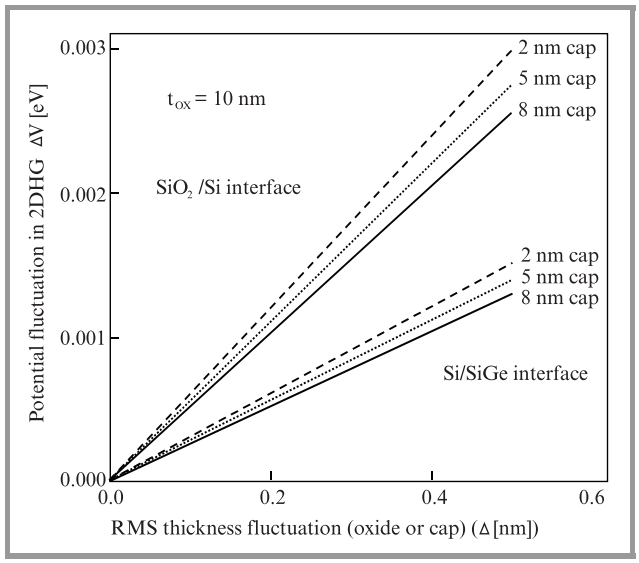


***Fig. 12.*** Coulomb potential fluctuations in the $Si_{0.64}Ge_{0.36}$ quantum well due to random thickness variations in the oxide and Si cap layers, giving rise to interface roughness scattering. A carrier density of $1 \cdot 10^{12}$ cm$^{-2}$ is chosen to avoid the complication of parasitic conduction in the silicon cap (*after Palmer et al. [16]*).

et al. [16] on $x = 0.36$ devices of various Silicon cap thicknesses. They argue that, for the devices in question, the potential fluctuations in the SiGe channel which limit the mobility, Fig. 12, are associated mainly with $Si0_2/Si$ as opposed to Si/SiGe interface roughness, in contrast to what is usually claimed. Ge segregation during growth and/or diffusion during processing degrades the $Si/Si0_2$ interface, presumably because of snowploughing of the Ge during oxidation, leading to increased roughness scattering. Thicker silicon caps lead to better $Si0_2/Si$ interfaces and higher peak mobilities. At high carrier densities, however, the thicker Si caps are populated, leading to a fall in effective mobility. A device configuration which has merit, is shown in Fig. 13. It uses an $n^+$ poly-Si gate and a B doping layer beneath the SiGe channel to suppress parallel conduction

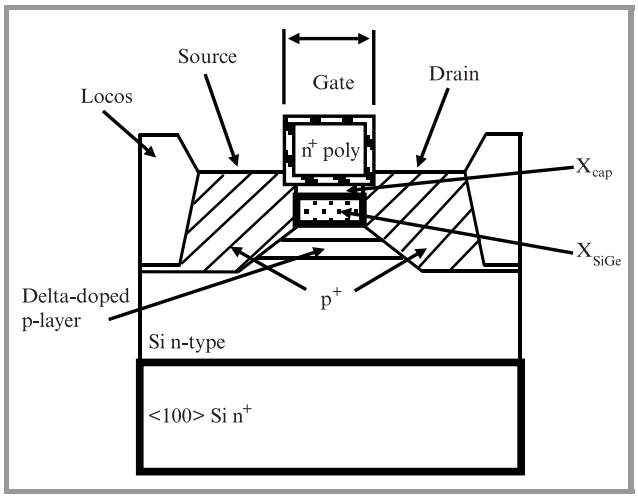


***Fig. 13.*** p-channel Si/SiGe/Si e-mode MOSFET with $n^+$ poly Si gate and Si:B doping layer to reduce effective (vertical) field and allow thicker Si cap.

in the cap while maintaining a low threshold voltage for enhancement mode operation. Because a thicker silicon cap becomes possible, it should be more tolerant of any Ge segregation. The B doping layer reduces the vertical effective field $E_{eff}$, which should give higher mobilities. Co-evaporation of C is being used by the Warwick group to stabilise the B against segregation and also diffusion. The velocity field characteristics reported by Kaya et al. [17] on an $x = 0.2$ SiGe p-MOS device, and reproduced in Fig. 14, are consistent with the view that, although the bulk saturation velocity in SiGe is less than that in Si, velocity overshoot affects dominate at short channel lengths and are responsible for the enhanced device performances discussed above. Zhao et al. [18] confirm this behaviour and also report that the observed velocity overshoot effects increase with mobility. Further improvements in device performance should be possible by engineering the doping

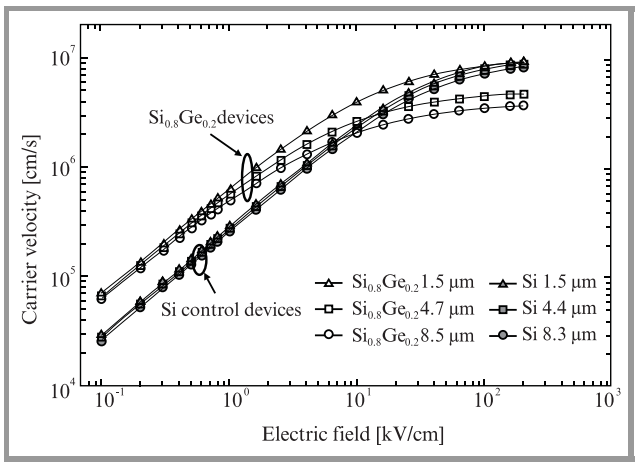


***Fig. 14.*** Carrier velocity versus horizontal field, extracted from measurements on thick oxide (140 nm) $Si_{0.8}Ge_{0.2}$ p-MOSFETs and by comparison with a drift diffusion model (*after Kaya et al. [17]*).

distributions to increase the velocity at the source end of the channel.

A number of other factors could tip the scales in favour of SiGe. The increased solid solubility and low diffusivity of B in SiGe promises shallow low resistance source and drain contacts [19]. SiGe sources have been demonstrated to suppress parasitic bipolar action and punchthrough [20, 21]. Poly SiGe gates [22] exhibit reduced gate-depletion, reduced boron penetration and give increased current through reduction of $E_{eff}$. Measurements by the Warwick group on a Siemens $Si/Si_{0.5}Ge_{0.5}/Si$ p-MOSFET give two orders of magnitude improvement in the relative $1/f$ noise, as shown in Fig. 15, which may be associated with the displacement of the Fermi level in the heterostructure [23].

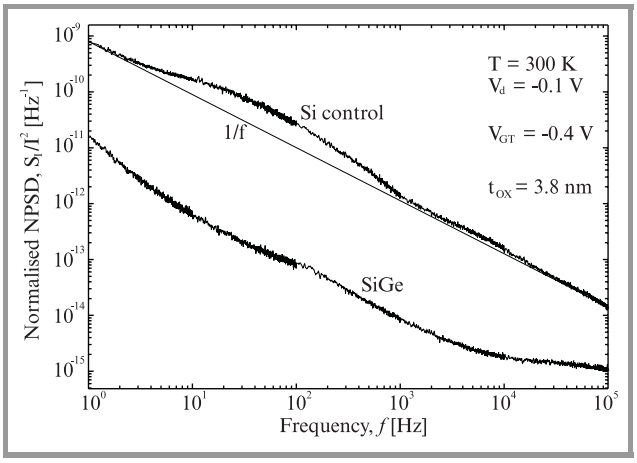


***Fig. 15.*** Showing two orders of magnitude improvement in relative noise power spectral density (NPSD) in a $Si/Si_{0.5}Ge_{0.5}/Si$ MOSFET as compared to a Si control (*after Prest et al. [23]*).

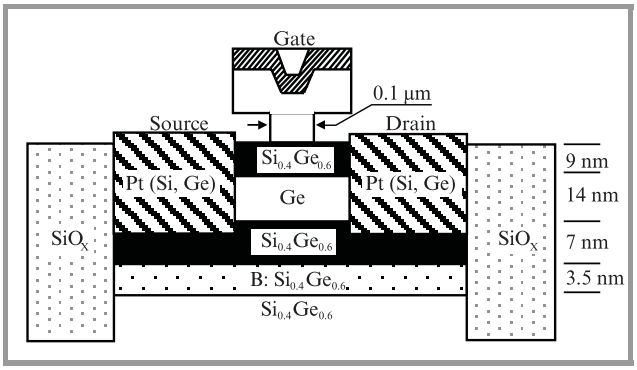


***Fig. 16.*** 0.1 $\mu$m gate length strained Ge p-MODFET. Contact pad metallisation not shown (*after Hammond et al. [26]*).

Even more dramatic performance enhancements might be expected in high Ge content and pure Ge strained layers on VS. The Daimler-Chrysler group et al. [24] have fabricated strained $Si_{0.3}Ge_{0.7}$ and Ge p-MOS and p-MODFETs on VS. A novel Ge p-MOS device yielded an $f_T$ of 59 GHz and an $f_{max}$ of 126 GHz at a gate length of 0.1 $\mu$m (*U. König, private communication*). The $f_T$ value is close to that in ordinary Si n-MOS [25]. A recent IBM 0.1 $\mu$m Ge p-MODFET is shown in Fig. 16. Transconductances of up

to 488 mS/mm at a drain source voltage as low 0.6 V were obtained [26]. For comparison ordinary 0.1 $\mu$m Si p-MOS exhibits a transconductance of 320 mS/mm at 1.5 V [25]. An 0.15 $\mu$m self aligned $Si_{0.2}Ge_{0.8}$ p-MOS structure, using SiN for the gate dielectric [27], displayed a maximum transconductance of 305 mS/mm an $f_T$ of 62 GHz at low drain source voltage of 0.75 V (compared to approximately 30 GHz at 1.5 V in Si [25]) and an $f_{max}$ of 68 GHz.
We have omitted to mention strained p-channel FETs in this article, which have also shown promise. The reader is referred to the review of Maiti and co-workers [29].

## 4. Some potential circuit applications

n-type Si/SiGe MODFETs promise improved performances comparable to III-V based circuits in analogue RF circuits and could play an important role in communication systems where they might be used as, for example, front and photoreceivers or low noise amplifiers. Saxarra et al. [29] have fabricated a transimpedance amplifier, based on the n-MODFET described in Section 2, the circuit of which is shown in Fig. 17. It consists of two stages, the input common-source stage having drain to gate feedback to

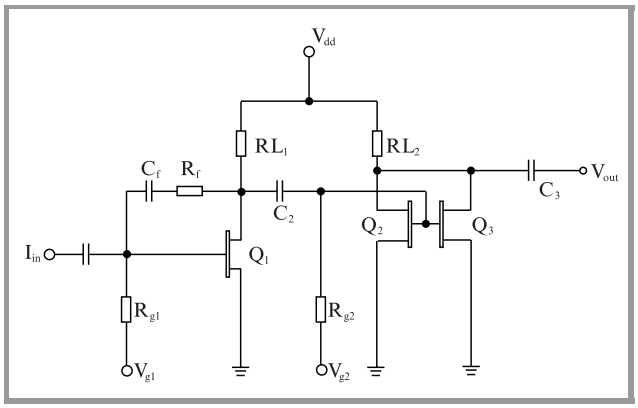


***Fig. 17.*** Two stage transimpedance amplifier using n-MODFETs sketched in Fig. 4.

transform current to voltage. The second stage amplifiers the output voltage of the first stage and uses two transistors to increase the gain. Spice simulations suggest a 3 dB Ω bandwidth of 4.84 GHz with a gain of 64.7 dB Ω for a power supply voltage of 5 V and for a feedback resistor of 1.5 kΩ, assuming ideal impedance matching. On the other hand, using a feedback resistor of 540 Ω, the maximum bandwidth measured is 1.8 GHz and the gain is 56 dB Ω. The performance shortfall is attributed in part to non-optimum oxide passivation and non-ideal impedance matching. A similar device has been used by Ostermann et al. [30] to fabricate an inverter circuit, Fig. 18. $Q_1$ is a common source amplifier which feeds on active load $Q_2$. The gate delay is 28 ps for 180 nm gate length, 100 $\mu$m gate width, and power supply voltage $V_{DD} = 2$ V.
SiGe CMOS offers for the first time the possibility of speeds to approach and match that of GaAs technology while at

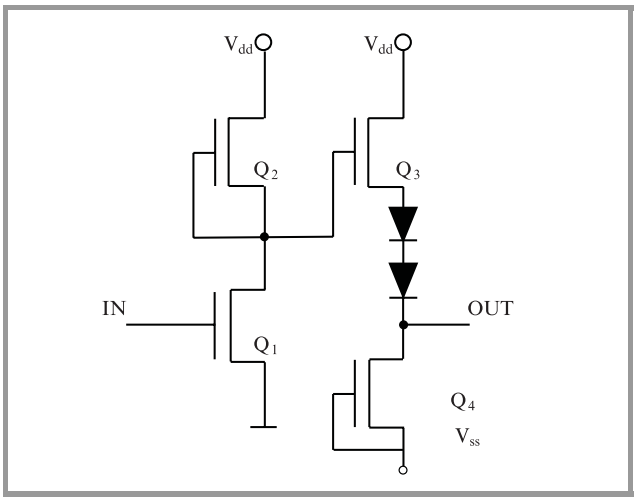


***Fig. 18.*** Inverter circuit with source follower, using n-MODFETs sketched in Fig. 4. $Q_2$ and $Q_4$ are active loads.

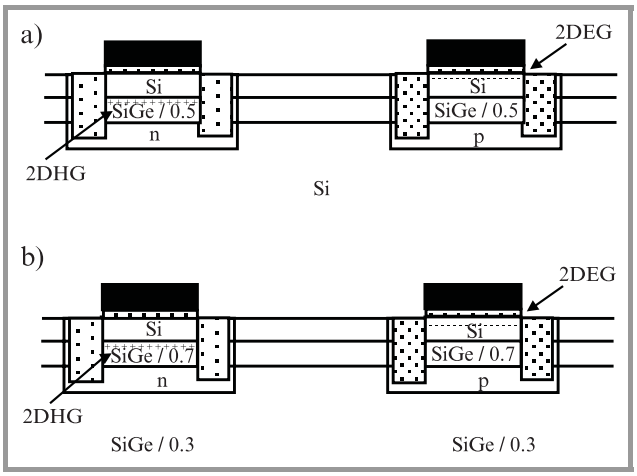


***Fig. 19.*** Si/SiGe CMOS process options: (a) giving enhanced p-channel performance, (b) giving enhanced n-channel performance and further enhancement of p-channel performance.

the same time offering p-channel and enhancement mode devices, not available in GaAs, simplifying circuit design. Figures 19a and 19b show, respectively, two process options for (a) a fully pseudomorphic CMOS technology of enhanced p-channel performance and (b) a VS one having both improved n and p-channel performance. A CNET group [11] and a Southampton/Warwick Group [32] have independently attempted the fabrication of a CMOS configuration of type (a). Whereas enhanced p-channel performance was demonstrated in the CNET device, Ge segregation and/or diffusion degraded the performance of the surface n-channel. Similarly, the Southampton p-channel showed enhanced transconductance but the n-channel device properties were poor due to unsuccessful attempts to find a low thermal budget oxide. Nevertheless, these are first attempts and the outlook is promising. As far as we are aware no work has yet been carried out on configuration (b).

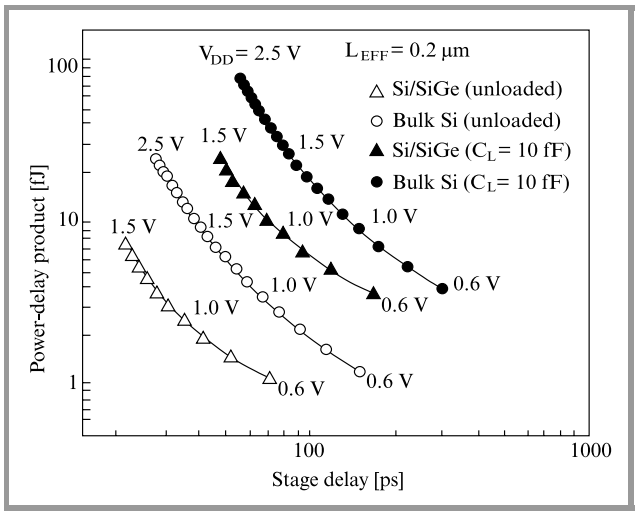


***Fig. 20.*** Simulated power delay product versus stage delay for a Si/SiGe CMOS configuration, based on strained silicon and strained SiGe alloy layers, given enhancements in both n- and p-channel current drive (*after Armstrong et al. [34]*).

Voinigescu et al. [33] have calculated the 3-stage ring oscillator delay for a fully pseudomorphic Si/SiGe 0.25 $\mu$m CMOS technology, and for a supply voltage of 2.5 V. Their calculations are based on a fully graded SiGe channel, the Ge fraction varying from 0 at the bottom to 0.5 at the top of the structure, the effective mobility [34] of which is shown in Fig. 2. They obtain a delay of 33 ps per stage compared to 50 ps for the Si CMOS circuit. The power delay products have been calculated by Armstrong et al. [35] for a VS based Si/SiGe CMOS configuration similar to that shown in Fig. 19b and for bulk Si CMOS, and are compared in Fig. 20. The authors assume channel lengths of 0.2 $\mu$m, gate oxide thicknesses of 5 nm and low field mobilities of 2500 $cm^2V^{-1}s^{-1}$ and 800 $cm^2V^{-1}s^{-1}$ for SiGe n-MOS and p-MOS. Factors of 1.23 and 2.25 increases are predicted for n-MOS and p-MOS current drive respectively. The drain current saturates at a low drain bias of 0.4 V for SiGe n-MOS and 0.8 V for SiGe p-MOS. This cuts down the power consumption by up to a factor of 3 or 4! The high carrier mobilities result in a factor of 6.4 improvement in power delay product for the unloaded case and a factor of 4.6 improvement at a delay of 55 ps for the loaded case compared to bulk Si. It is noted that the performance advantage derives largely from the increased current drive of the SiGe p-MOS channel.

The huge and wide ranging markets in wireless and optical communications offer plenty of opportunities for a SiGe FET technology. The digital wireless handset [36] shown in Fig. 21 may be used to illustrate the potential advantages of SiGe MOS technology, since it contains numerous important building blocks in mobile communications. GaAs currently predominates in the RF section containing the power amplifier (PA), driver amplifier, low noise amplifier (LNA) and transmit/receive (T/R) switch, and competes with silicon in the mixer sections. It is currently being challenged by the SiGe HBT in all these areas. A preferred solution,

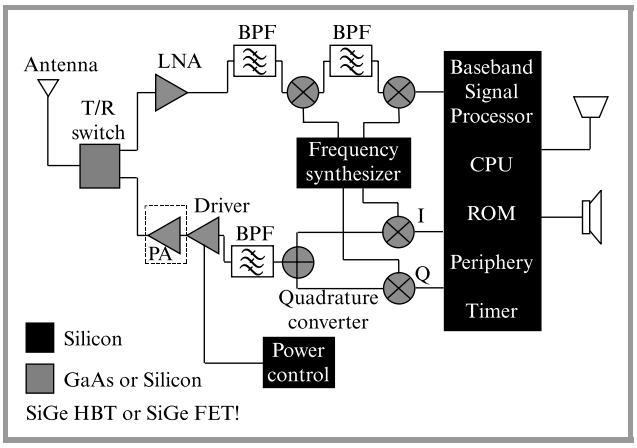


***Fig. 21.*** Building blocks of a digital handset (*after Costa [35]*). The areas where SiGe FETs could compete are shown shaded.

capable of giving higher levels of integration and lower power consumption is Si CMOS [37]. The incorporation of SiGe into CMOS may be what is needed for this to happen. As the technology matures we might expect that SiGe will bring the high $f_T$, $f_{max}$, better linearity and HF noise needed by the LNA. Switched capacitor circuits are promising candidates for band pass filters (BPF). Here the faster switching speed and low power consumption of SiGe CMOS could be of benefit. The good $1/f$ noise properties referred to in Section 3 could lead the development of low-phase noise local oscillators for the frequency synthesiser. The transmitter power amplifier places particularly onerous demands on Si CMOS. However, good progress is being made in this respect with ordinary Si. For example, an 0.4 $\mu$m Si n-MOS 2 GHz amplifier has been demonstrated with 1 W output power, 50% PAE at 3.6 V, with satisfactory linearity and a breakdown voltage of 15 V [38]. SiGe should, in principle, be able to significantly improve on these figures.

## 5. Conclusions

The current performance indicators for Si/Ge are such that it offers serious prospects of making significant inroads into, or even displacing, the more mature bulk silicon technology. An example of an early application would be in mobile telephony. Much work is still needed on design, growth and processing before this can happen.

## Acknowledgements

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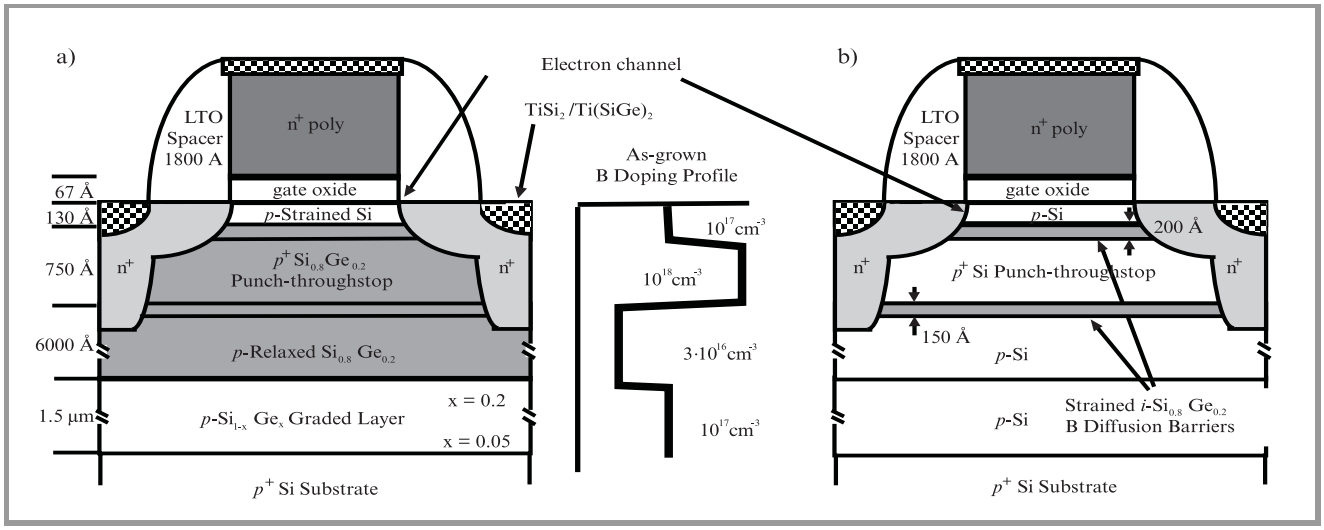


***Fig. 6.*** Showing (a) strained Si n-MOSFET and (b) unstrained Si control device structures. Boron profile control is aided by $Si_{0.8}Ge_{0.2}$ diffusion barriers in each case (*after Rim et al. [8]*).

*Invited paper*

# Reliability of deep submicron MOSFETs

Francis Balestra

**Abstract — In this work, a review of the reliability of n- and p-channel Si and SOI MOSFETs as a function of gate length and temperature is given. The main hot carrier effects and degradations are compared for bulk and SOI devices in a wide range of gate length, down to deep submicron. The worst case aging, device lifetime and maximum drain bias that can be applied are addressed. The physical mechanisms and the emergence of new phenomena at the origin of the degradation are studied for advanced MOS transistors. The impact of the substrate bias is also outlined.**

***Keywords — bulk MOSFETs, SOI devices, deep submicron transistors, reliability.***

## 1. Introduction

It is well known that hot-carrier-induced device degradation (creation of interface states and/or positive and negative trapped charges by electron or hole injection) can limit the long-term reliability of deep submicron MOSFETs (reduction of transconductance and drain current, shift of the threshold voltage). The impact ionization phenomenon is one of the main hot carrier effects [$1 \div 6$]. We can distinguish two stress regimes, which depend on the electron energy. The first one corresponds to the primary impact ionization in maximal substrate current condition ($V_g \cong V_{d/2}$). The second stress regime corresponds to the secondary impact ionization in maximal gate current condition ($V_g \cong V_d$). The longitudinal electric field responsible for the primary impact ionization produces hot carriers with energy around 1.5 eV [3]. Monte Carlo simulations have shown that the secondary ionization generates hot carriers with energy values higher than $3 \div 3.5$ eV after a secondary heating in the drain/substrate junction. These energies correspond to the interface state threshold energy [4, 5]. The interface state creation is one of the major causes of device degradation. Nevertheless, several issues are still not clear up to now:

1. What is the worst case aging condition (maximum substrate or gate currents) as a function of gate length and temperature?
2. Which physical mechanisms are at the origin of the main degradation for advanced devices?
3. Is there some differences for the aging of bulk Si and SOI MOSFETs?
4. What are the lifetime and maximum drain bias which can be applied as a function of device architecture?

In this work, the hot carrier phenomena and degradation in various regimes of n- and p-channel bulk silicon and silicon-on-insulator MOSFETs are studied in a wide range of gate length down to deep submicron as a function of temperature.

## 2. Results and discussion

### *2.1. Bulk Si MOSFETs*

Figure 1 shows the secondary impact ionization mechanisms. The first ionization leads to electron/hole pairs. The electrons flows towards the drain for a n-channel MOSFET and the holes are heated in the drain substrate junction where high electric fields exist for advanced MOSFETs due to high substrate doping. These holes gain high energies and can induce a second impact ionization leading to electrons/holes pairs. The holes constitute the substrate current and the electrons can be injected into the gate in particular for deep submicron devices realized with ultra-thin gate oxides leading to high transverse electric field. These electrons are at the origin of the gate current or can be trapped in this oxide.

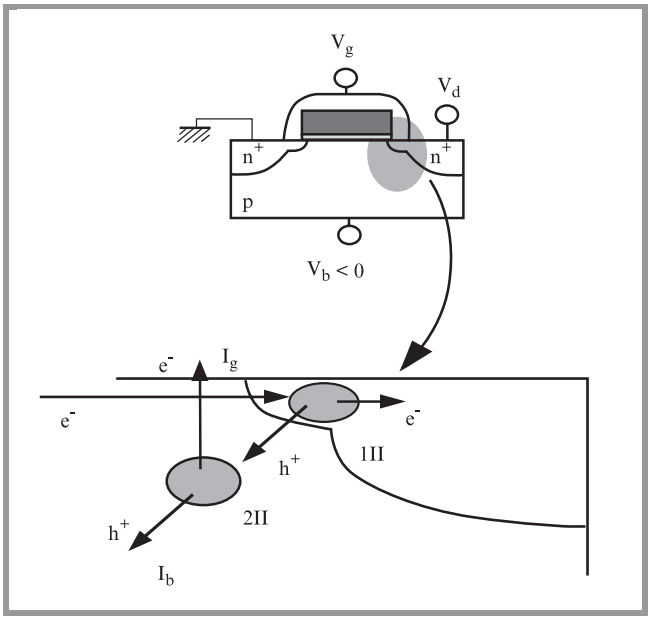


**Fig. 1.** Secondary impact ionization mechanisms.

Figure 2 exemplifies the gate current as a function of the substrate bias for a $0.45\,\mu$m MOSFET of a $0.1\,\mu$m technology with a 3.5 nm gate oxide [7]. The substrate bias is used in this experiment in order to enhance the electric field at the drain/substrate junction leading to a higher secondary impact ionization. The gate current induced by

this secondary heating obtained with a model based on the lucky electron concept is also shown in this figure. The good agreement observed between theory and experiment confirms the origin of this gate current. Therefore these additional hot carrier effects will play a major role for determining the worst case degradation and the reliability of advanced MOS transistors.

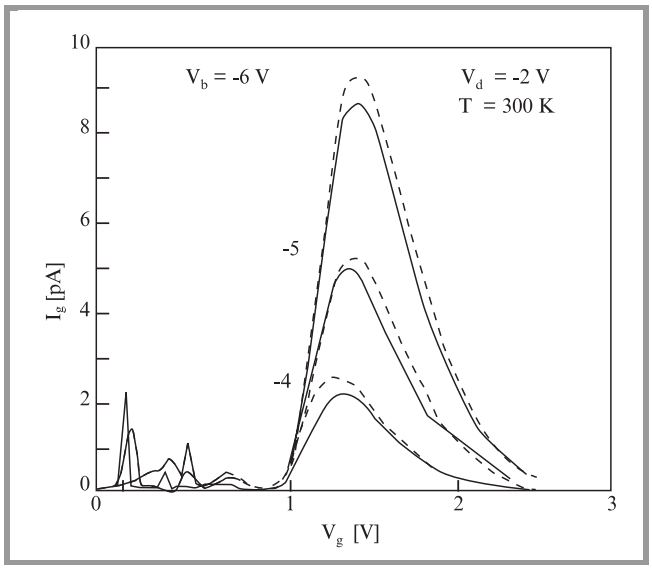


**Fig. 2.** Comparison between model and experimental data for the gate current of advanced bulk Si devices (0.45 $\mu$m N-MOSFET of a 0.1 $\mu$m technology with a 3.5 nm gate oxide) taking into account the secondary impact ionization.

Figure 3 is a plot of the impact of temperature on the gate current characteristics. $I_g$ is substantially increased at low temperature even for a low drain voltage (2 V). The model taking into account the secondary impact ionization is also in good agreement with the experimental data.

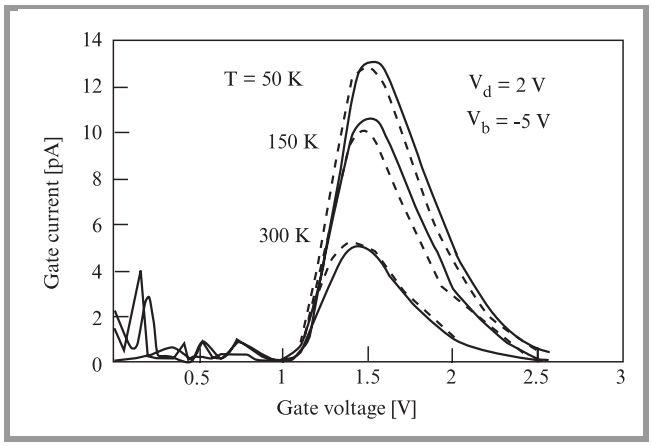


**Fig. 3.** Impact of temperature (experiment and modeling) on the $I_g\,(V_g)$ characteristics for a 0.45 $\mu$m bulk N-MOSFET of a 0.1 $\mu$m technology with a 3.5 nm gate oxide.

The number of emitted photons due to hot electrons as a function of energy is plotted in Fig. 4. The impact of the substrate bias on the light emission is also shown. For small energies ($1 \div 1.5$ eV) the substrate voltage has a very small impact. However, for high energies ($2 \div 3$ eV), the number of emitted photons substantially increases at high $V_b$ due to the secondary heating at the drain/substrate junction. These hot carriers can lead to significant device degradation.

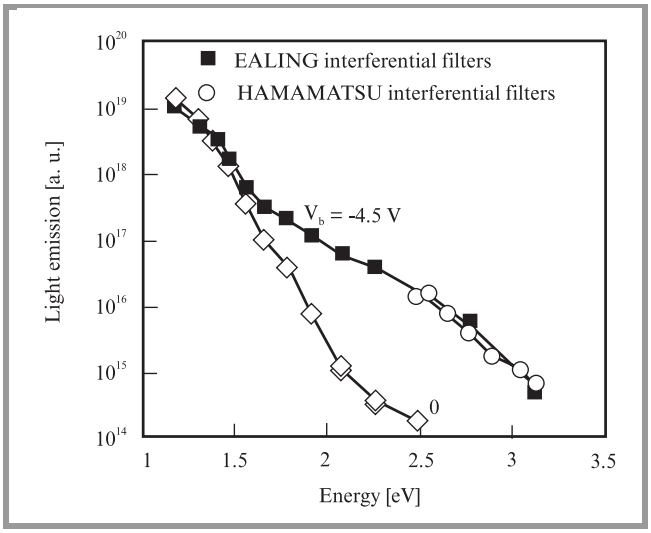


**Fig. 4.** Impact of the substrate bias on the light emission for deep submicron bulk MOSFETs.

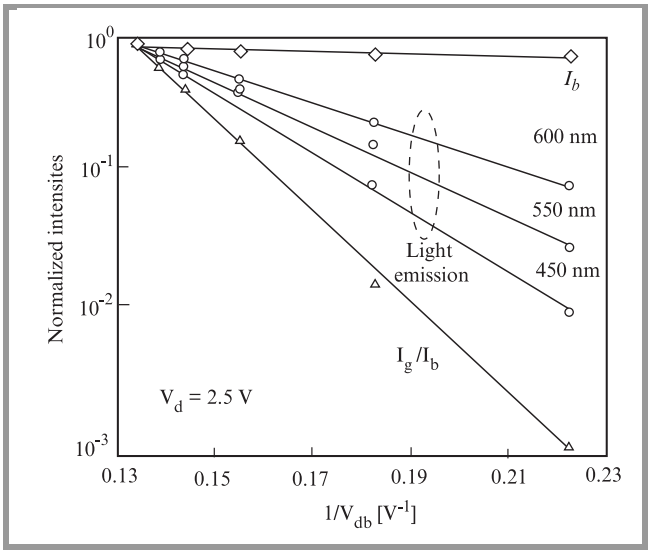


**Fig. 5.** Correlation between the normalized gate and substrate currents and the wavelength of emitted photons for bulk silicon n-channel MOSFETs.

Figure 5 presents the correlation between the light emission and the normalized gate and substrate currents. For long wavelengths, the variation of the light emission is similar to that of the substrate current (first heating), and for small wavelengths it is correlated with the gate current (second heating).

The impact of both the channel length and temperature on the worst case aging is exemplified in Fig. 6 [8]. For long devices, the worst case corresponds to the maximum substrate current ($V_g \cong V_{d/2}$) except for very low temperatures. However, for deep submicron devices (0.1 $\mu$m range) the limit between the two worst case regimes ($V_g = V_{d/2}$ or $V_d$) is observed in the room temperature range. Therefore, the maximum gate current ($V_g \cong V_d$) could become the worst case degradation even at 300 K. Furthermore, in the traditional operating range (between $-50$°C and 100°C) the worst case can shift from a regime to another one for advanced MOSFETs.

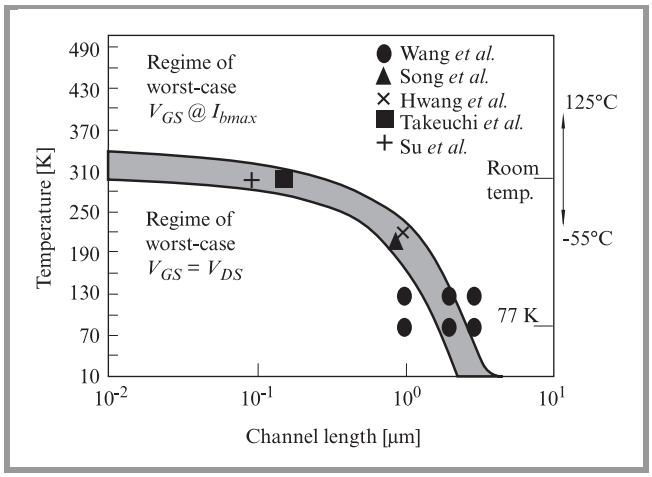


**Fig. 6.** Impact of channel length and temperature on the worst case degradation (bulk NMOS).

The influence of the substrate voltage for various temperatures is exemplified in Fig. 7. The significant impact of the substrate bias on the transconductance degradation both at 300 and 77 K demonstrates that the secondary heating plays a major role in the reliability of the devices. The maximum drain bias which can be applied in order to obtain a ten years lifetime (criterion: 10% transconductance degradation under static stress) is analyzed for 0.2 $\mu$m MOS transistors. The worst case aging leading to the minimum $V_{d\max}$ is obtained for a stress in $I_{g\max}$ condition both at room and liquid nitrogen temperatures (Fig. 8). In addition, a stronger degradation is always observed at 77 K as compared to 300 K, even in the case of $I_{b\max}$ stress (Fig. 8). In this regime, a smaller substrate current and impact ionization rate have been previously shown, but the enhancement of carrier trapping and the larger influence of a given degradation on the electrical properties at low temperature could explain this special behavior.

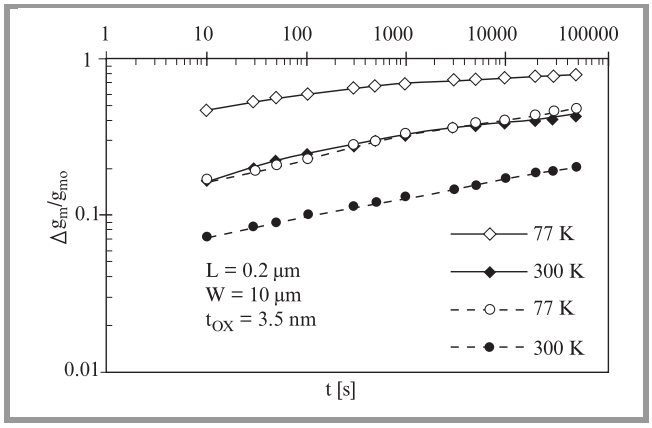


**Fig. 7.** Impact of substrate bias for bulk N-MOSFET devices on transconductance degradation for $I_{g\max}$ stress ($V_b = -3$ V full lines, $V_b = 0$ V dashed lines).

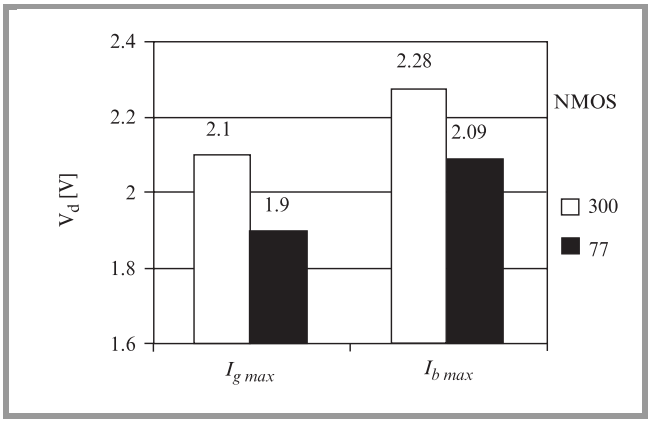


**Fig. 8.** Maximal drain voltage in order to obtain 10% transconductance degradation after 10 years for bulk N-MOSFET (W/L = 10/0.2, $t_{ox} = 3.5$ nm); static stress.

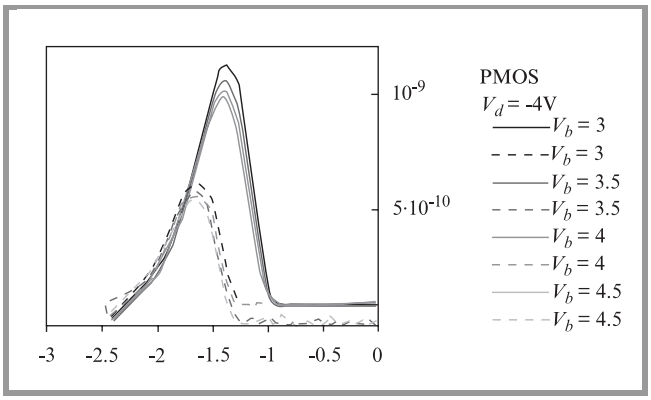


**Fig. 9.** Typical $I_g(V_g)$ characteristics obtained at $V_d = -4$ V for different substrate voltages at 300 K (full lines) and 77 K (dashed lines) (bulk PMOS, W/L = 10/0.2, $t_{ox} = 3.5$ nm).

Therefore, the impact of the secondary hot carrier effects is clearly demonstrated at room and low temperature for advanced n-channel MOSFETs.

Figure 9 exemplifies the typical gate current characteristics for a 0.2 $\mu$m p-channel bulk Si MOSFET. An electron current is found whatever the substrate and drain biases are. The substrate voltage has only a very low influence on the gate current level (small reduction with increasing the substrate bias). These results show that the influence

of the secondary impact ionization is negligible for PMOS devices. Furthermore, contrary to the case of n-channel MOSFETs, $I_g$ is reduced for lower temperatures (Fig. 9).

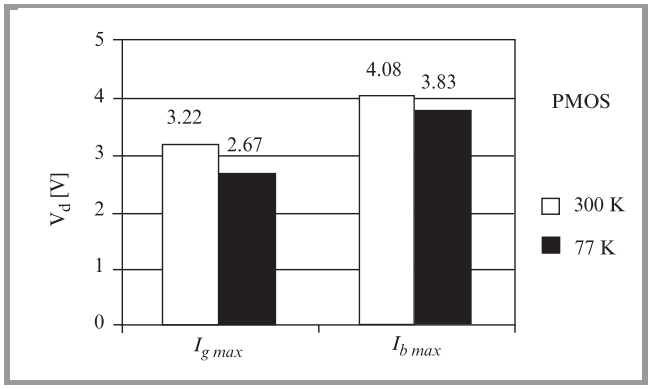


**Fig. 10.** Maximal drain voltage in order to obtain 10% transconductance degradation after ten years (static stress) (bulk PMOS, W/L = 10/0.2, $t_{ox} = 3.5$ nm).

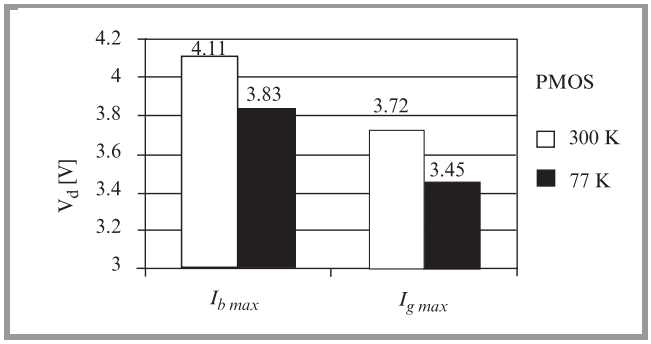


**Fig. 11.** Maximal drain voltage in order to obtain 100 mV threshold voltage degradation after ten years (static stress) (bulk PMOS, W/L = 10/0.2, $t_{ox} = 3.5$ nm).

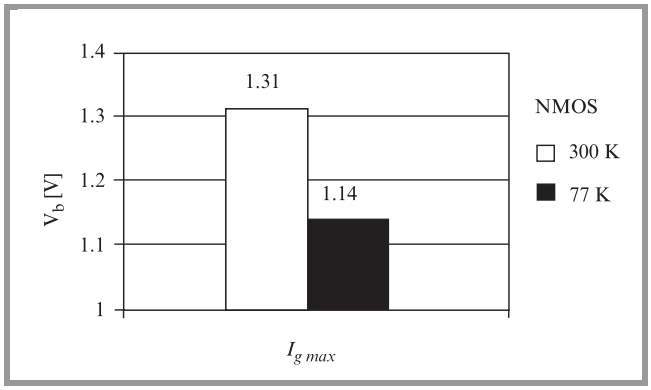


**Fig. 12.** Maximal substrate voltage in order to obtain 10% transconductance degradation after ten years (static stress) (bulk NMOS, W/L = 10/0.2, $t_{ox} = 3.5$ nm, $V_d = 2$ V).

The maximum drain bias which can be applied in order to obtain a ten years lifetime (criterion: 10% transconductance degradation under static stress) is shown in Fig. 10. The worst case aging is obtained for a stress performed at $V_g = V_d$ (noted „$I_{g\max}$"). However, it is worth noting that the maximum gate current is reached for a gate voltage substantially lower than the drain bias in the case of P-MOSFETs (see Fig. 9). The drain voltage $V_{d\max}$ for a 10 years lifetime is also reduced at 77 K as compared to room temperature operation, even if the substrate and gate currents are smaller at liquid nitrogen temperature. Therefore, for deep submicron devices, a stress at $V_g = V_d$ for a 77 K operation is always the worst case for PMOS and NMOS. A similar trend is observed for the threshold voltage degradation (Fig. 11).

The maximum substrate bias, which can be applied in order to obtain a 10 years lifetime for a 0.2 $\mu$m bulk Si N-MOSFET, is illustrated in Fig. 12. A nominal bias (2 V) is applied for this 0.2 $\mu$m technology. $V_{b\max}$ is around 1.3 V at 300 K and 1.1 V at 77 K, which shows that the applied substrate bias could become a limitation in some applications.

### *2.2. SOI MOSFETs*

The SOI technology is well known for its advantages as compared to bulk devices, in particular in the field of low voltage/low power and high frequency applications [9, 10]. However, SOI MOSFETs can suffer from possible degradation of the front and the buried silicon/oxide interfaces. Furthermore, another hot carrier regime associated with the parasitic bipolar transistor triggered at high $V_d$ can be harmful for deep submicron SOI devices. Therefore, it is necessary to perform a thorough evaluation of these effects as function of the SOI transistor architecture.

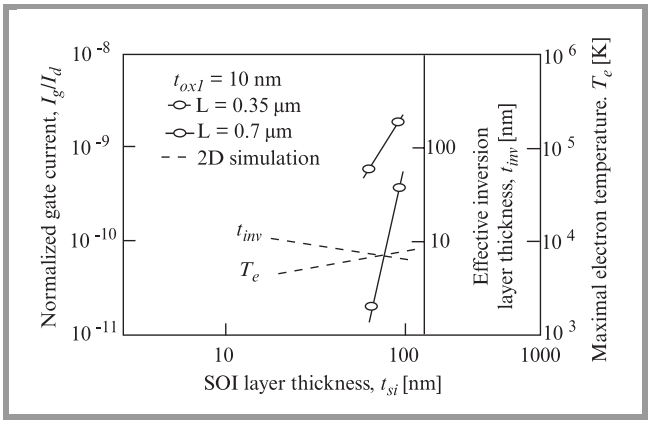


**Fig. 13.** Comparison between the variations of the normalized gate current, the inversion layer thickness and the electron temperature versus Si film thickness for fully depleted SOI MOSFETs.

In Fig. 13 the dependence of the normalized gate current versus the silicon film thickness is plotted [11]. The gate current is reduced for thinner films whatever the gate length is. This interesting behavior is partially attributed to the increase of the inversion layer thickness in fully depleted SOI films which is induced by the reduction of the transverse electric field. This phenomenon leads to a reduction of carrier temperature. However, another possible effect in order

to explain the decrease of hot carrier effects is the lowering of the secondary impact ionization. Indeed, in thin film SOI, the area of the drain/substrate junction decreases as compared to thick Si layers or bulk MOSFETs, and therefore a reduction of the number of high energy carrier is obtained. Moreover, the reduction of the transverse electric field also leads to a smaller injection probability into the gate.

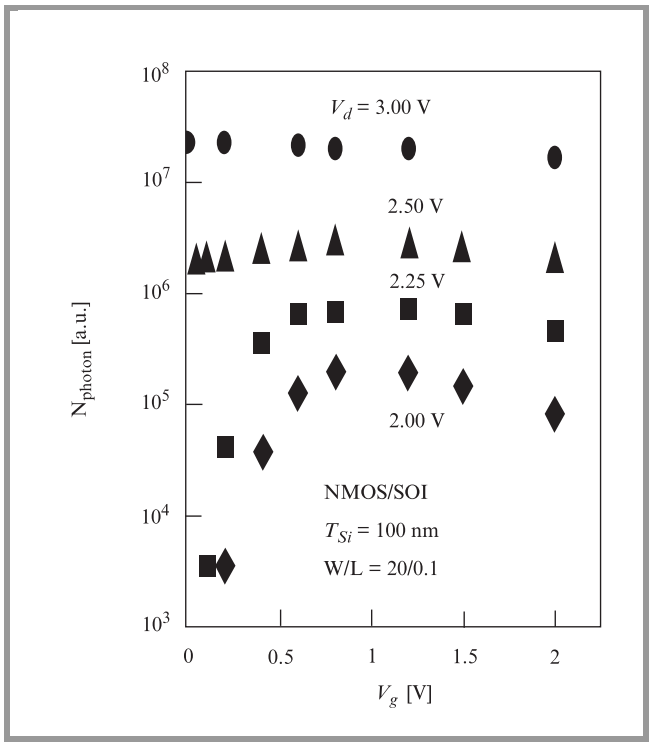


**Fig. 14.** Number of emitted photons in 0.1 $\mu$m n-channel SOI MOSFET versus gate and drain biases.

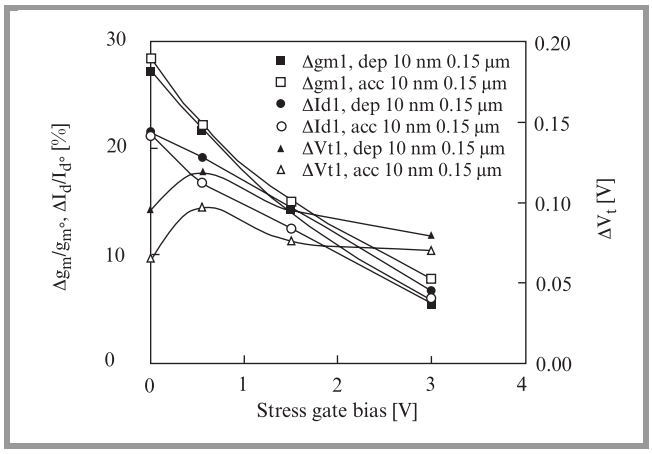


**Fig. 15.** Device parameter degradation as a function of gate bias for 0.15 $\mu$m n-channel SOI MOSFETs realized on an ultra-thin (10 nm) Si film thickness measured with accumulated or depleted opposite interface.

However, another typical SOI mechanism associated with the floating body has to be taken into account for long term device reliability. Figure 14 shows the number of emitted photons for a 0.1 $\mu$m SOI MOSFET versus gate and drain biases [12]. For small gate and high drain voltages, a large increase of the photon number is observed due to the parasitic bipolar transistor (PBT) action inducing high energy carriers. Contrary to the case of bulk Si MOSFETs, as illustrated in Fig. 15 for a 0.15 $\mu$m fully depleted SOI device fabricated on a 10 nm Si layer thickness, the worst case aging is obtained for small gate biases $(0 \div V_t)$ due to this PBT action [13].

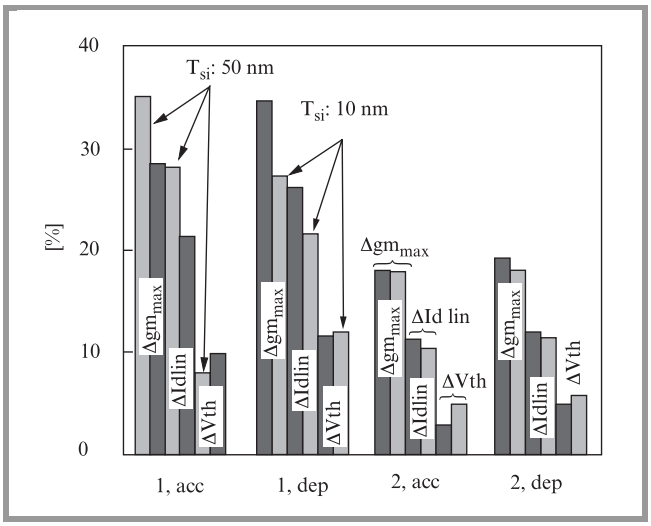


**Fig. 16.** Device degradation $(I_d, gm, V_t)$ at the front (1) and back (2) interfaces as a function of Si layer thickness (10 and 50 nm) measured with accumulated or depleted opposite interface for n-channel fully depleted SOI MOSFETs.

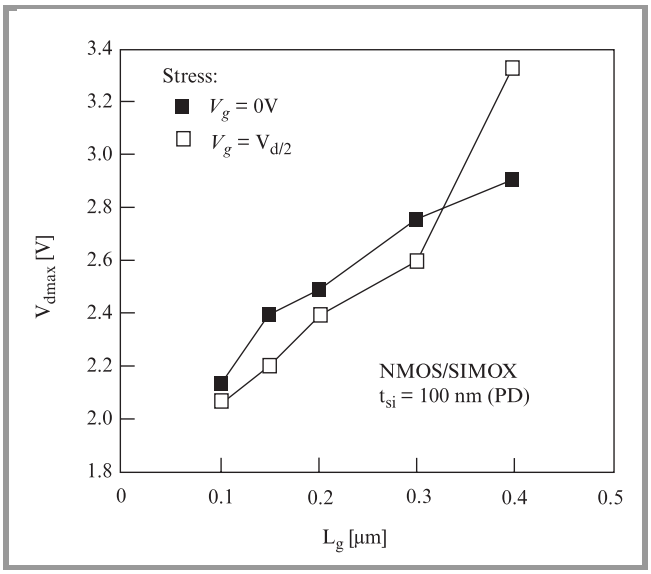


**Fig. 17.** Maximum drain bias that can be applied in order to obtain 10 years device lifetime (static stress) versus gate length for partially depleted (100 nm Si film thickness) n-channel SOI MOSFETs.

Figure 16 presents the impact of the Si film thickness on fully depleted SOI device degradation in the PBT regime [13]. It is clear that a reduction of the transconductance and drain current degradation is obtained with reducing the SOI layer thickness. In particular, a significant decrease of the front interface aging is observed, while similar degradations are observed for the back interface due to larger interface coupling in ultra-thin films.
The reliability of partially depleted SOI MOSFETs is exemplified in Fig. 17 [12]. The maximum drain bias which can be applied in order to obtain a 10 years lifetime is shown. For this device architecture, the worst case aging with a minimum $V_{d\max}$ is observed in the maximum substrate current condition $(V_g = V_{d/2})$ in the deep submicron range. Therefore, contrary to the case of bulk devices, the worst case aging is obtained for low gate voltages $(0 \div V_{d/2})$ in n-channel SOI MOSFETs whatever the device architecture is.

## 3. Conclusion

A review of the reliability of n- and p-channel bulk Si and SOI MOSFETs as a function of gate length and temperature has been given. The worst case aging, device lifetime and maximum drain bias that can be applied have been addressed. The impact of the substrate bias has also been outlined. The worst case degradation has been found at $V_g = V_d$ (which corresponds to the maximum gate current condition for n-channel) for deep submicron bulk Si MOSFETs whatever the temperature is and for long channel transistors at low temperature. The substantial influence of the secondary impact ionization on the degradation has been clearly demonstrated for very short channel N-MOSFETs. The interest of using ultra-thin film SOI MOS transistors for reducing the secondary impact ionization and device aging has also been pointed out. Contrary to the case of bulk MOSFETs, the worst case aging has been found for small gate biases $(0 \div V_{d/2})$ in all the n-channel SOI devices.

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*Invited paper*

# High-temperature instability processes in SOI structures and MOSFETs

Alexei N. Nazarov, V. I. Kilchytska, Ja. N. Vovk, and J. P. Colinge

**Abstract — The paper reviews the problems related to BOX high-temperature instability in SOI structures and MOSFETs. The methods of bias-temperature research applied to SOI structures and SOI MOSFETs are analysed and the results of combined electrical studies of ZMR, and SIMOX SOI structures are presented. The studies are focused mainly on electrical discharging processes in the BOX at high temperature and its link with new instability phenomena such as high-temperature kink effects in SOI MOSFETs.**

***Keywords — SOI, MOSFET, high-temperature instability, ZMR, SIMOX.***

## 1. Introduction

Devices fabricated on silicon-on-insulator (SOI) structures are very promising for high-temperature microelectronics [1]. Consequently, the high-temperature stability of SOI structures is the necessary condition for proper device operation. From this point of view, the main weakness of SOI structures is thick buried oxide (BOX), which can effectively accumulate a positive and a negative charge during the application of sufficiently low electric fields to SOI structures [2, 3].

Thus, the paper is devoted to review high-temperature instability phenomena in SOI structures and devices especially with respect to bias-temperature (BT) processes in the BOX.

## 2. Methods for electrical characterization of high-temperature instability processes

### *2.1. Capacitance-voltage method for SOI structures*

The most widely used method to study the BT instability is the analysis of capacitance-voltage (C-V) curves. In this method measurements are performed at room temperature before and after application of the bias to the gate of SOI structure at high temperature. For SOI structures the C-V method is very useful, since it permits the potentials at BOX/substrate and at BOX/film interfaces (Fig. 1a) and, consequently, the total net charge, $Q_{tn}$, in the BOX and its centroid, $X_0$, to be determined. As it was proposed in [4, 5]

$$Q_{tn} = Q_f + Q_{sub} = \frac{C_d\left(V_{FB}^f - V_{FB}^{sub}\right)}{qS}, \qquad (1)$$

$$X_0 = \frac{\int_0^d \rho(x)x\,dx}{\int_0^d \rho(x)x\,dx} = \frac{|V_{FB}^f|\,d}{V_{FB}^f - V_{FB}^{sub}}, \qquad (2)$$

where $V_{FB}^f$, $V_{FB}^{sub}$ are flat-band voltages related to the film/BOX and the substrate/BOX interfaces, respectively, $\rho(x)$ is the charge distribution in the BOX, $d$ is the BOX thickness, $C_d$ is the buried insulator capacitance. The centroid is determined with respect to the BOX/substrate interface (Fig. 1b).

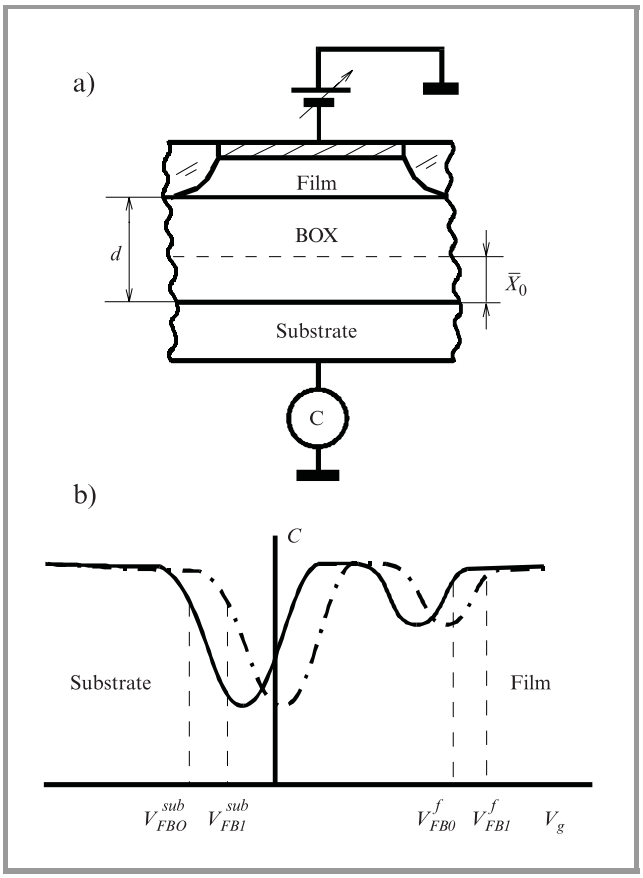


***Fig. 1.*** A schematic diagram of a SOI capacitor (a) and low-frequency C-V characteristics before (bold line) and after (dotted line) BT stress (b).

The amount of the mobile charge related to the BOX/film interface, $\Delta Q_m^f$, and to the BOX/substrate interface, $\Delta Q_m^{sub}$, after BT stress can be calculated as

$$\Delta Q_m^f = \frac{C_d\left(V_{FB1}^f - V_{FB0}^f\right)}{qS} = \frac{C_d \Delta V_{FB}^f}{qS} \tag{3}$$

and

$$\Delta Q_m^{sub} = \frac{C_d \Delta V_{FB}^{sub}}{qS}\,, \tag{4}$$

where $V_{FB1}$, $V_{FB0}$ are flat-band voltages after and before BT stress, respectively (see Fig. 1a). Thus, the change of the charge in the BOX is

$$\Delta Q_{tr} = \Delta Q_m^f - \Delta Q_m^{sub}\,. \tag{5}$$

If $\Delta Q_{tr} = 0$, we can consider the BOX/semiconductor interfaces as electrically blocking ones, if $\Delta Q_{tr} \neq 0$, interfaces are electrically unblocking.

### *2.2. Thermally stimulated polarization/depolarization currents*

Thermally stimulated polarization/depolarization (TSP/TSD) current method is used to investigate the charge transfer processes in a dielectric during linear heating of the structure, holding a fixed voltage across the capacitors and measuring the resulting current (Fig. 2).

It has been shown that charge moving in the outer circuit during the polarization or depolarization processes, $Q_{TSP/TSD}$, is equal to the mirror charge at the blocking electrode [6]. Therefore:

$$Q_{TSP/TSD} = \frac{1}{\beta S}\int_{T_0}^{T} I(T)\,dT = \Delta Q_m^f\,, \tag{6}$$

if the BOX/film interface is blocking, or

$$Q_{TSP/TSD} = \Delta Q_m^{sub} \tag{7}$$

if the BOX/substrate interface is blocking, where $\beta$ is the heating rate.

Thus, the comparison of C-V with TSP/TSD data allows to identify the electrically blocking interfaces and to determine the degree of blocking.

In addition, the TSP/TSD method gives the possibility of determination the activation energies of the polarization/depolarization processes and the frequency factor or capture cross section for traps involved in the processes (see, for instance [7]). In the case of energy distributed traps the fractional thermally cleaning method can be used in order to calculate the trap parameters [8].

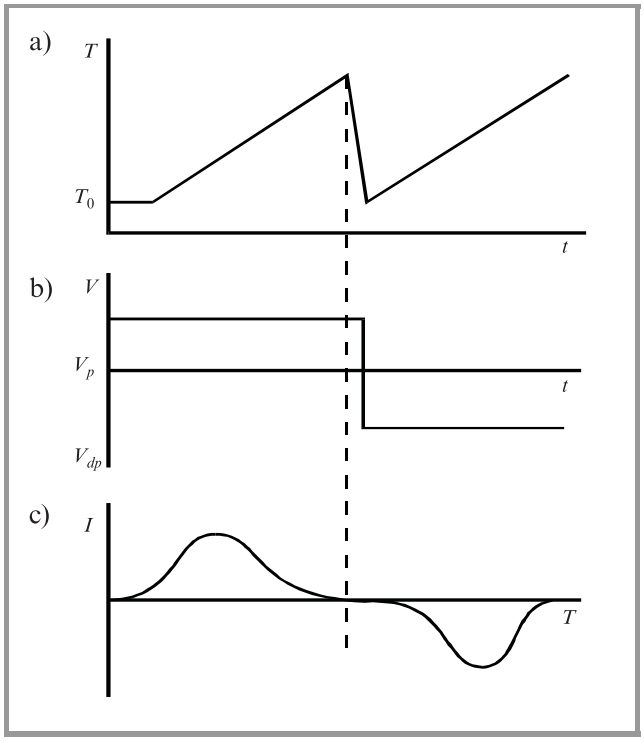


***Fig. 2.*** Schematic time diagrams of temperature (a) and applied voltage (b), and TSP/TSD current (c).

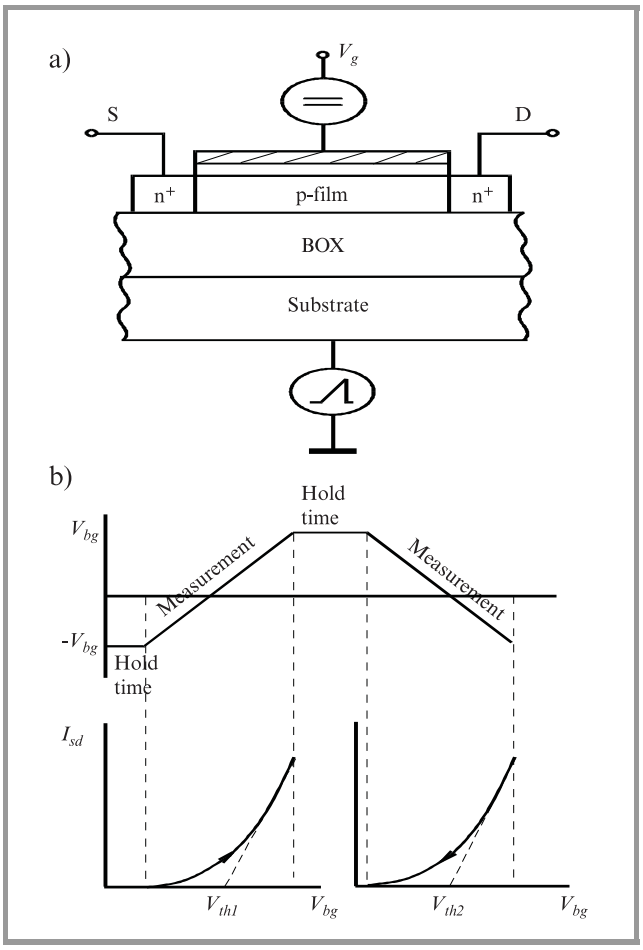


***Fig. 3.*** A schematic diagram of a SOI MOSFET (a) and the applied voltage at the back-gate (b) for BT instability measurements using the drain-gate characteristic technique.

### *2.3. Source-drain current – gate voltage characteristics of MOSFETs*

Source-drain current $I_{sd}$ – gate voltage $V_g$, characteristics at high temperature enable the polarization parameters to be determined and the operation stability of the devices to be analysed. Measurement of the source-drain current, $I_{sd}$, in the back channel SOI MOSFET at high temperature, after holding the back-gate voltage positive or negative (Fig. 3), permits the change in the charge in the BOX layer relative to the BOX/film interface to be determined:

$$\Delta Q_m^f = C_d \frac{V_{th1} - V_{th2}}{qS} = \frac{C_d \Delta V_{th}}{qS} , \qquad (8)$$

where $V_{th1}$, $V_{th2}$ are back-channel threshold voltages after negative and positive applied voltage to the back-gate, respectively.
Investigation of the threshold voltage shift as a function of temperature and hold time permits all main parameters of high temperature instability processes to be calculated.

### *2.4. Source-drain current relaxation*

If at high temperature the polarity of the back-gate voltage is reversed and, as result, relaxation of the source-drain current occurs it is possible to determine the relaxation time of the processes, that links with the relaxation time of the charge changing in the BOX. This phenomenon is depicted schematically in Fig. 4. Indeed, as it was shown in [9] in the linear regime of the inversion mode (IM) SOI n-MOSFET operation, the source-drain current can be given by

$$I_{sd}(t,T) = \left(\frac{W}{L}\right) \mu_e C_d \left[V_{bg} - V_{thb}^* + Q_{BOX}(t,T)/C_d\right] V_{sd} , \qquad (9)$$

where $W$, $L$ are the width and the length of the channel, $\mu_e$ is the electron mobility in the inversion channel, $V_{bg}$ is the back-gate voltage, $V_{thb}^*$ is constant with weak temperature dependence, $Q_{BOX}$ is the total buried oxide charge, $V_{sd}$ is source-drain voltage. That is, the source-drain current relaxation is directly linked with buried oxide charge changing.
If the BOX charge depends on the time and temperature as:

$$Q_{BOX}(t,T) = Q_{BOX}(t=0) \exp\left[-\frac{t}{\tau(T)}\right] \qquad (10)$$

the relaxation time, $\tau(T)$, can be calculated from slope angle tangent of the following dependence:

$$\ln \frac{I_{sd}(t) - I_{sd}(\infty)}{I_{sd}(0) - I_{sd}(\infty)} = -\frac{t}{\tau} , \qquad (11)$$

where $I_{sd}(0)$ and $I_{sd}(\infty)$ are the source-drain current at first and at final moment, respectively.
The measurement of source-drain current relaxation at different temperature allows the activation energy of the instability processes to be determined.
Thus, a combination of the C-V and the TSP/TSD current methods with $I_{sd}$-$V_{bg}$ characteristics of MOSFETs fabricated on the same SOI wafer opens a wide range of possibilities for the study of high-temperature instability processes in the BOX.

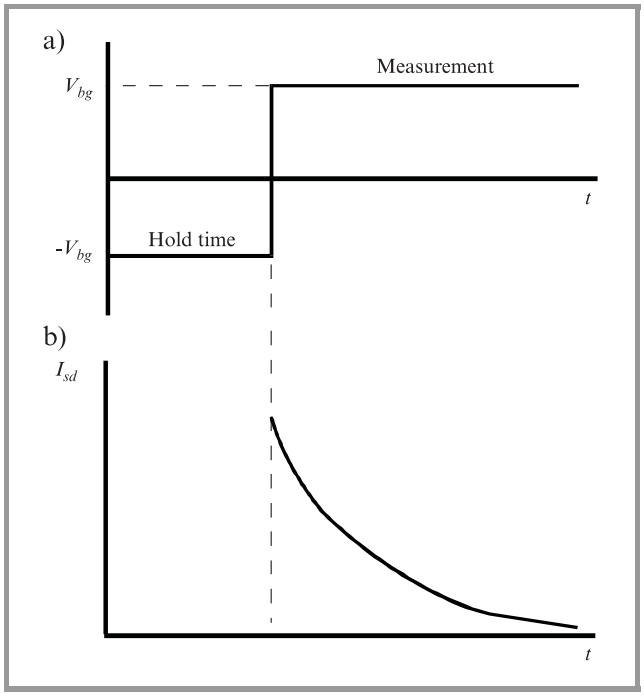


***Fig. 4.*** A schematic diagram for (a) back-gate voltage switching and (b) measurement of the relaxation current.

## 3. High-temperature instability in buried oxide of SOI structures

### *3.1. Structure fabricated by zone-melting recrystallization technique*

The SOI structures used in this study have been fabricated by the laser zone-melting recrystallization (LZMR) technique [10]. A linear melted zone was formed by a high-power CW YAG:Nd laser. A circular laser beam was transformed into a linear spot with thickness of 0.1 mm using special cylindrical lenses. In order to provide a low thermal gradient regime the wafer was heated up to 1300°C from the back side by a set of halogen lamps. Recrystallized structure was composed of a 400 nm thick poly-Si film deposited on silicon wafer thermally oxidized at high pressure ($d_{BOX} = 360$ nm) and covered by a $SiO_2$ cap layer to prevent agglomeration of the molten zone. SOI capacitors (Al-Si-$SiO_2$-Si-Al) were fabricated by LOCOS technique after recrystallization of polysilicon film.

Measurements of the C-V characteristics of LZMR SOI capacitors before and after TSP and TSD processes up to 400°C has led to the conclusion that the BOX/semiconductor interfaces in this material are almost blocking (Table 1) [11]. Bias application to the SOI structure at high temperature leads to charge movement from one interface to the other. During this movement only 10% of the charge is lost. Comparison of the total net charge in the BOX, obtained by C-V method, with moving charge in the BOX, obtained by TSP/TSD current method, helps us to conclude that almost all of the positive charge, which is trapped in the BOX, participated in the observed movement of charge.

Table 1
Total, $Q_{tn}$ and mobile charges, $Q_{TSP}$ and $Q_{TSD}$, and charge centroid in buried $SiO_2$ in ZMR SOI structures

| $Q_{tn}$ [cm$^{-2}$] (C-V) | | | $\overline{X}_0$ [Å] (C-V) | | | $Q_{TSP}$ | $Q_{TSD}$ |
|---|---|---|---|---|---|---|---|
| initial | after TSP | after TSD | initial | after TSP | after TSD | [cm$^{-2}$] | [cm$^{-2}$] |
| $1 \cdot 10^{12}$ | $8.3 \cdot 10^{11}$ | $9.4 \cdot 10^{11}$ | 1070 | 1900 | 380 | $5 \cdot 10^{11}$ | $7 \cdot 10^{11}$ |

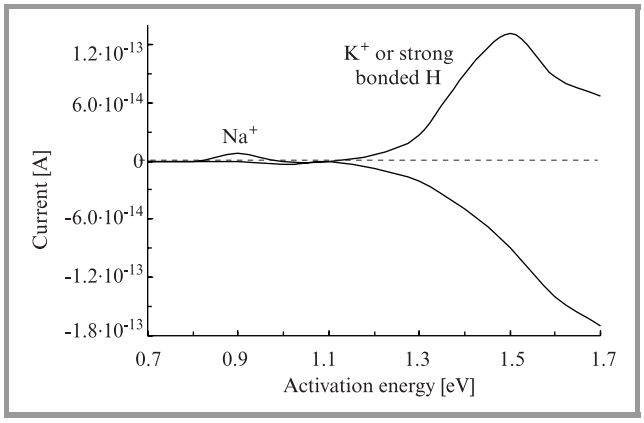


*Fig. 5.* TSP/TSD current spectra measured in ZMR mesa structures ($\beta = 0.3$°C/s).

Investigation of thermal polarization/depolarization processes (Fig. 5) [11] makes it possible to suggest that a small low-temperature current peak (located in temperature range from 50 to 100°C) with activation energy ranging from 0.75 to 0.9 eV can be related to $Na^+$ ions whilst the high-temperature current peak, located in the temperature range from 200 to 400°C with the activation energy from 1.2 to 1.7 eV is due to the movement of $K^+$ ions or to strongly bonded hydrogen.

### *3.2. SOI structures fabricated by single implanted SIMOX technique*

The SOI structure used in this study has been fabricated by the standard single implanted SIMOX technique. The implanted dose was $1.8 \cdot 10^{18}$ $O^+$/cm$^2$, the energy of implantation was 200 keV, and the temperature of implantation was 600°C. Post-implantation annealing was performed at 1320°C in Ar + 2% $O_2$ for 6 hours. After wafer processing the thickness of the BOX was 360 nm.

Investigation of the high-temperature stability of the charge in the BOX layer in SIMOX SOI structures using C-V and TSP/TSD current methods has shown [12] considerable distinction of this material from LZMR SOI one.

It should be noted that at first measurement of TSP and TSD processes there is a significant difference between the values of the polarization and depolarization current in SIMOX samples which is greater than a factor of 5 (Fig. 6). Next, the current peaks are completely asymmetric, from which it is concluded that different processes are involved during polarization and depolarization. In addition, after thermal polarization when a negative voltage is applied to the substrate a positive charge buildup in the BOX is observed; whilst a positive voltage applied to the substrate leads to negative charge accumulation, which compensates the positive charge in the BOX. In each case a considerable variation in the charge close to the BOX/substrate interface is observed whilst a very small charge change occurs near the BOX/silicon film interface (Table 2).

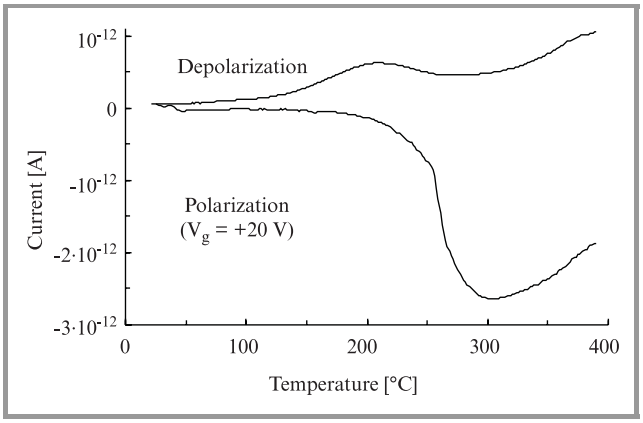


*Fig. 6.* The TSP/TSD current spectra measured in SIMOX mesa structures.

The important point is similar changing of total charge in the BOX obtained from C-V ($\Delta Q_m^{sub}$, $\Delta Q_m^f$) and TSP ($Q_{TSP}$) measurements at polarization up to 250°C, that can be considered as the BOX/semiconductor interfaces in SIMOX structure are almost electrically blocking in this temperature range. After thermal polarization up to 400°C the charge measured from TSP current is considerably higher than the transported charge determined from C-V measurements. This may be an evidence of electrical unblocking properties of the BOX/semiconductor interfaces in SIMOX structures at temperatures ranging from 250 to 400°C.

The activation energy of the main polarization process (observed at a negative bias applied to the substrate), determined by the fractional thermal cleaning method, is 1.2 eV. Charge movement during this polarization process at first measurement may reach the value of $1.1 \cdot 10^{12}$ cm$^{-2}$ (see Table 2). In the case of depolarization at zero applied voltage we observed two small current peaks from which the activation energy can be only roughly estimated.

Table 2
The charges, obtained from C-V characteristics and from TSP current technique ($Q_{TSP}$) and charge centroid for SIMOX structures

| Kind of treatment | Parameters | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $\Delta Q_{sub}$ [cm$^{-2}$] | $\Delta Q_f$ [cm$^{-2}$] | $\Delta Q_{tn}$ [cm$^{-2}$] | $\overline{X}_0$ [Å] | $Q_{TSP}$ [cm$^{-2}$] | $\Delta Q_m^s$ [cm$^{-2}$] | $\Delta Q_m^f$ [cm$^{-2}$] | $\Delta Q_{tr}$ [cm$^{-2}$] |
| Initial | $-3\cdot10^{10}$ | $6.8\cdot10^{11}$ | $6.5\cdot10^{11}$ | 3600 | | | | |
| Polarization (250°C) | $1.4\cdot10^{11}$ | $6.2\cdot10^{11}$ | $7.6\cdot10^{11}$ | 2680 | $1.8\cdot10^{11}$ | $1.7\cdot10^{11}$ | $-5.8\cdot10^{10}$ | $1.1\cdot10^{11}$ |
| Polarization (400°C) | $9\cdot10^{10}$ | $7.4\cdot10^{11}$ | $8.3\cdot10^{11}$ | 3270 | $1.1\cdot10^{12}$ | $1.2\cdot10^{11}$ | $6\cdot10^{10}$ | $1.8\cdot10^{11}$ |

We think that the thermal polarization process at negative voltage applied to the substrate of SOI structure is associated with electron emission from traps located near the BOX/substrate interface. The capture cross section for these traps determined from TSP current peak is $8\cdot10^{-18}$ cm$^{-2}$. It should be noted that the flat-band voltage at the BOX/substrate interface is about zero, which is attributed to the complete compensation of the electrical charge located near this interface.

# 4. High-temperature instability of SOI MOSFETs

### *4.1. High-temperature kink-effect of back-channel SOI n-MOSFETs*

The processes of charging and discharging in the BOX at high temperature can lead to some unusual effects in the MOSFETs. In the paper [3] a new high-temperature effect in the SIMOX SOI n-MOSFET named the high-temperature back-channel kink-effect has been described. This effect appears in fully depleted (FD) inversion mode (IM) n-MOSFETs, fabricated on single implanted SIMOX SOI wafer, when a negative voltage is applied to the substrate at a temperature above 200°C and thereafter the back-gate (substrate) voltage, $V_{bg}$, is rapidly swept to a positive value. Under these conditions and with a bias at back gate about zero it was observed that a jump occurs in the source-drain current (Fig. 7). This current jump increases with increasing temperature and hold time of negative voltage applied to the substrate prior to the back-gate voltage sweeping and tends to saturation for high-temperature measurements and for long hold times (Fig. 8a).

The current jump cannot be related to the floating-body effects in the SOI MOSFET because the drain voltage is low during the measurements (0.1 V) and the measurements are performed at high temperature, when the floating body effects have to be suppressed [13, 14]. In order to check that special experiments on the SOI MOSFETs with contact to silicon film have been performed. The source-drain current jump near zero back-gate voltage have been observed beginning from 200°C and have not disappeared when silicon film was grounded. Thus, it is believed that charging and discharging processes in the BOX of the SOI structure are responsible for the observed phenomenon [15, 16].

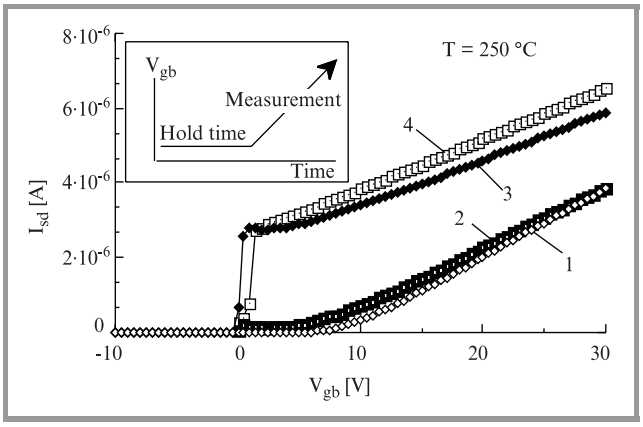


***Fig. 7.*** Drain current versus back-gate voltage for different sweep rates: initial characteristic (sweep rate is 50 V/s) (*1*); the characteristics measured after keeping back gate at −30 V during 150 s and when a sweep rate equals to 1.7 V/s (*2*), 5 V/s (*3*) and 50 V/s (*4*).

The drain-current jump has been explained by the following processes taking place in the BOX of the SOI MOSFET. Firstly, when negative voltage is applied to the substrate at high temperature, a positive charge is accumulated in the BOX. Since this positive charge does not result in an increase of the channel current in the MOSFET, it has been concluded that this positive charge is compensated by a negative electron charge easily injected from the substrate (Fig. 8b). Accumulation of the positive charge has been suggested to be associated with electron extraction from traps located near the BOX/substrate interface. Secondly, when the back-gate voltage approaches to zero, the electrons, located in the vicinity of the BOX/substrate interface, recombine with the thermally generated holes in this region and cannot further compensate the positive charge in the BOX (Fig. 8c). Thus, a sharp increase of the drain current is observed. Thirdly, when a positive voltage is

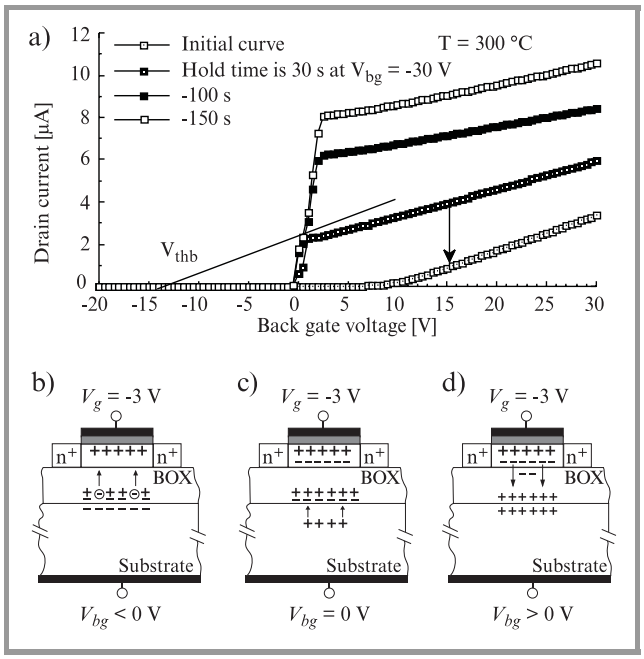


***Fig. 8.*** Drain current versus substrate voltage for different hold times at −15 V (arrow signifies the direction of current relaxation) (a), schematic illustration of the positive charge accumulation in the BOX at $V_{bg} < 0$ V (b), electron recombination at $V_{bg} = 0$ V (c) and the neutralization of the positive charge at $V_{bg} > 0$ V (d).

applied to the substrate, the positively charged traps in the BOX are compensated by electrons injected from the channel of the MOSFET (Fig. 8d). In this case a change in the slope of the $I_{sd}$-$V_{bg}$ – characteristic in dependence of the back-gate voltage sweep rate (Fig. 7) and of the magnitude of the current jump (that is the value of a positive charge accumulated in the BOX) (Fig. 8a) has to be observed.

Using the above considered model and studying the processes of positive charge accumulation (charging) and relaxation (discharging) in the BOX, the parameters of traps associated with these processes have been estimated.

### *4.2. BOX trap parameters extraction from high-temperature kink-effect of back-channel SOI n-MOSFET*

It was shown [15], that the positive charge accumulation in the BOX can be investigated by measuring the magnitude of a drain current jump at different temperatures and hold times of a negative voltage applied to the substrate.

In order to estimate the threshold voltage in the presence of a high-temperature kink effect while taking into account the discharging effect it was suggested to draw the line parallel to the initial $I_{sd}$-$V_{bg}$ – characteristic and passing through the point of the measurement characteristic where the jump is observed (Fig. 8a). The intersection of this line with the voltage axis gives the desired threshold voltage [15]. Using this method the values of positive charge accumulated in the BOX at different temperatures have been obtained (Fig. 9). From these dependences the maximum accumulated positive charge, $Q_{BOXm}$, activation energy of the process of

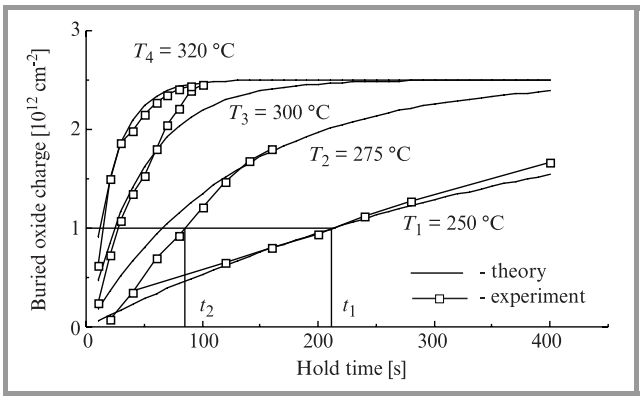


***Fig. 9.*** Theoretical and experimental dependences of positive accumulated charge in the BOX on time at different temperatures.

electrons escaping from the trap, $E_a$, and capture cross section of the traps at room temperature, $S_t$, have been determined. It was found that $Q_{BOXm}$ equals to $2.5 \cdot 10^{12}$ cm$^{-2}$, $E_a$ is 1.1 ±0.1 eV and $S_t$ is $2 \cdot 10^{-17}$ cm$^2$. These values are very similar to those obtained from TSP/TSD current measurements on the same SIMOX SOI structures (see part 3.2).

From studying the drain current relaxation (see part 2.4) at different temperature the activation energy of discharging process that has been equaled to 0.65 eV has been estimated [15]. It has been suggested that electron trapping is associated with multiphonon emission processes, which are an inherent feature of oxygen vacancy defect (E′-center) in dioxide [17].

Comparison of experimentally obtained trap parameters with the published ones [18÷21] leads to conclusion that the observed deep traps, responsible for high-temperature instability in the BOX are possibly related to oxygen vacancies which are capable to trap and release the electrons at high temperature [22, 23].

### *4.3. High-temperature kink-effect of front-channel FD SOI n-MOSFET*

Positive charge accumulation in the BOX of FD SOI IM n-MOSFET can result in additional high-temperature instability of the MOSFET [24, 25]. This phenomenon is simply observed when the set of $I_{sd}$-$V_g$ characteristics is measured in dependence of back-gate voltage changing at high temperature. If, at first, the back-gate voltage is negative, the $I_{sd}$-$V_g$ curves show the jump of the current in the vicinity of the zero gate voltage when the back-gate voltage reaches the positive values (Fig. 10a). In the other case, when in the beginning of the set of measurements the back-gate voltage is positive, the $I_{sd}$-$V_g$ curves have a usual form for all voltages at the substrate (Fig. 10b).

It is worthy noting that this current jump, as well as the high-temperature kink-effect of back-channel MOSFET, depends on the temperature of measurements and is created by the above mentioned condition at the temperatures higher than 200°C (Fig. 11). The observed phenom-

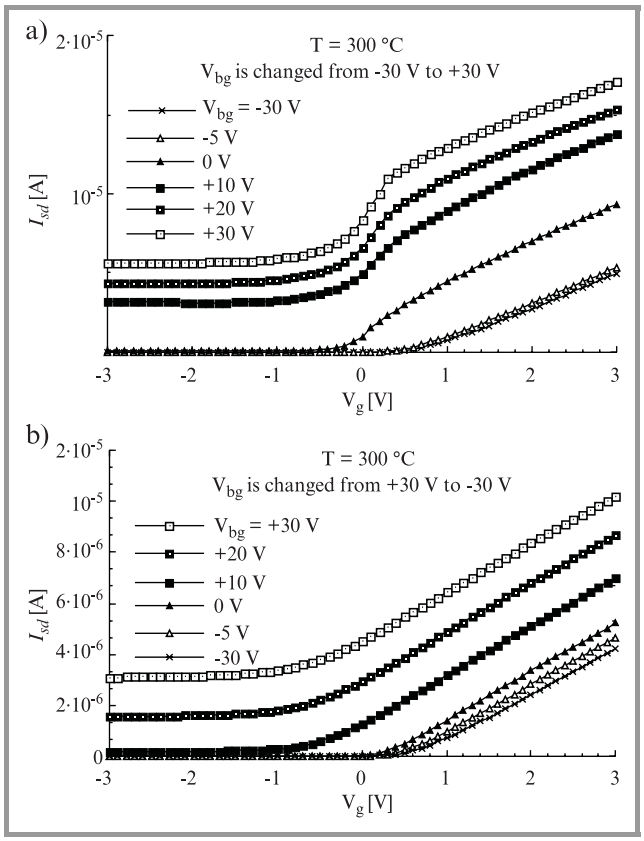


***Fig. 10.*** Source-drain current versus gate voltage for different substrate voltages ($V_{bg}$) at 300°C when substrate voltage is swept from $-30$ V to $+30$ V (a) and from $+30$ V to $-30$ V (b).

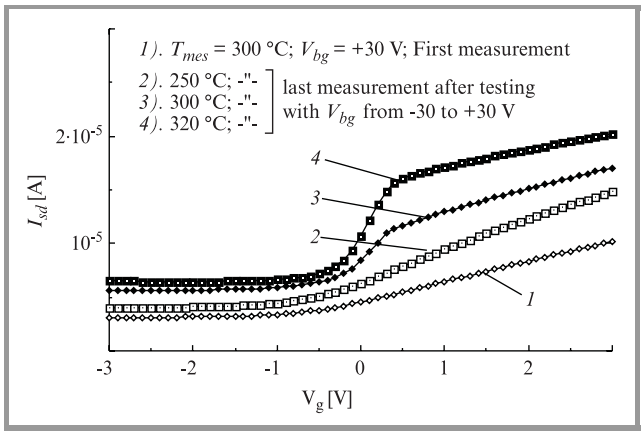


***Fig. 11.*** Source-drain current versus gate voltage for different temperature and sequence of measurement.

ena were named as high-temperature kink-effect of front-channel MOSFET [24].

In the papers [24, 25] the direct link of the drain current jump in the front MOSFET and the positive charge creation in the BOX has been demonstrated. Indeed, the application of negative voltage to the substrate for 150 s at a temperature 250°C leads only to a small shift of the $I_{sd}$-$V_g$ curve towards more negative gate voltage values, showing that some small positive charge is produced in the BOX

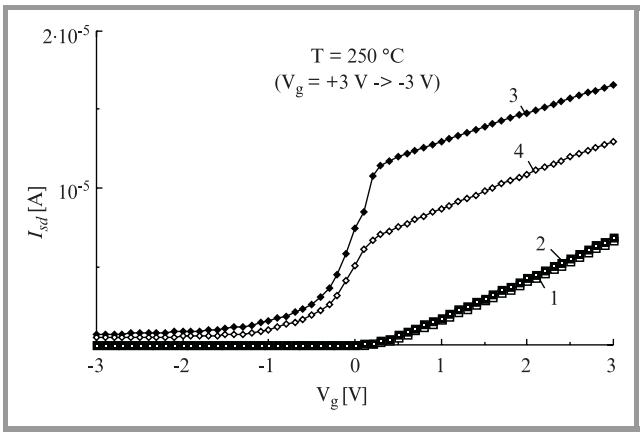


***Fig. 12.*** Source-drain current versus gate voltage in dependence on conditions of the substrate: (*1*) $V_{bg} = -30$ V, hold time is 0 s; (*2*) $V_{bg} = -30$ V, hold time is 150 s; (*3*) $V_{bg} = -0$ V, hold time is 0 s after stressing at $V_{bg} = -30$ V for 150 s; (*4*) $V_{gb} = 0$ V, hold time is 150 s.

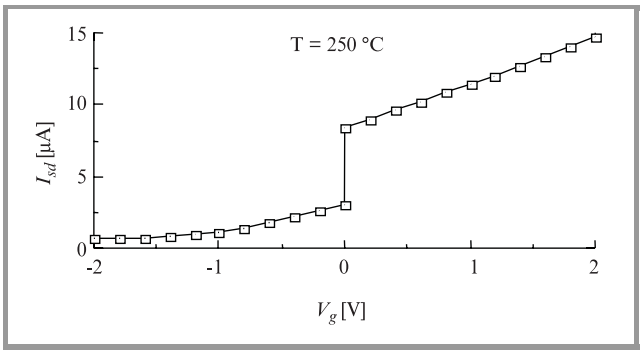


***Fig. 13.*** MEDICI simulation of the drain current „jump". For $V_g > 0$ the curve was calculated for the case of a uniform positive charge distribution as a function of depth in the BOX. The positive charge $3.5 \cdot 10^{17}$ cm$^{-3}$ is uniformly distributed within a distance of 200 nm from the BOX/substrate interface. For $V_g < 0$ the curve was calculated for the same positive charge distribution, but where $1.05 \cdot 10^{12}$ cm$^{-2}$ electron charge is located in the BOX near the BOX/silicon film interface.

(curve *1* and *2* in Fig. 12). In this case as it was shown in [15] the positive charge, compensated by electrons from substrate, are accumulated in the BOX (see Fig. 8b). If the substrate voltage is switched to zero, the discompensation of the positive charge in the BOX (see Fig. 8c) takes place and considerable current increase and formation of a current jump appears (curve *3* in Fig. 12). After that, if the drain, the source and the substrate are shortened for 150 s, the values of the drain current and the magnitude of the current jump decrease (curve *4* in Fig. 12). This attests that the compensation of the positive charge in the BOX (the process is shown in Fig. 8c) leads to the decrease of the current jump in the $I_{sd}$-$V_g$ characteristics.

The phenomenon can be due to simultaneous influence of two effects. The first one is related to gate voltage influence (due to charge coupling effect) on trapping of electrons from the back channel of the MOSFET into the electron

traps located in the BOX near the BOX/silicon film interface when the negative voltage applied to the gate. The second one is associated with considerable positive charge built-up into the BOX. At positive voltage applied to the gate an electric field at the BOX/silicon film interface decreases that leads to electrons release from the traps and increase of drain current. 2D MEDICI simulation [26] of this effect is presented in Fig. 13.

## 5. Conclusions

The developed complex of high-temperature methods for SOI capacitors and MOSFETs allows the processes of charge building up and neutralization in buried dielectrics of SOI structures and effect of this charge on SOI MOSFET operation to be studied.

In the LZMR SOI structures the BOX/semiconductor interfaces are almost electrically blocking up to 350°C, which leads to small discharging of internal BOX charge through these interfaces. The main processes of charge instability at high temperature in LZMR SOI BOX are linked with an ionic charge transport and determined by technological process cleanness.

In SIMOX SOI structures the BOX/semiconductor interfaces (especially the BOX/substrate interface) are electrically unblocking at temperatures above 200°C. This leads to considerable charge exchange through these interfaces at high temperatures. The building up of positive charge in SIMOX BOX and its neutralization is determined by charging processes of structural defects located near the BOX/substrate interface (for example, oxygen vacancies and oxygen vacancy complexes).

Positive charge incorporated into SIMOX BOX can lead to instability of the MOSFET high-temperature operation, which appears as uncontrolled MOSFET threshold voltage shift and drain current jump near zero gate voltage.

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*Invited paper*

# Challenges in ultrathin oxide layers formation

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and Michał Korwin-Pawłowski

**Abstract — In near future silicon technology cannot do without ultrathin oxides, as it becomes clear from the „Roadmap'2000". Formation, however, of such layers creates a lot of technical and technological problems. The aim of this paper is to present the technological methods that potentially can be used for formation of ultrathin oxide layers for next generations ICs. The methods are briefly described and their pros and cons are discussed.**

***Keywords — silicon technology, oxidation, PECVD, RTO, gate oxide, ultrathin layers.***

## 1. Introduction

The ultrathin silicon oxide layers have been within the scope of interest of researchers for many years, now. However, only recently, this topic has become of great importance to ICs manufacturers. They have created an extreme pressure, which results in great number of works on the problems related with ultrathin oxide manufacturing, characterisation and reliability. The reasons are clear when looking at „Roadmap'2000" (see Table 1). It is not only that within two to three years the equivalent oxide thickness is expected to fall below 1.5 nm, but also, that the methods of its formation in this thickness range is not known.

The roadmap, however, does not explain the physical background of these revolutionary steps. These physical reasons are, obviously, dependent on the type of the semiconductor device considered. Thus, for MOSFETs, where ultrathin oxides are used for **gate dielectrics**, the reasons for their thickness reduction are:

- to increase transconductance, as: $g_m \sim C_{ox} \sim \varepsilon_{ox}/t_{ox}$;
- to avoid short channel effects, as: $t_{ox} \sim 1/\lambda$;
- to minimise parasitic oxide charge effect.

In DRAMs, such layers are used for **capacitor dielectric**, and their reduction allows farther reduction of area covered by capacitors $A_C$, while maintaining minimum storage charge, as: $Q_{\min} \approx V_p C_{ox} \sim V_p A_C \varepsilon_{ox}/t_{ox}$.

In EEPROMs and Flash EPROMs, where they are used as **injection dielectric** farther reduction of these layers thickness results in increase of injection efficiency, as $I_{tunnel} \sim \exp(-\beta/t_{ox})$.

In all these applications, lists of prime parameters to be obtained are little different, still, in all of them these layers are playing very important role in device operation.

In some of the presented above cases dependencies shown prove, that reduction of dielectric layers thickness can be compensated by increase of dielectric layer permittivity. This is a promising sign, as further reduction of dielectric layer thickness is very limited due to basic physical limitations (one cannot form continuous layer of less that one monolayer thickness, although such thin layer would have unacceptably low reliability). Another words, by changing the dielectric layer from the so far used silicon oxide to the material characterised by higher than the oxide permittivity value, we can achieve the same goals without farther reducing the dielectric layer thickness. In fact, this move should also to be taken into account when looking for the next stage ultrathin gate dielectric technology.

## 2. What does define final oxide thickness?

If we compare the size of a $SiO_2$ molecule with expected thickness of the ultrathin oxide layer, that we want to obtain in the real device, we realise, that the layers we are dreaming about in the future are only few (two to three) monolayers thick[1]. This thickness is also comparable with the thickness of interface region (as it was determined some years ago by HRTEM method), interface roughness and „natural oxide"[2] thickness. Thus, it becomes clear, that all the situations where silicon can become oxidised have to be taken into account when ultrathin oxide growth is studied. The final oxide thickness is determined by following processes:

- silicon surface cleaning process;
- oxidation process (in case of thermal oxidation this would include all its individual stages, namely: pre-oxidation stage heating up, oxidation itself, and post oxidation – e.g. POA if applicable).

During the „silicon era" few different approaches for silicon cleaning have to be distinguished and shortly discussed in reference to the main technological aim – i.e. formation of ultrathin oxides on Si surface.

[1]We have to realise, however, that due to the amorphous character of the oxide layer, the oxide thickness cannot be, for formal reasons, expressed in number of monolayers.

[2]The „natural oxide" is an oxide of poor quality spontaneously grown when the bare silicon surface is exposed to the ambient atmosphere (unless is purposely hydrogen terminated).

Table 1
Long term roadmap

| Indicators | Years | | | | | |
|---|---|---|---|---|---|---|
| | 1999 | 2002 | 2005 | 2008 | 2011 | 2014 |
| Technology node [nm] | 180 | 130 | 100 | 70 | 50 | 35 |
| $T_{ox}$ equivalent OET [nm] | $1.9 \div 2.5$ | $1.5 \div 1.9$ | $1.0 \div 1.5^{*)}$ | $0.8 \div 1.2^{*)}$ | $0.6 \div 0.8^{*)}$ | $0.5 \div 0.6^{*)}$ |
| MPU gate length post etch [nm] | 140 | 90 | 65 | 45 | 30 | 20 |
| $^{*)}$ Technology of these dielectric layers is not yet known. | | | | | | |

The original „RCA method" proposed by Kern [1] has been focused on leaving the silicon surface unprotected, however, with minimum oxide layer on its top. It consisted of S.C.-1 and S.C.-2 being followed by HF etching of silicon oxide, as last treatment. Due to extremely high reactivity of bare silicon surface, „natural oxide" was growing spontaneously afterwards. As a result of that, the starting point for silicon oxidation would strongly depend on the time spent between HF last etching and the beginning of the oxidation process. It is important to realise that the quality of the „natural oxide" (as it grows in clean-room atmosphere) is very poor in both, purity and defects.

Realising the fact, that inevitably, at the beginning moment of oxidation we have certain thickness of natural oxide, the approach has been changed to „better good purity than poor". In practice this has ment, that HF etching has been moved in-between the S.C.-1 and S.C.-2 processes. The S.C.-2, being the last in this sequence, left the silicon surface covered with some 1.5 nm to 2.0 nm of the „chemical oxide", which was still of poor quality, but at least was grown in controlled, chemical ambient. Thus, „chemical oxide" exhibited better than „natural oxide" purity and did not change its thickness in time giving reasonable and repeatable starting point for the standard oxidation process.

When ultrathin oxides are to be formed (e.g. below 3.0 nm), however, even the lower range of the „chemical oxide" thickness is difficult to accept. Thus, a lot of the pressure has been made to find out some other possible cleaning procedures, which would result in still thinner oxide to start oxidation from. This has led to the hydrogen passivated silicon surfaces, in which pretty stable Si-H bonds are created at the silicon surface, by HF last etch. In fact, only these procedures allow the growth of ultrathin oxide in a controllable way starting from basically bare silicon surface.

The oxidation process is also not a one step process, thus, the oxide growth can take place during all of them. The schematic view of the processing stages for the thermal oxidation is shown in Fig. 1. In fact, oxide growth can take place any time when hydrogen termination is removed (due to elevated temperature or even intensive rinsing in water). Thus, in the thermal processing, the silicon surface is prone to oxidation already during the temperature ramp up and temperature stabilisation stage, and later, also during the post oxidation annealing – POA (if applicable),

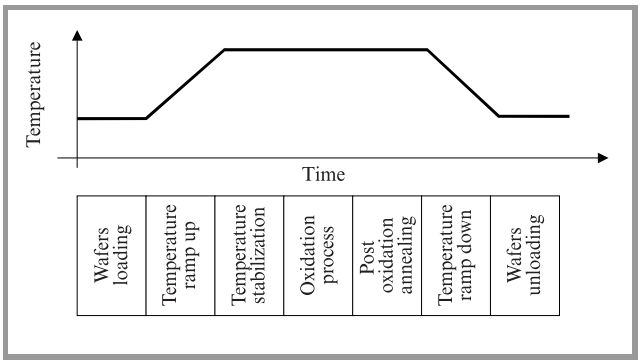


***Fig. 1.*** The schematic view of the temperatures in the furnace during all the stages of the thermal oxidation process performed in the classical furnace.

or temperature ramp down. As a consequence, the finally obtained oxide thickness can differ from the assumed one determined basing on the kinetics of the oxidation process used only. This problem will be discussed in more detail in paragraphs below.

## 3. High temperature thermal oxidation in classical furnace

### *3.1. Kinetics of thermal oxidation*

The kinetics of thermal oxidation process has been studied already for many years. The most important problem to overcome in these studies was how to avoid the mentioned above influence of pre- and post-oxidation steps on the oxide growth. The only group that succeeded in this respect was Young et al. [2], who installed ellipsometer in their furnace, allowing *in situ* dynamic readout of the oxide growth[3]. However, also this experimental set up required that the important assumptions had to be made – namely, they had to assume the refractive index temperature dependence.

[3]Although such experiments gave a lot of information for studies on oxidation kinetics, from practical point of view they were of practically limited use, as for real processing it is the final oxide thickness (including the influence of pre- and post-oxidation stages) that matters.

The well known set of curves they received is shown in Fig. 2. The first obvious consequence of these curves is that ultrathin oxides require extremely short oxidation times, particularly for higher oxidation temperatures. For example, formation of ultrathin oxide in 1000°C takes, according to the presented curves, few minutes only.

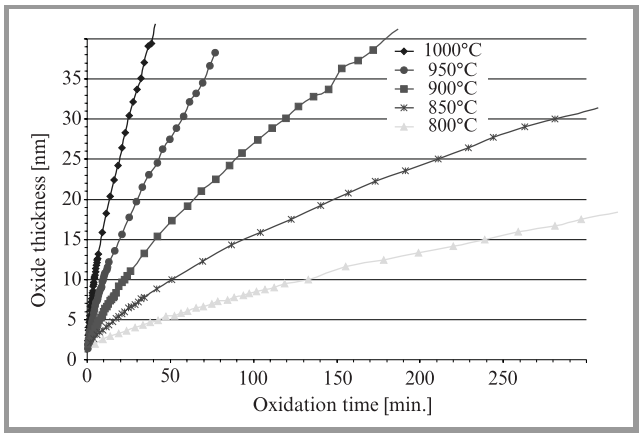


***Fig. 2.*** Kinetics of thermal oxidation in the range of ultrathin and very thin oxide layers for exemplary temperatures from the range between 800°C and 1000°C.

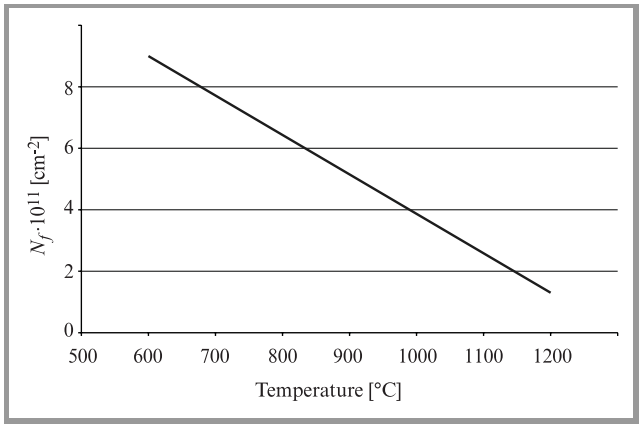


***Fig. 3.*** The experimentally obtained relation of $N_f$ (density of fixed oxide states) versus oxidation temperature, showing the relation of oxide quality with the temperature of its formation.

Much more controllable, in this thickness region, is oxidation in lower temperatures (e.g. 800°C), however it is widely known (see Fig. 3) that higher is the oxidation temperature the better is oxide quality (this relation is also known as „Deal's triangle"). Thus, some sort of compromise has to be reached. It seems that these compromises are set differently in different companies, according to their previous experience and technological skills.
It has been already shown before [3, 4] that oxidation rate can also be decreased by reducing the oxygen partial pressure during the process. The reduction of oxygen partial

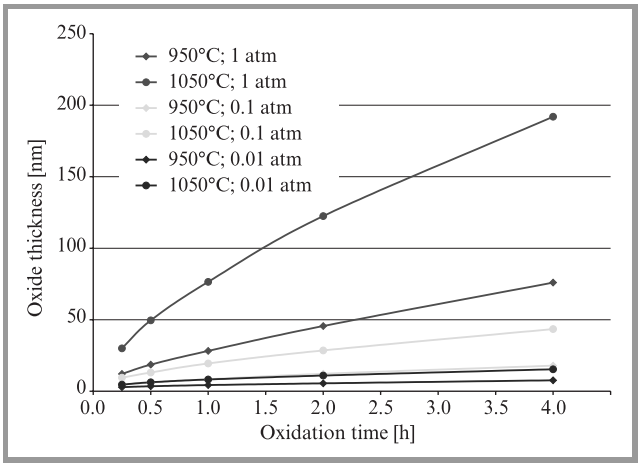


***Fig. 4.*** The experimentally obtained kinetics of high temperature oxidation under the reduced pressure conditions, showing that by reducing the oxygen partial pressure one can significantly slow down the oxidation rate for given process temperature.

pressure can be performed either by running the process under the vacuum conditions (with some oxygen refilling) or by oxygen mixing with the neutral ambient gas (like argon). Although the former solution requires dedicated, vacuum tight set up – the latter one can be performed in classical furnace, only after some minor modifications.
The exemplary kinetics of such oxidation is presented in Fig. 4. One can realise that from the ultrathin oxide layer formation, the interesting oxygen partial pressure would be of the order of 0.001. One has to realise, however, that mixing of gases in such proportions is not a trivial problem.

### *3.2. Issues resulting from furnace construction*

#### 3.2.1. Gas exchange rates

The horizontal furnaces are, in order to allow simultaneous processing of few wafers lots, is about 2 m long, while the tube diameter is wafer size dependent. This results in very high volumes of the furnace tubes, which has crucial consequences as far as the gas exchange issue is considered. For the sake of simplicity we will consider in our discussion below oxidising gas as pure oxygen, although, in reality, oxidising gas may be a mixture of oxygen and ambient gas (nitrogen or argon) and/or chlorium containing gases (e.g. HCl or TCE). The oxidation time is, then, determined technically by the time between mass flow controller (MFC) on oxygen gas line is turned on (to begin oxidation) and then off (to end the process). The situation looks totally different from the wafers located along the furnace tube in the quartz boats point of view. Prior to oxidation start the furnace tube is filled with ambient gas (usually nitrogen or argon) with some very small addition of the oxygen (to avoid pitting), which has been flowing through it during the previous stages of the process (namely, during: loading the tube, heating up the whole furnace and temperature

stabilisation). The oxygen getting through the tube end replaces the previous gas composition gradually (see Fig. 5). Assuming, for the sake of simplicity, that the „new gas" is replacing „old one" without mixing with it nor any turbulence, the moment that the wafers face oxidising ambient is position (in the tube) dependent. Consequently, the wafers located at the far end of the tube start their oxidation first, while the one close to the loading station – the last. This effect could be reduced (or even eventually compensated) if only the gas replacement after the oxidation process would have the same dynamics (resulting from the same gas flow). However, this simple method does not hold when gas mixing and some turbulence during the gas flow is taken into account.

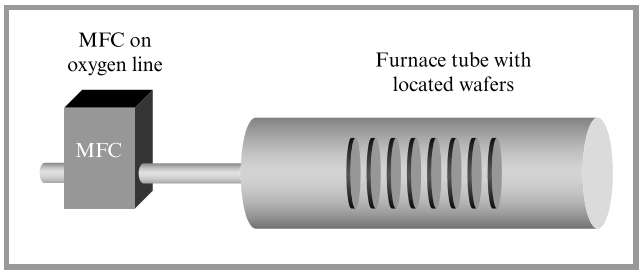


***Fig. 5.*** Schematic view of the classical furnace set up, with the mass flow controller controlling the oxidation time, and wafers located along the furnace tube.

We can, therefore, conclude that some period of wafers oxidation time is basically out of the control and that this time is for particular furnace gas flow rate dependent. In order to reduce it, the possibly high gas flows rates are advantageous.

The gas flow rate is, however, limited from the top by cooling effect of the wafers and creation of turbulence flow within the furnace tube. Particularly the former effect is extremely important in high temperature oxidation, which is so sensitive to the process temperature. Consequently, the gas flow is limited (depending on the diameter of the tube, which in turn depends on the processed wafers diameter) to few standard litres per minute (slm), which when compared with typical volumes of tubes results in at least few minutes of gas replacement stage.

This discussion proves that few minutes of uncontrollable oxidation seem to be unavoidable in oxidation in standard furnaces.

#### 3.2.2. Temperature ramp up and ramp down dynamics

The time length of the temperature ramp up is limited by wafer warpage effect. It is, therefore, determined by the diameter of the wafers used[4], however, for number of years already the 10°C/min has seemed to be the widespread standard value of the ramp up rate. Typical stand-by temperature of the furnace is usually between 700°C and 750°C, hence, even for low oxidation temperatures (like e.g. 800°C) the ramping up must take at least some minutes.

On the contrary to ramping up, the ramping down dynamics is only furnace construction dependent. It has to be pointed out, that it is often even slower than the ramp up rate, thus, we have yet some more minutes of wafers presence in high temperature and, as a result of it – still longer time of probable uncontrollable oxidation.

Traditionally, the post-oxidation period was supposed to be not affecting the control of the oxidation process. This has been true, for thicker oxides, where due to the saturation type of kinetics of oxidation, the rate of oxide growth for thicker oxides is much smaller than for very thin ones. For the ultrathin oxides, however, there is no significant difference between oxide growth rate before and after oxidation process, thus, in this case post-oxidation growth can also influence considerably to the final thickness of the oxide layer. This effect is, thus, also important for the setting POA stage for ultrathin oxide processing.

[4]In order to avoid wafer warpage due to non-uniform wafer heating during the heating process, low ramping rates have to be used.

## 4. Rapid thermal oxidation

Rapid thermal oxidation (RTO) technique, has been developed as one of the possible applications of rapid thermal processing (RTP) reactors that have been developed in late eighties. Commonly used for very short annealings, RTP reactors, which allow very high temperature processing (often up to 1300°C) and very abrupt temperature changes, have been often considered for oxidation process. As long as the thickness of the oxide to be grown was not so thin, there were no clear advantages of this process versus standard oxidation. Now, when considering ultrathin oxides formation, RTO seems to be very strong candidate to become new standard gate formation technique.

### *4.1. Kinetics of RTO process*

Despite what has been believed at the beginning of its introduction to technology, RTO kinetics is essentially the same as of the standard thermal oxidation performed in the furnace. This point has been proved in [5], where theoretical model of high temperature oxidation successfully fitted to standard oxidation gave also excellent fit for RTO experimental data. The problems from the past where then attributed to poor modelling efforts and ignoring effects important within the region of ultrathin oxide from growth considerations. Important differences, however, do exist, but they refer to the pre- and post-oxidation period, allowing gaining better control over the whole oxidation process. First of all, RTO reactors operate on single wafers, thus, the inner volume of the quartz tube is very small (of the order of few litres only – comparing to the horizontal furnace of several hundreds litres). Hence, in RTO, the gas exchange times are very small indeed.

Also ramping up and ramping down rates are in RTO very high, due to high electric power applied to the heating systems and very small heated mass (one wafer only). The ramping rates of the order of 200°C/s are not uncommon in this type of equipment.

These two features allow solving the problem of too long pre- and post-oxidation stages in ultrathin oxidation.

Extremely fast ramping generates, however, some other problems in RTO processing. The main issue here is uniformity of the temperature across the wafer at all the stages of the process, namely, during: ramp up, oxidation and ramp down. Number of effects affects this uniformity. This results, at the worst case, in build up of dislocations and slip lines within the silicon substrate, thus, these effects they cannot be ignored. The most important of them will discussed briefly below.

In order to obtain so high ramping rate without the wafer warpage, temperature across the wafer has to be uniform during the whole process. Wafer edges, however, radiate out heat much easier than wafer inner part, thus, in order to satisfy this demand, special profile of the energy source radiation has to be executed in the reactor (higher energy at the wafer edges to compensate mentioned above energy loss at the edges)[5]. If this condition is not satisfied, cooler wafer edges create a mechanical stress upon the inner wafer part, which has two different consequences. First, the mechanical stress triggers up the build up of the structural defects in the processed wafers. Secondly, mechanical stress has significant influence upon the kinetics of the oxidation process hence, we may obtain non-uniform oxide thickness. For ultrathin oxide layers, where we hope to control formation of few monolayers of the oxide, lack of uniformity, as well as defects in the silicon substrate, are very important reliability issues. Thus, both effects are dangerous for modern ICs, hence, high priority to solve this problem.

The nature of the heating in RTO reactors is also different than in classical furnaces, as the energy transfer from the source to the wafer takes place, in this case, by photons radiation and not by convection mechanism. Thus, the temperature of the object in the reactor is dependent on the absorption properties of the material to be heated. The obvious consequence of this fact is that silicon wafer which may be covered by various patterned layers (of different absorption properties) can exhibit locally different temperatures. Such temperature differences result in local stress, which after incubation period leads to local defects in the wafer structure. Even local differences in the same type of layer thickness (e.g. field oxide – FOX and gate oxide – GOX) can lead to dislocations, as can be seen in [6]. This is a very serious problem, as no compromise can be made in patterning the layers used for ICs construction (they result from the ICs layouts), nor we can change the types of layers used.

Concluding on RTO, we could say, that two main problems of ultrathin oxidation in standard furnace seem to be solved by the RTO, however, other technological problems are generated by this technique. Still, RTO is obviously among the most important players for extreme ultrathin oxide formation.

[5]Thus, RTO reactors can perform well only for the assumed by manufacturer wafer size.

# 5. Plasma enhanced chemical vapour deposition

Plasma enhanced chemical vapour deposition (PECVD) is one of the few deposition methods which involves chemical reaction between gas reagents introduced into the reactor, thus, no chemical bonds with the substrate are established. Very important consequence of this fact is that, unlike in thermal oxidation, new layer can be grown on any substrate, as the substrate is not a source of any chemical elements needed for the reaction. Hence, this method gives us a lot technological flexibility. Above all, changing the types of gases supplied to the system, can immediately, without removing the wafer from the system, switch the type of material deposited. Hence, this method can basically be considered not only for single, but also for double, or even multiple layers formation. These are obviously very important pros for CVD techniques.

In PECVD methods very reactive radicals are produced rather by plasma excitation than thermal activation. This allows considerable reduction of temperature required for the CVD process. For example, silicon oxide layers can be formed in temperatures around 150°C ÷ 400°C rather than in 600°C ÷ 1000°C, which drastically reduces „thermal budget" of the ICs manufacturing.

On the other hand, precision of the deposition time control is very good, as due to the facts, that PECVD takes place in vacuum chamber, and the process without plasma basically does not take place.

From the early beginning, however, due to previously mentioned well known relation between the formation temperature and quality of the oxides, PECVD have never been seriously considered for gate oxide layer formation. Thus, the main advantage of this method, as it was believed then, was possibility to manufacture thick dielectric layers at the high deposition rate and very low temperatures. This has oriented PECVD methods for many years mainly for manufacturing thick dielectric films[6]. Even now, most of the process recipes are for processes characterised by deposition rate of the order of 50 nm/min. In order to control well deposition rates within the ultrathin range we require, however, deposition rates at least 10 times lower.

Reoptimising the PECVD process in order to meet such deposition rates is, however, possible although is not a trivial matter – it usually requires some changes in typical set up (e.g. lower MFCs range, or adding gas mixing modules). Then, the problems of non-uniformity and overall

[6]The exception to this rule were investigations of possible use of PECVD ultrathin films for DRAM capacitors (where the requirements for quality of the dielectric layers are much lower), which were carried out since late eighties.

poor quality of the deposited layers still have to be overcome. So far, the properties of PECVD layers have fallen well behind the ones obtained by thermal oxidation (including RTO) but much effort is spent in order to improve the results.

## 6. Other techniques reported

It is interesting to realise what are other candidates for ultrathin oxide processing. Among them, we have two processes that have been in the waiting-room of the silicon technology already for number of years, namely: plasma anodisation and oxidation. There is also number of completely new techniques around. One of the most interesting among them seems to be GRILOX. Below you will find brief comments on their possible applicability to ultrathin oxides formation.

### *6.1. Plasma anodisation*

Plasma anodisation is a process in which oxygen ions that are produced in plasma region, are transported to the oxide-silicon interface due to the electric field appearing across the already formed oxide (on the top of silicon wafer), where they undergo chemical reaction with silicon atoms that forms silicon oxide layer. This process, as it was proved experimentally many years before [7], allows formation of thin but also ultrathin oxide layers in low temperatures and with the growth rate enabling full control of the process and its automation. The control of the process is very simple, as one measures voltage drop across the sample – plasma system, which value can be scaled vs. oxide thickness.
Due to reasons similar to mentioned in description of PECVD, also in plasma anodisation there is no problem with the pre- and post-oxidation growth (as it was the case for thermal oxidation).
The properties of the obtained oxide layers were reported [8] to be comparable with classical thermal oxidation (especially after performing additional short annealing procedure).
The feature that prevented, in our opinion, previous application of plasma anodisation for silicon processing was the fact, that by its nature the process is single wafer. Nowadays, when more and more processes are performed in single wafer reactors, this is no more a decisive drawback.

### *6.2. Plasma oxidation*

Plasma oxidation instead of using oxygen ions uses oxygen neutral radicals excited in the plasma region. They are eagerly forming the bonds with silicon if they meet them. As the oxygen radicals are not charged, their transport through the already formed oxide layer can take place due to diffusion, which cannot be very effective in low temperature that this process takes place in. Thus, the process kinetics saturates very quickly, at the thicknesses of the order of few monolayers. One cannot control the process very efficiently, however setting the process parameters in such a way that the saturation thickness would be thickness of interest, seems to be very interesting proposal for ultrathin oxide formation in very low temperatures.

Both above mentioned techniques allow basically combining them with some reduced pressure techniques, thus, are prone to farther development when the need of double gate insulators will come.

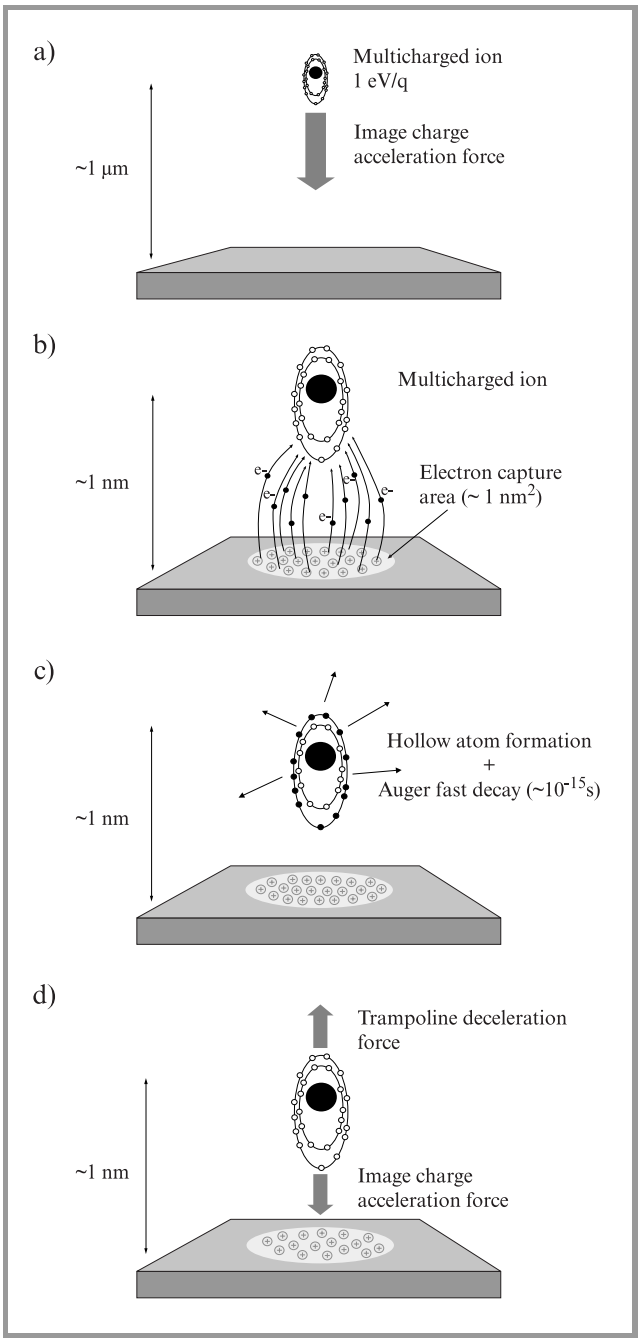


***Fig. 6.*** Schematic view of the stages (a ÷ d) of the GRILOX process leading to the oxidation of the silicon surface by low energy multicharge ions collisionless interaction with the silicon surface [9].

### *6.3. GRILOX*

This method, which is subject to number of patent pendings, and is described in more details for example in [CC], relays on „trampoline effect", which prevents slow multicharged ion bombardment of the solid state surface (see Fig. 6). During this process, surface bonds of the substrate break up and this state can be kept on for some minutes, due to the very high vacuum in the experimental system ($10^{-10}$ Tr). Introduction of some oxygen into the system results in the formation of silicon – oxygen bonds, namely – formation of silicon oxide. As there is no electric field within he already formed monolayers of the oxide layer, there are no means to support oxygen transport through it towards silicon surface (similarly like in plasma oxidation). Thus, process ends very quickly, when only two, three monolayers of oxide are formed. This way the process ends well within interesting region of ultrathin oxide layers and no special control method of oxidation kinetics is required. So far we do not know anything about the properties of ultrathin oxide formed by this method, however, thus, it is too early to calculate its chances in the competition. Still, it certainly is worth noticing and keeping an eye on the results of its development in near future.

## 7. Conclusions

After the presented above discussion it seems clear, why the „Roadmap'2000" does not specify the technology of the gate dielectrics after 2005 (expected thickness below 1.5 nm). All the discussed methods have some pros and cons. Some, like thermal oxidation have been used for long for GOX in the ICs manufacturing, have very good reputation for the quality of the layers, but bring many problems with the ultrathin oxidation process control. RTO seems to solve some of the problems that classical thermal oxidation has with the process control, however, it brings some others.

PECVD, on the other hand, has never been seriously considered for such demanding process as GOX fabrication, however a lot of effort has been recently spent in order to study possible limits of the obtained layers quality improvement. Still, good control of the process and low temperature make this method worth studying as possible technology of ultrathin GOX.

In respect to plasma anodisation and plasma oxidation one should realise, that the features of these method, which until now, were considered as unacceptable from the mass scale manufacturing point of view, are no more so decisive. Good properties of the anodic oxide, as well as precise control of the process and its low temperature are definitely important factors for these methods.

Finally, one should realise that also completely new methods are appearing (like e.g. GRILOX) and that they need some time to prove weather they can take part in the competition to become next generation technology of the ultrathin gate dielectric, or not.

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Paper

# Piezoresistive sensors for atomic force microscopy – numerical simulations by means of virtual wafer fab

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**Abstract — An important element in microelectronics is the comparison of the modelling and measurements results of the real semiconductor devices. Our paper describes the final results of numerical simulation of a micromechanical process sequence of the atomic force microscopy (AFM) sensors. They were obtained using the virtual wafer fab (VWF) software, which is used in the Institute of Electron Technology (IET). The technology mentioned above is used for fabrication of the AFM cantilevers, which has been designed for measurement and characterization of the surface roughness, the texturing, the grain size and the hardness. The simulation are very useful in manufacturing other microcantilever sensors.**

***Keywords — atomic force microscopy, piezoresistive sensors, technology simulation, technology characterization.***

## 1. Introduction

Scanning probe microscopy (SPM), based on the interaction of the Van der Waals forces, is a breakthrough technology that allows three-dimensional imaging and measurement of structures from the atomic to the micron scale. Atomic force microscopy, which followed few years later, measures the attractive or repulsive forces between tip and sample. AFM can be used for measurements of conductive and non-conductive samples. The typical applications are:

- semiconductors – characterization of silicon surface roughness, implant carrier distribution, defect in layers, sub-micron geometry devices and mask development;
- data storage and magnetic materials – characterization of topography and magnetic domains with very high resolution;
- biotechnology – analysis of cellular motion, viscoelasticity and morphology, protein structure and wide variety of biomaterials;
- electrochemistry – real-time imaging of surface chemical processes, electropolishing and corrosion;
- material characterization – analysis of surface roughness, surface stiffness, surface structure, grain size and defects.

Characterization of the interfacial phenomena like friction and wear is particularly important for the effective design of microdevices (Fig. 1).

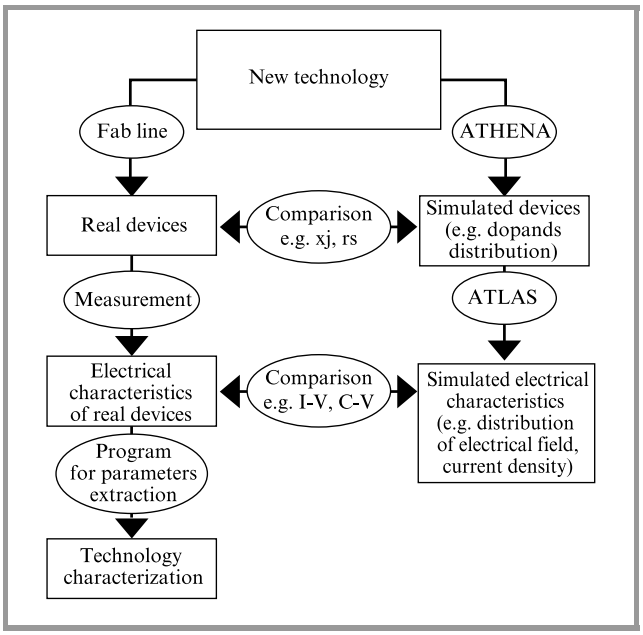


***Fig. 1.*** Correlation between technology process characterization and simulation.

## 2. Theory

The most typical construction of the AFM is a silicon cantilever with an integrated piezoresistive deflection detector. The displacement of the cantilever is sensed by the piezoresistive Wheatstone bridge. The mechanical stress change the resistance of the piezoresistors. To obtain optimal maximal resistivity variation the Wheatstone bridge is located in the crystal orientation [110] (Fig. 2). The bridge output voltage $U_{out}$ due to electrical scheme (Fig. 3) can be calculated:

$$U_{out} = \frac{12\xi l U}{b d^2} F \ ,$$

where $\xi$ – piezoresistive coefficient, $l$ – cantilever length, $b$ – cantilever width, $d$ – cantilever thickness, $U$ – supply voltage, $F$ – force.

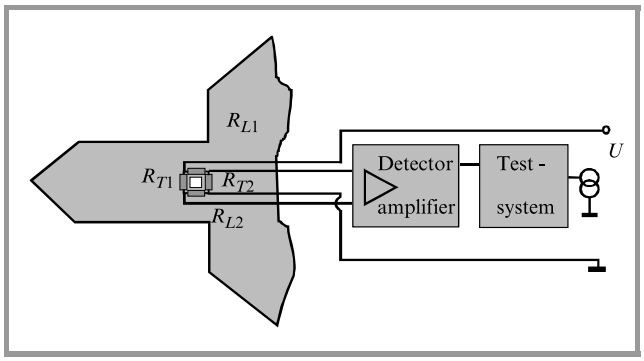


***Fig. 2.*** Electrical scheme of the piezoresistive cantilever measurement system.

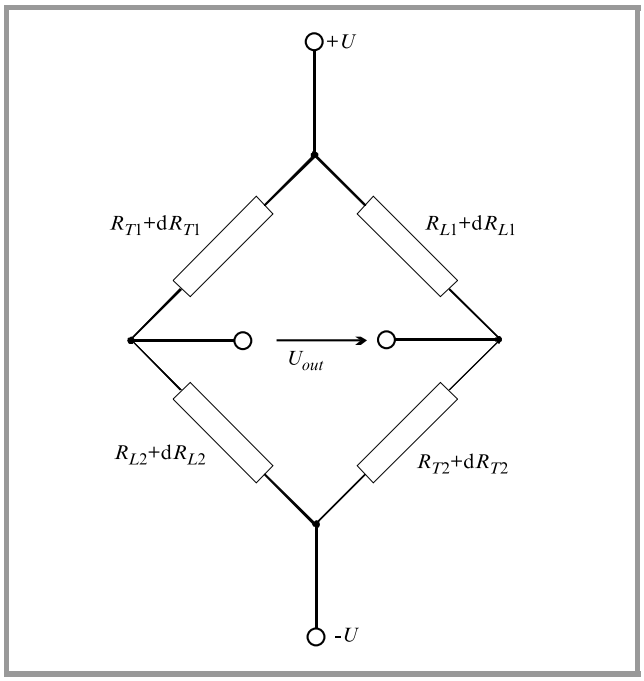


***Fig. 3.*** Electrical scheme of the piezoresistive Wheatstone bridge.

The equation describes the piezoresistive cantilever in the contact mode. In this method forces from 1 nN to 100 nN acting on the tip can be measured. Bridge output voltage $U_{out}$ strong depends also on the beam geometry.

## 3. Simulation

Every technological experiment must be preceded by detailed considerations of the assumptions, proposed solutions and its expected results. The technical experience supported by advanced CAE techniques and software is very relevant at this point. Such an approach is a common practice in IET, where the simulation package developed by SILVACO (USA) is used. Two simulation tools: ATHENA/SSUPREM4 and ATLAS/SPISCES are the basic parts of our system (Fig. 4).

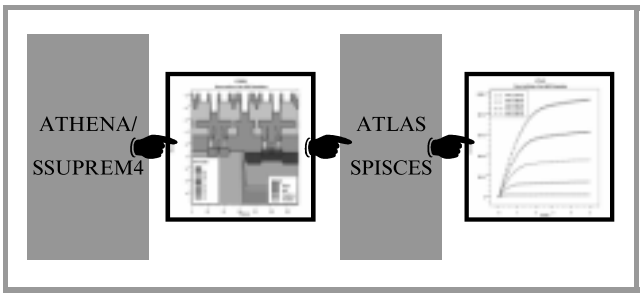


***Fig. 4.*** Simulation package developed by SILVACO (USA).

ATHENA is a very complex program for numerical simulation of sequences of technological processes. It enables both one- and two-dimensional simulation of the following processes: diffusion, oxidation, deposition, chemical and plasma etching and ion implantation. The models of these processes are controlled by a great number of parameters which determine the model's complexity on their characteristics.

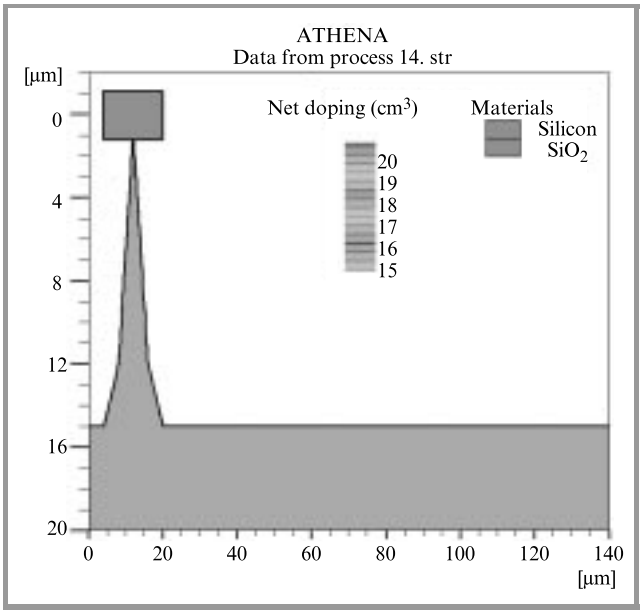


***Fig. 5.*** Cross-sections of the piezoresistive cantilever – tip etching.

ATLAS is a software for numerical two-dimensional simulation of electrical characteristics of semiconductor devices. It enables calculation of DC, AC and transient characteristics.

ATHENA/SSUPREM4 input data file contains a detailed description of the material used as a bulk of the device, its crystallographical orientation, type of the conductivity and resistivity. Modelling of the subsequent processes is the next stage of simulation. The engineer determines the processes parameters, like operations duration, the temperatures, processes atmosphere, doping concentrations, type, stechiometry and the density of the deposited layers, doses

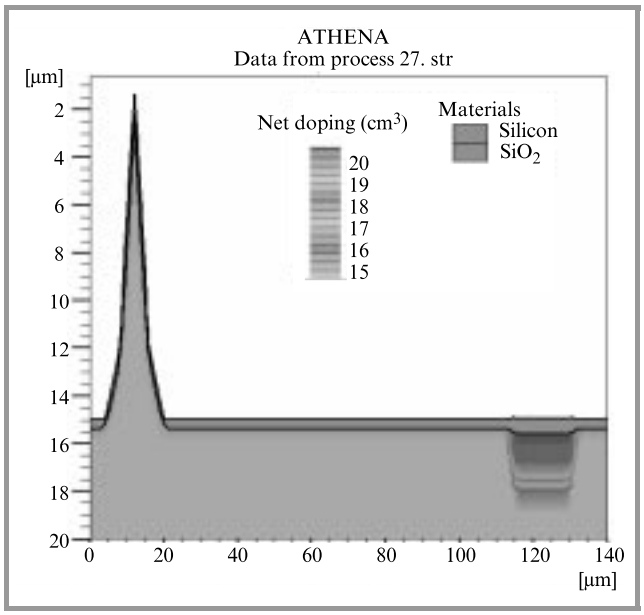


*Fig. 6.* Cross-sections of the piezoresistive cantilever – $n^+$ diffusion.

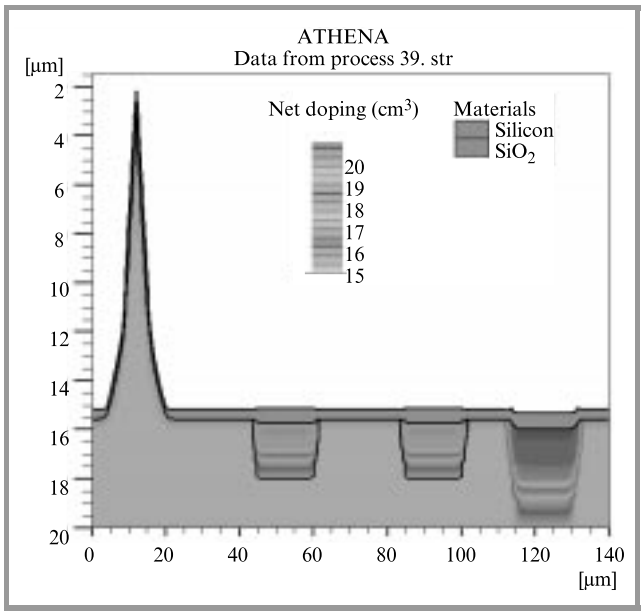


*Fig. 7.* Cross-sections of the piezoresistive cantilever – $p^+$ diffusion.

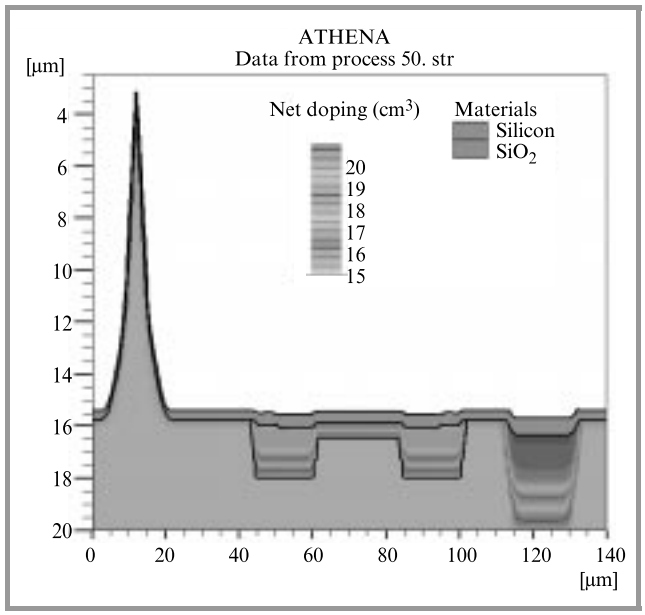


*Fig. 8.* Cross-sections of the piezoresistive cantilever – piezoresistors diffusion.

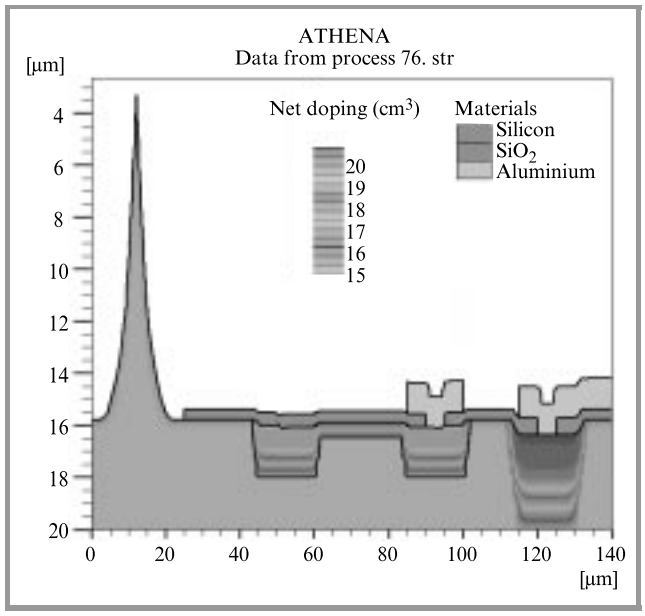


*Fig. 9.* Cross-sections of the piezoresistive cantilever – final structure.

and the energies of ion implantations. After these calculations we obtain the doping concentration distributions, junctions depths and the layers thicknesses in the final structure. Figures from 5 to 9 represent cross-sections of the piezoresistive AFM cantilever simulated by mean virtual wafer fab.

The output data of processes simulation establish the input data for ATLAS/SPISCES program. At the moment all the electrodes in the devices must be defined. Next, the input signals must be determined. After the simulation we obtain a solution which comprises not only device electrical characteristics but spatial distributions of variables like potential and current density as well.

The development of a new technological sequence is a very difficult task. The engineer must be familiar with many complicated physical phenomena, which are dependent on many input parameters.

## 4. Fabrication

The fabrication process is based on the double side silicon micromachining process. Double-side polished

<100>-oriented, $3 \div 7$ Ωcm silicon wafers were used as the starting material. Next, standard CMOS processing like oxidation, phosphorus and boron diffusion, ion implantation, dry and wet etching, insulator and aluminum film deposition and photolithography were sequentially applied to form $n^+$ and $p^+$ diffusion connecting paths, piezoresistors, contact windows and metallic connections. In the following – back side processing sequence a corner compensated membrane pattern was created by two-side photolithography process and anisotropic deep etching of silicon in 30% KOH solution at 60°C, to create 15 $\mu$m thick silicon membrane in the future beam area. Finally, the cantilever was defined in the membrane by last photolithography step at the top side of the wafer and silicon dry etching in $SF_6/CHF_3$/Ar plasma. 50 $\mu$m thick photoresist AZ4562 was used to mask piezoresistive circuit and the tip (Fig. 10).

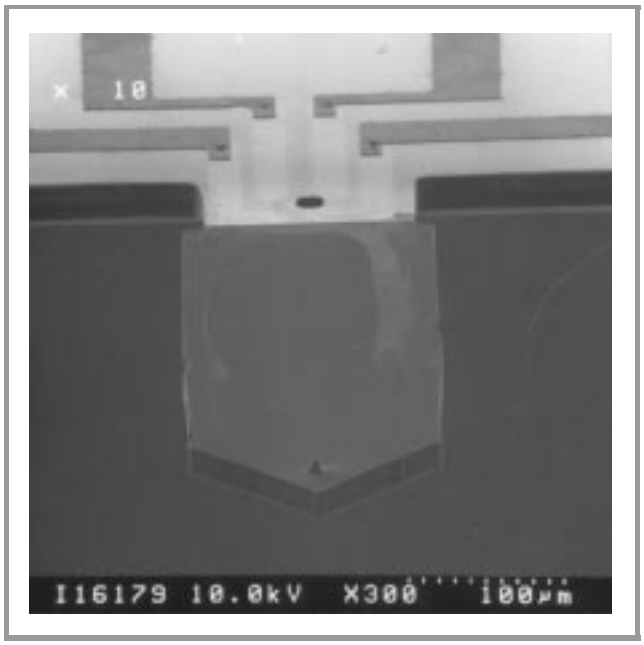


***Fig. 10.*** The SEM picture of the piezoresistive AFM cantilever.

## 5. Results and discussion

An important element in microelectronics is the comparison of modelling and the measurements results of the real semiconductor devices. Our paper describes the final results of the numerical simulation of the piezoresistive AFM cantilever process sequence and the experimental results. Silicon devices are prepared by performing a sequence of processing steps on a silicon wafer. VWF simulation of the atomic force microscopy sensors should optimize the device parameters, reduce the development time and cost. Programmes for the simulation of semiconductor devices allow to reduce cost of technological experiments. They give better understanding of the complex modern microelectronics. However engineers must be aware of software limitations. The necessity of good correlation of simulated and real data is particularly relevant. It is a very difficult problem, which can be solved only if sufficient knowledge is gathered.

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*Paper*

# On possibility to extend the operation temperature range of SOI sensors with polysilicon piezoresistors

Anatoly Druzhinin, Elena Lavitska, Inna Maryamova, Igor Kogut, and Yuri Khoverko

**Abstract — The aim of this work was to study the possibilities of developing mechanical sensors with poly-Si piezoresistors on insulating substrate for operation in different temperature ranges (low, elevated and high temperatures). Laser recrystallization is used as a technological tool to adjust the electrical and piezoresistive parameters of the polysilicon layer. For this purpose a set of studies including numerical simulation and experimental work has been carried out. The main three directions of the studies are considered: problems of thermal stabilization of the pressure sensor performance at elevated and high temperatures; problem of sensor operation at cryogenic temperatures; development of a multifunctional pressure-temperature sensor.**

***Keywords — SOI, mechanical sensors, poly-Si piezoresistor, ZMR.***

## 1. Introduction

Zone-melting recrystallization (ZMR) technique in its application to polysilicon-on-insulator structures represents a method of fabrication of relatively large areas of monocrystalline silicon [1]. The electrical properties of a laser-recrystallized SOI film on a slice surface may be controlled to a certain extent by a change of the parameters of laser treatment, the selection and corresponding preparation of the initial SOI structures, the choice of the scan direction for the laser beam; seeds, covering strips to control defect location in recrystallized poly-Si, etc. In order to improve performance of IC's and sensors fabricated on laser-recrystallized SOI structures the film layout should correspond to the layout of device active elements. This goal may be achieved using the lateral epitaxy; a method providing separate islands of recrystallized silicon film [2]. Since one can succeed in placing the active elements in the perfect material, this way is believed to be highly promising.

Investigations presented here were aimed to solve the following practical problems: development of high-temperature pressure sensors, study of possibilities to develop pressure sensors for operation at cryogenic temperatures and development of a two-functional pressure-temperature sensor.

Since laser recrystallization influences all the electrical and piezoresistive parameters of SOI layers prediction of the laser treatment results requires careful analysis of many factors and needs both theoretical simulation and experimental verification.

## 2. On the temperature invariance of piezoresistance in the climatic range and at elevated temperatures

Using the model [3] of boron-doped p-type polycrystalline silicon software has been developed to calculate electrical and piezoresistive properties of polysilicon layers numerically with the average grain size as a parameter. The main transport mechanism in polycrystalline poly-Si was suggested to be thermionic emission over the barriers at the grain boundaries combined with diffusion through the grain boundaries and the traditional carrier transport through the crystallites [4].

Figures 1 and 2 present the calculated temperature dependencies of resistivities of boron-doped poly-Si layers with grain size $L$ as a parameter. Figure 3 shows the measured $\Delta R/R_{20C}$ dependencies for the samples before and after laser recrystallization with two different initial carrier concentrations. Theoretical considerations show that laser recrystallization of poly-Si layers increases carrier concentration due to the enlargement of the average grain size, which results in the reduction of the total surface of grain boundaries, and due to trap passivation. Therefore, it changes the contributions of thermionic emission and diffusion in the carrier transport. On the other hand, the contribution of the grain boundaries themselves in the total resistivity of polycrystalline silicon strongly depends on the average

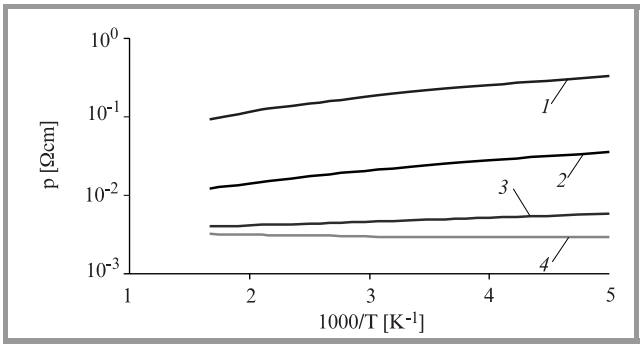


***Fig. 1.*** Calculated p-type poly-Si resistivity versus temperature for carrier concentration $N = 1.3 \cdot 10^{20}$ cm$^{-3}$ and the following values of the average grain size: *1* – 100 nm; *2* – 1 $\mu$m; *3* – 10 $\mu$m; *4* – 100 $\mu$m.

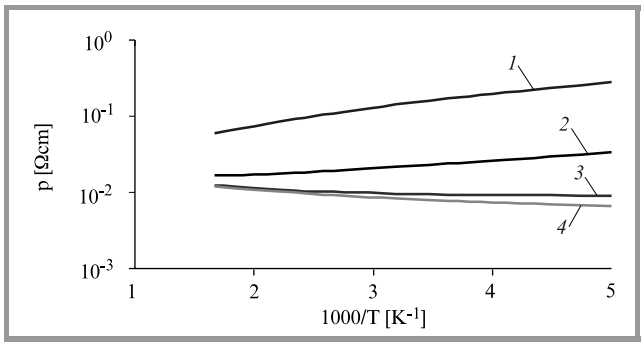


*Fig. 2.* Calculated p-type poly-Si resistivity versus temperature for carrier concentration $N = 3.2 \cdot 10^{19}$ cm$^{-3}$ and the following values of the average grain size: *1* – 100 nm; *2* – 1 $\mu$m; *3* – 10 $\mu$m; *4* – 100 $\mu$m.

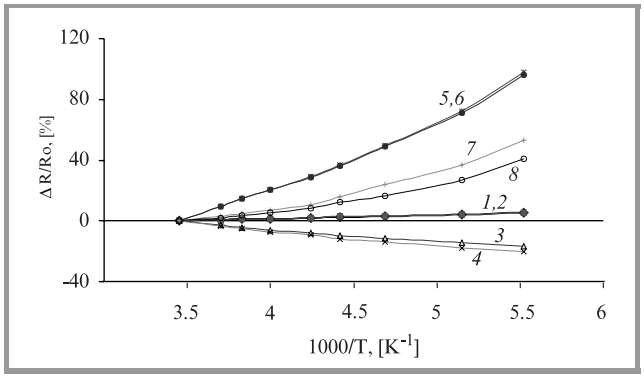


*Fig. 3.* Measured resistance versus temperature for the samples before *(1, 2, 5, 6)* and after laser recrystallization with two different initial carrier concentrations: *1, 2* – $3.9 \cdot 10^{19}$ cm$^{-3}$; *5, 6* – $2.4 \cdot 10^{19}$ cm$^{-3}$. The samples were parallel *(4, 8)* and perpendicular *(3, 7)* to the scan direction of the laser beam.

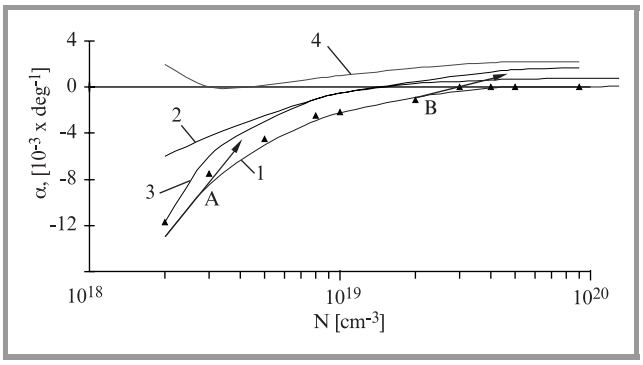


*Fig. 4.* Calculated TCR of poly-Si resistors near 20°C for *1* – $L$ = 120 nm and *2* – $L = 1\,\mu$m, compared with *3* – simulation and experimental data from [5] (triangles). Curve *4* corresponds to the data for bulk silicon.

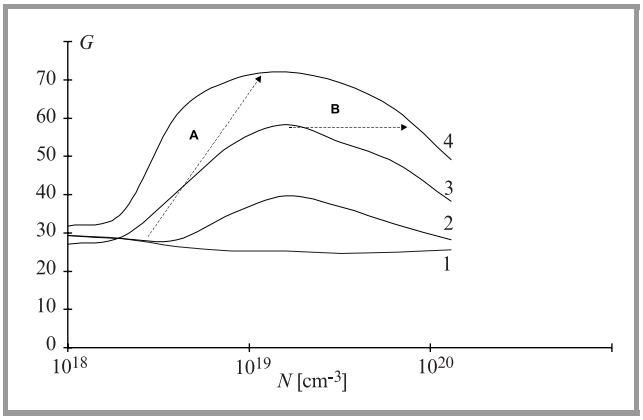


*Fig. 5.* Calculated longitudinal gauge factor in boron-doped polysilicon piezoresistors for the following values of average grain size: *1* – $L = 20$ nm; *2* – $L = 1\,\mu$m; *3* – $L = 10\,\mu$m; *4* – $L = 100\,\mu$m.

grain size $L$. After laser recrystallization the volume of the grains dominates in the electrical conductivity of polycrystalline material.

Figures 4 and 5 present calculated concentration dependencies of the temperature coefficient of resistance and longitudinal gauge factor for poly-Si piezoresistors with the average grain size $L$ as a parameter. The investigations demonstrate that the initial doping (boron) concentration in poly-Si piezoresistors to be used in mechanical sensors should be less than $1 \cdot 10^{19}$ cm$^{-3}$. In this case laser recrystallization leads to a rise of the longitudinal gauge factor and reduces the temperature coefficient of resistance (TCR) of poly-Si piezoresistors [1]. Arrows **A** and **B** in Figs. 4 and 5 show the two possible consequences of laser ZMR action on poly-Si piezoresistors: arrow **A** shows the most desirable result when after recrystallization the gauge factor increases and TCR decreases, while arrow **B** corresponds to the situation where neither sensitivity nor thermal stability is improved.

There are two important coefficients which define the temperature dependence of the piezoresistor output signal: temperature coefficient of the gauge factor (TCGF) $\alpha_G$ and temperature coefficient of resistance (TCR) $\alpha_R$. These coefficients are defined by the following formulae:

$$\alpha_G(T) = \frac{1}{G(T)} \frac{\partial G(T)}{\partial T}, \tag{1}$$

$$\alpha_R(T) = \frac{1}{R(T)} \frac{\partial R(T)}{\partial T}. \tag{2}$$

If the condition $\alpha_G + \alpha_R \approx 0$ is satisfied over a certain temperature range in the sensor measuring bridge supplied by the current source, then it is possible to achieve self-compensation of the temperature dependence of the sensor output. In this case the decrease of the sensor output due to the gauge factor reduction with temperature is compensated by the output rise due to the increase of the piezoresistor's resistance. The conditions required to achieve such a situation are explained by Figs. 4 and 5 where calculated temperature coefficient of resistance and gauge factor of boron-doped poly-Si piezoresistors are plotted as functions of carrier concentration and average grain size.

Some theoretical predictions concerning the temperature-dependence of the characteristics were made. On the basis of the studies two regions of the doping concentration were recommended where the temperature invariance of piezoresistance is achievable:

- Non-recrystallized poly-Si layers with $N \approx (5 \div 8) \cdot 10^{19}$ cm$^{-3}$; for these layers TCGF is small and negative whilst TCR is small and positive.
- Moderately doped poly-Si layers with impurity concentration in the initial samples $N \approx (2 \div 3) \cdot 10^{18}$ cm$^{-3}$; appropriate choice of the recrystallization regime provides positive TCR in the layers with enlarged grain size and similar values of TCGF but with the opposite sign. Both coefficients are higher than in the previous case. Besides temperature stability laser recrystallization provides increases the gauge factor of the samples. That is why this concentration region combined with the laser treatment is recommended for the development of the mechanical sensors with improved sensitivity.

## 3. Low-temperature region

At cryogenic temperatures, when a significant freezing of the carriers is expected, one should consider an alternative carrier transport mechanism: quantum transport by the states at grain boundaries (GB). The difference in the barrier heights at GBs results in a random potential relief due to the energy band bending near the GBs. That is why this system may be considered as a heavily doped and strongly compensated semiconductor where the boundary states play a role of compensating impurities [6].

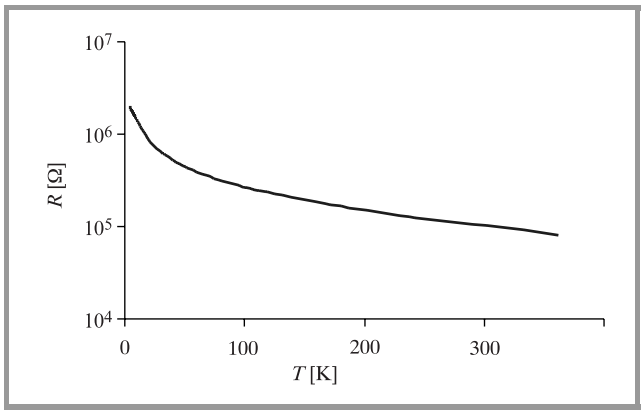


***Fig. 6.*** Low-temperature resistance of non-recrystallized poly-Si resistor with $N = 2.4 \cdot 10^{18}$ cm$^{-3}$.

In order to study the feasibility of using poly-Si resistors at cryogenic temperatures with ZMR as a method to improve their parameters the resistance of poly-Si samples presented in Fig. 3 was measured as a function of temperature in the range of $4.2 \div 300$ K. Figures 6 and 7

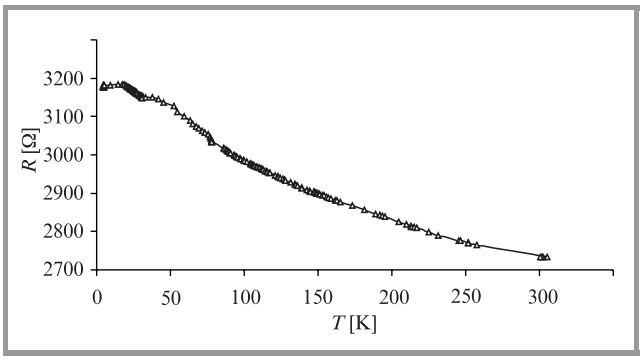


***Fig. 7.*** Low-temperature resistance of non-recrystallized poly-Si resistor with $N = 3.9 \cdot 10^{19}$ cm$^{-3}$.

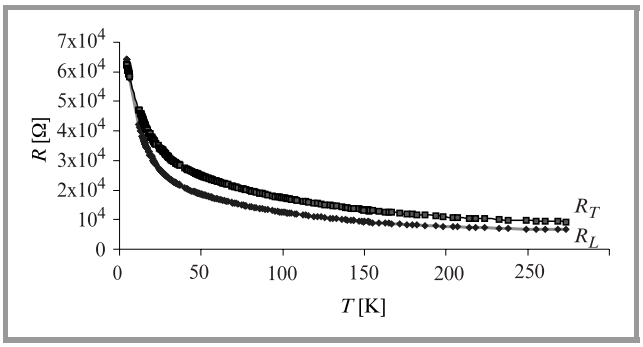


***Fig. 8.*** Low-temperature resistance of recrystallized poly-Si resistors with $N = 4.8 \cdot 10^{18}$ cm$^{-3}$. $R_T$ and $R_L$ represent transversal and longitudinal resistance as related to the laser scan direction.

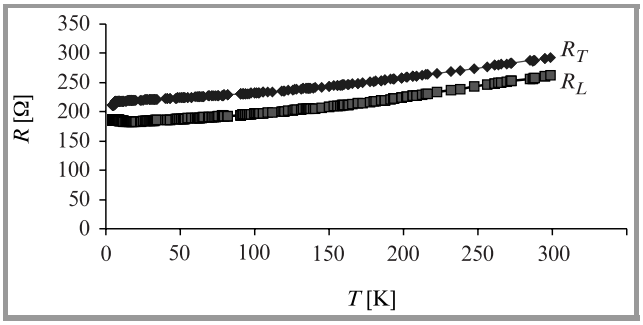


***Fig. 9.*** Low-temperature resistance of recrystallized poly-Si resistors with $N = 1.7 \cdot 10^{20}$ cm$^{-3}$. $R_T$ and $R_L$ represent transversal and longitudinal resistance as related to the laser scan direction.

show resistance-versus-temperature dependencies in non-recrystallized samples, while Figs. 8 and 9 present these dependencies for laser-recrystallized samples. The analysis of the experimental results proves that for moderately doped samples (Figs. 6 and 7) at relatively high temperatures $200 \div 300$ K there is a traditional carrier drift through the crystallite volume combined with thermionic emission at the grain boundaries while at cryogenic temperatures the electrical conductivity is due to the carrier transport along the grain boundaries that could be described in terms of percolation theory [6]. Moderately doped non-recrystallized

poly-Si has a strong temperature coefficient of resistance (Fig. 6) and could be recommended to be used as a thermoresistor in a wide temperature range. Other samples (Figs. $7 \div 9$) show a reasonable change of the resistance in the range $4.2 \div 300$ K. This result combined with theoretical assessment of their piezoresistive properties [1] let us expect that it is possible to use them as piezoresistive elements at cryogenic temperatures.

## 4. Development of a microelectronic pressure-temperature sensor

The problem of the development of multifunctional sensors simultaneous measurement of several parameters, mechanical and thermal in particular, is a task for different branches of science and engineering. The IC fabrication process on SOI substrates seems particularly prospective for manufacturing these sensors.

The investigation indicates that in the case of the most thermally stable poly-Si layers with the initial boron density $\approx (2 \div 5) \cdot 10^{18}$ cm$^{-3}$ laser recrystallization using the technique developed for such SOI-structures results in the change of resistance within the limits of 1% (Fig. 10) in the range of $+20 \ldots 140$°C. The studies of the temperature characteristics of poly-Si-on-insulator layers show that the strongest temperature dependence of resistivity for non-recrystallized, i.e. fine-grained, poly-Si layers is found for the doping density of $\approx 2.4 \cdot 10^{18}$ cm$^{-3}$ (Fig. 10).

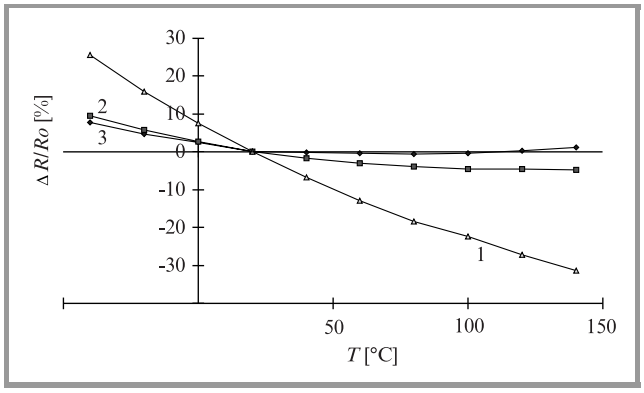


***Fig. 10.*** Relative change of resistance versus temperature for the sample with $N = 2.4 \cdot 10^{18}$ cm$^{-3}$ before *(1)* and after *(2, 3)* laser recrystallization in longitudinal *(2)* and transversal *(3)* direction as related to the scan direction.

The experimental data enabled a concept of the multifunction microelectronic sensor for the pressure-temperature measurement to be developed. It is proposed that non-recrystallized poly-Si layers with boron concentration $\approx 2.4 \cdot 10^{18}$ cm$^{-3}$ be used as thermoresistors for temperature measurements. As far as pressure measurements are concerned it is proposed that piezoresistors based on laser-recrystallized poly-Si layers with initial boron concentration $\approx 2 \cdot 10^{18}$ cm$^{-3}$ ($4.8 \cdot 10^{18}$ cm$^{-3}$ after the laser recrystallization) be used. These piezoresistors have sufficiently high gauge factor and show reasonable thermal stability over a wide temperature range.

A layout of such microelectronic pressure-temperature sensors has been developed. According to this layout (Fig. 11) SOI-based piezoresistors $R_1 \div R_4$ connected to form a bridge circuit were placed on a micromachined membrane while the thermoresistor $R_5$ was fabricated of appropriately doped poly-Si. The thermoresistor is on the same chip but not on the membrane. Thus it is insensitive to the mechanical stress in the membrane under external pressure.

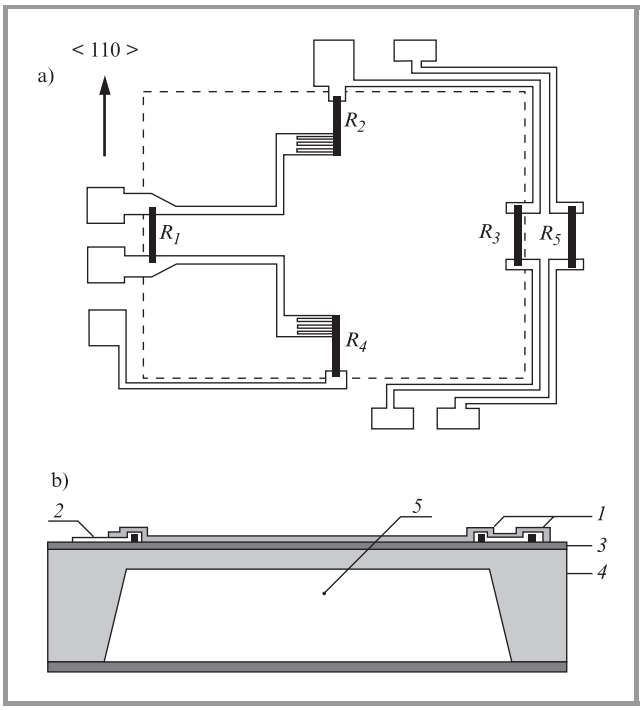


***Fig. 11.*** Layout (a) and design (b) of SOI pressure-temperature sensor: $R_1 \div R_4$ – poly-Si piezoresistors; $R_5$ – poly-Si thermoresistor; *1* – poly-Si resistors; *2* – Al contacts; *3* – $SiO_2$ layer; *4* – Si wafer; *5* – Si membrane.

The fabrication process of the microelectronic pressure-temperature sensor was based on the fabrication process of microelectronic pressure sensors with laser-recrystallized polysilicon piezoresistors [7]. Because the polysilicon piezoresistors and thermoresistor in the multifunctional sensor have the same initial boron concentration ($\approx 2.4 \cdot 10^{18}$ cm$^{-3}$), doping of these resistors does not require any additional technological operation. Doping of poly-Si layers was carried out by the ion implantation method. During laser recrystallization of poly-Si piezoresistors the poly-Si thermoresistor was protected by $Si_3N_4/SiO_2$ film with the thickness sufficient to provide absorption of laser irradiation.

Using the developed technology the experimental sensors have been fabricated for different pressure and temperature ranges:

1. pressure $0 \div 2.4 \cdot 10^5$ Pa ($0 \div 2.5$ bar), temperature $20 \div +150$°C;

2. pressure $0 \div 1.6 \cdot 10^5$ Pa ($0 \div 1.6$ bar), temperature $-40 \div +60$°C.

The performance of the multifunction sensors is presented in Figs. 12 and 13. Temperature coefficient of resistance of the developed temperature sensor is $-0.386\% \cdot \deg^{-1}$.

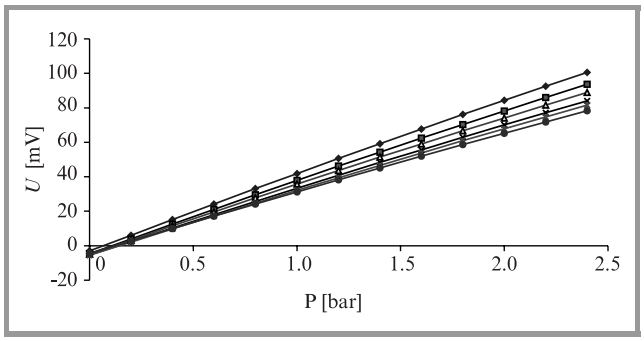


***Fig. 12.*** Pressure-dependent output signal of the multifunctional sensor at several temperature points.

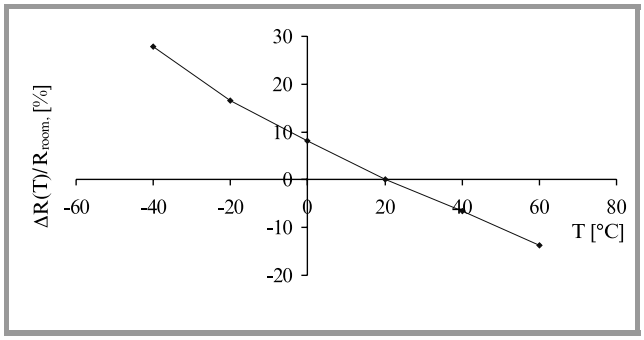


***Fig. 13.*** Output performance of the thermoresistor of multifunctional sensor.

The chips size is 5 mm × 5 mm, while membrane size is 2 mm × 2 mm. For certain applications, especially in medicine, the size of the chip could be significantly reduced.

The advantages of pressure-temperature sensors based on poly-Si resistors are a simple and reproducible fabrication process and adjustability of the temperature coefficient by appropriate choice of doping concentration and laser recrystallization regime. The developed multifunctional sensors may be applied in different branches of industry, science and medicine.

## 5. Conclusions

Our studies reveal that:

- poly-Si piezoresistors exhibit regions of thermal stability at climatic and elevated temperatures;
- these piezoresistors may be used at cryogenic temperatures.

In both cases laser recrystallization represents a method to tailor the parameters of poly-Si piezoresistors to the desired temperature range.

Multifunction pressure-temperature sensors have been developed as an application of the results of the studies performed.

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Paper

# Grain boundary effect on the anisotropy piezoresistance of laser-recrystallized polysilicon layers in SOI-structures

Yury Pankov and Anatoly Druzhinin

**Abstract — A physical model of grain boundary influence on the piezoresistive effect of p-type conductivity of polysilicon layers in SOI-structures is developed. Software calculating piezoresistive properties of boron-doped p-type polysilicon layers has been developed. These properties may be calculated over wide concentration and temperature ranges with anisotropy taken into account and with the average grain size as a parameter. The potential barrier regions around the grain boundaries influence the deformation changes of anisotropy resistance in the fine-grained non-recrystallized SOI-structures doped with boron up to $3 \cdot 10^{19}$cm$^{-3}$ only.**

*Keywords — SOI, polysilicon layers, MLR.*

## 1. Introduction

The increasing requirements imposed on polycrystalline silicon films, which are suitable for fabrication of low-cost MEMS-sensors, stimulate studies aimed to improve the properties of polysilicon. A possible way to obtain high-quality poly-Si layers is the microzone laser recrystallization (MLR), a process used in the fabrication of SOI-structures. MLR changes the microstructure of poly-Si layers modifying their piezoresistive properties. Thus microzone laser recrystallization of poly-Si layers is a prospective way to obtain high-quality SOI-structures. This method allows poly-Si films with predetermined orientation to be melted locally. Moreover, crystallite growth and defect formation may be controlled. Finally, the method affects the structure and other parameters of the semiconductor.

The appearance of anisotropy in electrical conductivity is the primary effect of anisotropy strain action and scalar component of resistance remains nearly constant. This is the result of Smith's classical investigations of single-crystal bulk silicon [1]. Previous well-known investigations of piezoresistance in both n- and p-type polycrystalline polysilicon consider longitudinal and transverse gauge factors under uniaxial stress [1, 2]. But these parameters do not describe the behavior of microelectronics sensors adequately. Scalar isotropy resistance changes, which are averaged in all directions, are given by

$$\Delta r = 1/3\,\mathrm{Sp}\boldsymbol{r} = 1/3 \sum_{i,k=1}^{3} \Delta r_{ik} \,. \qquad (1)$$

The fully symmetrical current bridge circuit compensates the total isotropy resistance. This compensation is a result of the temperature change of resistance compensation without stress (an additive temperature error). It has been shown that in conditions of optimum tenzoresistors location the output signal of piezoresistive microelectronic sensor is proportional to the maximum anisotropy resistivity

$$U_{out} \sim i_p \max \left( r_{ik} - 1/3 \sum_{i,k=1}^{3} r_{ik} \right) , \qquad (2)$$

where $i_p$ is the current bridge power supply.
Therefore, the resistance anisotropy

$$\mathrm{Dev}\boldsymbol{r} = r - 1/3\mathrm{Sp}\boldsymbol{r} = r_{ik} - 1/3 \sum_{i,k=1}^{3} r_{ik} \qquad (3)$$

is the fundamental parameter in MEMS-sensors. This conclusion opens the possibility to reduce negative influence of grain boundaries on sensor characteristics by means of laser recrystallization of the SOI-structures.

## 2. Theory

The aim of our studies was to investigate the electrical conductivity anisotropy, changes of carrier mobility and hole effective mass under general strain of boron-doped polysilicon-on-insulator patterns both before and after the laser recrystallization. This model considers the contribution to both anisotropy and isotropy piezoresistance from the grain and the isotropy Schottky-type barrier regions around the grain boundaries.

Polysilicon consists of small single-crystalline (grains), which have point symmetry of the cubic group $O_h$. Single crystals are separated by non-crystalline regions with isotropy symmetry SO(3). Broken bonds on the grain boundaries form the so-called traps, which capture charge carriers. As a result of trapping, boundary areas depleted of carriers are created on both sides of the grain boundaries. Thus, the crystalline structure of a polycrystalline semiconductor is characterized by the isotropy and the energy structure is characterized by the presence of potential barriers at the grain boundaries.

The theoretical analysis of piezoresistive characterization of poly-Si layers is based on the consideration of the resistivity tensor of both the bulk silicon and the barrier regions. The carrier transport through the potential barrier is supposed to be due to the thermionic emission combined with diffusion. Let's extend the well-known model of the polysilicon piezoresistance for the total case of arbitrary strains and total resistance changes. In the limit of small voltages, the barrier can be modelled by anisotropy linear resistors. Thus, the total anisotropy resistivity $\rho$ can be written in terms of an anisotropy grain and approximate isotropy barrier resistivity $\rho_g$ and $\rho_b$ by

$$\rho_{ik}(\varepsilon, T) = \rho_{g,ik}\left[1 - \frac{2W+\delta}{L}\right] + \rho_b \frac{2W+\delta}{L}\,\delta_{ik}\,, \qquad (4)$$

where $W$ is width of the carrier-depleted zones formed on both sides of the grain boundary, $\delta$ is the grain boundary thickness, $L$ is the grain size and $\delta_{ik}$ is the Kronecker delta. This equation can be concluded by the consideration of total resistivity tensor in major axes.

For the thermionic emission-diffusion theory the total isotropy conductivity from both heavy and light holes in p-type material is given by [2]

$$\sigma_b \sim \sum_{l=1}^{2} B_l \exp\left(-E_f/kT\right)\exp\left(-qV_b/kT\right)\,, \qquad (5)$$

where $E_f$ is the Fermi energy, and

$$V_b = V_{bo}\left(1+\zeta T\right)\,,\ \ \zeta \approx 1.5\cdot 10^{-3}K^{-1} \qquad (6)$$

is the temperature-depending height of the potential barrier at the grain boundary and factor $B_l$ is defined by the effective mass of holes in $l$-th sub-zone $m_l$ and the relaxation time $\tau_l$:

$$B_l(\varepsilon, T) = m_l / \left[1 + \left(2m_l kT / \pi q^2 \xi^2 \tau_l\right)^{1/2}\right]\,, \qquad (7)$$

where $\xi$ is the dielectric permitivity.

## 3. Results and discussion

Details of the complicated valence band structure of silicon were taken into consideration. A special method was developed for piezoresistance calculations in the grain volume that allowed both the main effect due to the carriers redistribution between the sub-bands and a significant effect on the magnitude because of change in warpage of the constant energy surfaces in strained silicon to be estimated. In the case of p-type semiconductors the anisotropy strain splits initially degenerate parabolic valence band, but essential non-parabolic effects appear in their energy spectrum under this kind of the strain. Therefore, effective masses of holes essentially depend on the energy and anisotropy strain. Details of the complicated valence band structure in strained silicon were taken into consideration [4]. Carrier concentration in semiconductor with arbitrary energy spectrum is given by

$$n = \frac{1}{4\pi^3}\int f(E)\,dk^3 = \int_{S_E} f(E)\,g(E)\,dE\,. \qquad (8)$$

From this expression it follows that the density of states in the strained semiconductor with any given energy spectrum is given by the following total definition: Lebesgue measure, originating from the energy surface averaging of volume element $dk^3$:

$$dE = <\left(dk^3\right)> = \frac{dE}{4\pi^3}\int_{S_E} \mathrm{Det}\left(\mathbf{J}_l^{-1}\right) dS_E\,, \qquad (9)$$

where $\mathbf{J}_l$ is the Jacobi matrix of transformation to arbitrary coordinates $(E, \zeta_1, \zeta_2) \to (k_1, k_2, k_3)$, which are associated with constant energy surfaces $S_E : dS_E = d\zeta_1\, d\zeta_2$.

In the semiconductor with isotropic and parabolic zone states density is defined by

$$g(E) = (2m)^{3/2}E^{1/2}/\left(2\pi^2\hbar^3\right)\,. \qquad (10)$$

From this relation it follows that the effective masses in strained p-type semiconductor may be given as [4]:

$$m_{dl}(E, \varepsilon) = \frac{\pi^{2/3}\hbar^2}{2^{5/3}E^{1/3}}\int_{S_E} \mathrm{Det}\left(\mathbf{J}_l^{-1}\right) dS_E\,. \qquad (11)$$

In our calculation the modified energy Bir spectrum of valence zone was used [4, 5]. Calculated effective masses of holes are shown in Fig. 1 for uniaxial stressed p-type Si.

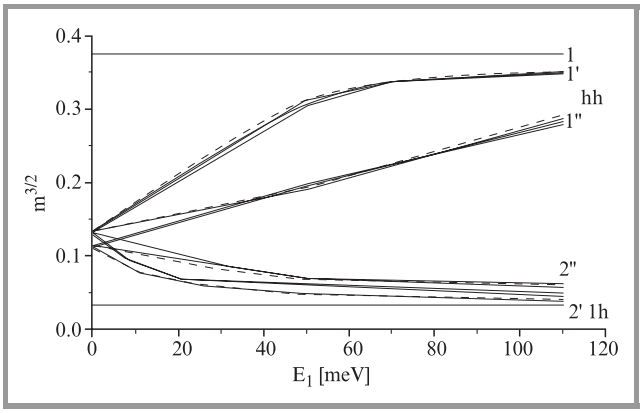


***Fig. 1.*** Hole effective masses of uniaxial stressed Si: 1, 1', 1" – heavy holes, 2,2',2" – light holes; under the strain: $1,2 - \varepsilon = 0, 1', 2' - \varepsilon = 0.4\%, 1'', 2'' - \varepsilon = 1.2\%$. Dashed lines represent compression and solid ones tension.

Fermi energy and relaxation time changes, which belong to Eq. (7), were computed through solving the electroneutrality equation for the real strain energy spectrum [4]. The strain dependence of the relaxation time is revealed through the strain dependence of effective masses. Changes of Fermi energy versus uniaxial strain are shown in Fig. 2.

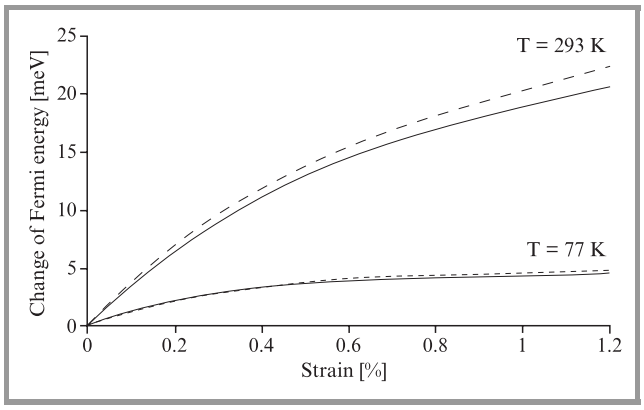


***Fig. 2.*** Changes of Fermi energy versus uniaxial strain. Dashed lines represent compression and solid ones tension.

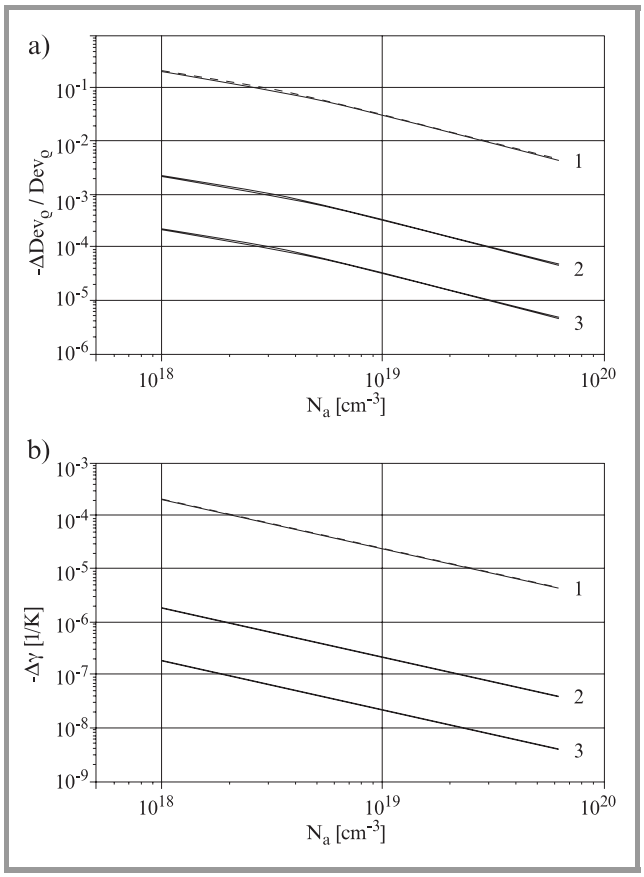


***Fig. 3.*** Relative changes of strain anisotropy resistivity versus the doping concentration after taking into account the grain boundary effects (a) and changes of its temperature coefficient for average grain size: $1 - L = 0.1\,\mu$m, $2 - L = 10\,\mu$m, $3 - L = 100\,\mu$m (b). Dashed lines correspond to situation before whereas solid ones – after laser recrystallization.

According to selection rules of strain effect tensors in cubic semiconductor [6], the total conductivity/resistivity tensor cannot have a linear term relative to anisotropy strain. As a result the strain dependence of effective masses could only increase nonlinearity of SOI-sensor output characteristics. Numerical calculations of the anisotropy resistivity tensor (as a function of boron doping concentration) were made for different types of practically interesting patterns: initial ones with the average grain size $L \sim 0.1\,\mu$m; after laser recrystallization with a chevron-like structure and $L \sim 10\,\mu$m; and after laser recrystallization with lateral seed region ($L \sim 100\,\mu$m). The carrier energy $E \approx E_T = = 3/2kT$ was estimated through calculations. In Fig. 3a the corresponding results are presented for the calculated changes of maximum strain anisotropy resistivity after taking into account potential barrier at the grain boundary and in Fig. 3b – changes of its temperature coefficient are shown.

The results of calculations demonstrate that potential barrier regions around the grain boundaries influence the deformation changes of anisotropy resistance in the fine-grained non-recrystallized boron-doped SOI-structures with boron concentration less than $3 \cdot 10^{19}$ cm$^{-3}$. This is in good agreement with the results of measurements of all the components of elastoresistance tensor in laser-recrystallized polysilicon layers. A set of theoretical and experimental investigations was curried out to reveal the possibilities of SOI-structures in microelectronic piezoresistive mechanical sensors [7].

## 4. Conclusion

After laser recrystallization the grain bulk dominates in the specific strain resistance of polycrystalline material. Thus this recrystallization enables negative influence of grain boundaries on piezoresistive sensor characteristics of the SOI-structures to be reduced.

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**Anatoly Druzhinin** – for biography, see this issue, p. 44.

Paper

# Fabrication and properties of the field emission array with self-alignment gate electrode

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**Abstract — A new method for the fabrication of field emission arrays (FEA) based on bulk/surface silicon micromachining and diamond-like-carbon (DLC) coating was developed. A matrix of self-aligned electron field emitters is formed in silicon by mean anisotropic etching in alkali solution of the front silicon film through micro holes opened in silicon oxide layer. The field emission of the fabricated emitter tips is enhanced by a diamond-like-carbon film formed by chemical vapor deposition on the microtips. Back side contacts are formed by metal patterning. Detailed Raman, Auger and TEM investigations of the deposited DLC films (nanocrystalline diamond smaller than 10 nm) will be presented. In this paper we discuss the problems related to the development of field emission arrays technology. We also demonstrate examples of devices fabricated according to those technologies.**

***Keywords — field emission array, field emission display, diamond-like-carbon layers emission, silicon micromachining, self- alignment technology.***

## 1. Introduction

The most characteristic feature of today electronic market is a very strong development of portable equipment sector. The demand for pocket systems as games, cellular phones, palm-top computers and advanced measurements systems increases remarkably. All this application require low power consumption and new visualization systems. Standard LCD technology however, which dominates in production of the integrated circuits and systems, has some serious limitations. The most promising solution of this fundamental problem seems to be employment of the field emission display (FED). FED is one of the principal candidates for future flat screen displays. Its key attraction is the ability to deliver high quality (in terms of brightness, colour, viewing angle) images with relatively low power consumption.

Investigations on the new materials with negative electron affinity and new technologies allowed to build field emitters which can be operated at low voltage and in very poor vacuum with very high current density. Costs and the device performance are the most important issues influencing the industrial applicability of the FE-arrays (FEA) devices.

## 2. Theory

In typical solutions, single emitter cells consist of a microtip located in a hollow, with the tip apex surrounded by a gate electrode (Fig. 1). The electron emission current ($I$) from the tip describe Fowler-Nordheim relation:

$$\frac{I}{V^2} = \frac{\alpha a \beta^2}{\phi} \exp\left(\frac{-\mathrm{b}\phi^{\frac{3}{2}}}{\beta V}\right), \quad E = \beta \cdot V,$$

where: $\phi$ – work function, $\beta$ – enhancement factor, $a$ – emission area, $E$ – electric field strength, $V$ – voltage, $I$ – emission current, $\alpha$, b – constants.

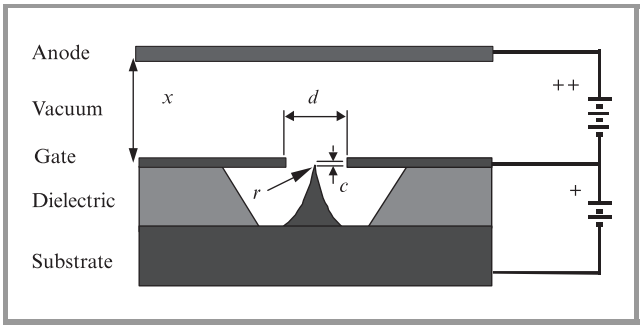


***Fig. 1.*** Typical single field emitter cell.

The enhancement factor ($\beta$) depends strongly on the tip radius ($r$) and on the gate opening diameter ($d$). The processing sequence has to be optimized to obtain very sharp tip, small diameter of the gate opening and very good uniformity of the structure geometry. A good alignment of the tip due to the gate opening is particularly important.

## 3. Fabrication

The micromachining fabrication process was based on a sequence of deposition, lithography, and dry/wet etching processes. Double side polished, <100> oriented, $4 \div 5$ Ωcm n-type silicon wafers were used as a starting material. First, the bottom, 400 nm thermal silicon oxide layer was created, then low stress $0.5 \div 1.0$ $\mu$m $SiO_xN_y$ film was deposited using PECVD technique. The emitter shape was defined in first lithography step. The tip location and the central gate opening are formed in the same lithography step,

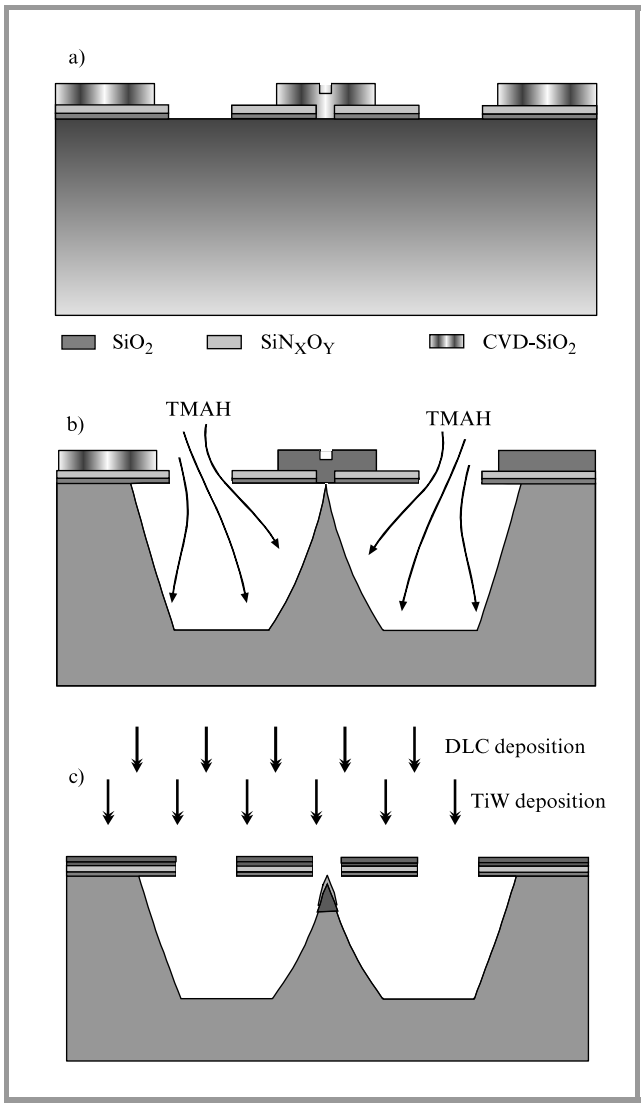


***Fig. 2.*** Field emitter array cell fabrication by silicon micromachining; (a) ÷ (c) explanation in the text.

thus ensuring perfect self-alignment of the gate and the tip (Fig. 2a).

Low stress silicon oxide layer was deposited and in a second lithography step to enable access to silicon surface. A matrix of self-aligned electron field emitters is formed in silicon by mean anisotropic etching in alkali solution of the front silicon film through micro holes opened in silicon oxide layer (Fig. 2b). Then was deposited TiW metal film by means of magnetron sputtering technique followed by CVD DLC film deposition (Fig. 2c). This double layer coating provides a conductive gate electrode. The DLC film was also deposited at the apex of the tip.

## 4. Results and discussion

Figures 3 and 4 show the SEM microscopy photographs of the fabricated emitter arrays.

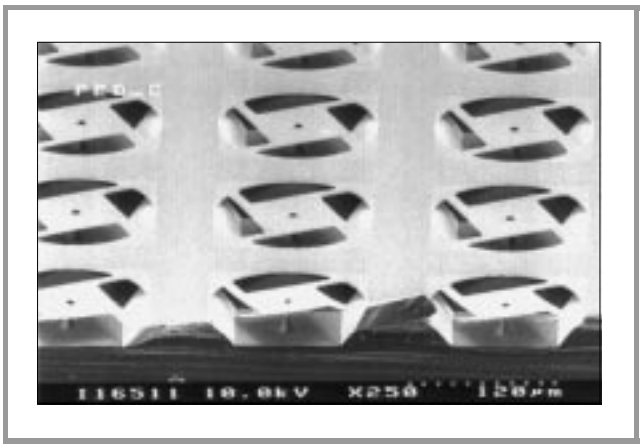

***Fig. 3.*** Field emitter array fabricated using silicon micromachining technique.

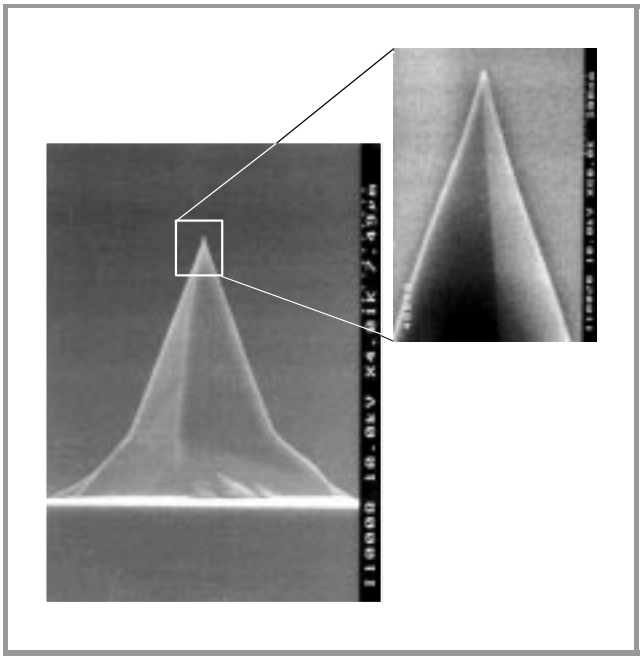

***Fig. 4.*** SEM photographs of the silicon tip with apex region enlarged. Visible very good sharpness of the tip.

Uniformity of the fabricated microtips was very good. The tips were sharp, with curvature radius below 50 nm. Additional sharpening by means of thermal oxidation yields a tips with radius in the range of 20 nm or better. Emission performance of the fabricated tip array was estimate by measuring the emission current for samples $10 \times 10$ mm big with 2800 tips.

Experimental results of the field emission measurements regarding F-N behavior and long term stability of the electron current for the different emitter structures including unique characteristics of uncoated and DLC coated silicon tips will be presented and discussed.

### *4.1. Characterization of the TEM microscopy*

We have used a Philips CM200 STA with $LaB_6$- cathode and CCD- camera (with resolution $1024 \times 1024$ pixel), 200 kV acceleration voltage, condenser aperture 100 $\mu$m, objective aperture 50 $\mu$m. The TEM investigations do not show the presence of nanocrystallites below 10 nm (Fig. 5).

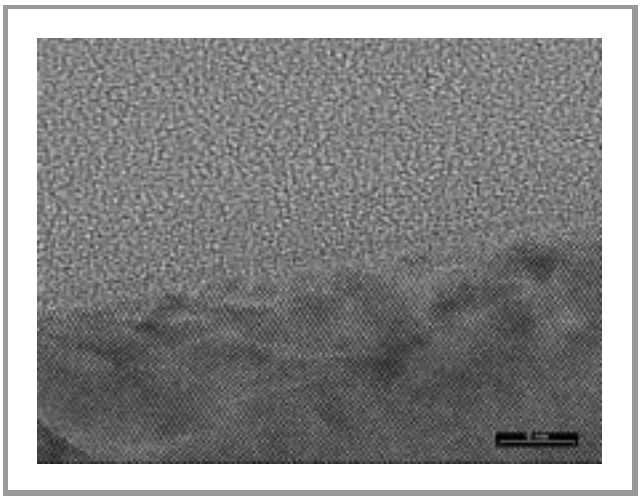

***Fig. 5.*** TEM analysis – nanocrystalites below 10 nm could not be seen.

### *4.2. Characterization of the Raman spectra*

Basic structural investigations of the carbon DLC were done by micro-Raman spectroscopy. The Raman spectroscopy proved the presence for the nanocrystallites. The Raman spectrum of DLC layer (Fig. 6) shows a sharp peak at about 1340 $cm^{-1}$ which is usually referred to as diamond peak. The second peak emerges at 1600 $cm^{-1}$ and is referred to as graphite peak. Given the relative sensitivities of the Raman technique to diamond and graphite at the wavelength used, it can be estimated that the film contains a few percent

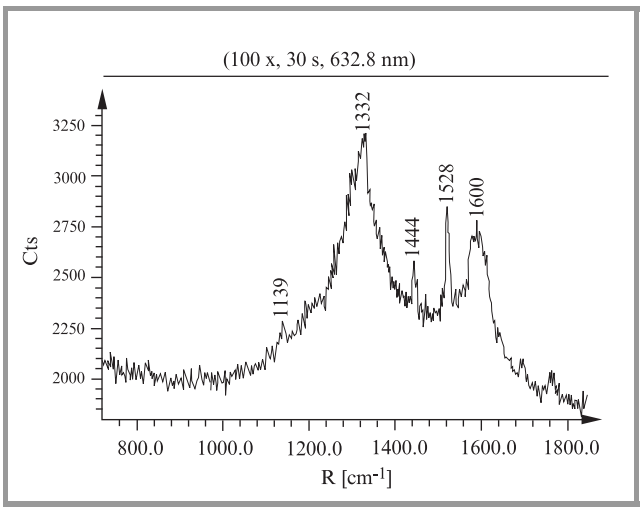


***Fig. 6.*** Raman spectra of the DLC film deposited on the FE-sources.

graphite. The full width at half-maximum of the 1332 $cm^{-1}$ peak can be attributed to a very small grain size (below 10 nm) of the diamond nanocrystals.

### *4.3. Measurements*

The emitter array sample was placed in a vacuum chamber. The chamber was pumped down below $1 \cdot 10^{-6}$ Torr. Next, the I-V characteristics were measured using 610C Keithley electrometer. Two types of arrays were evaluated, coated with DLC film and silicon structures without DLC coating. Results of the measurements are shown in Fig. 7. The relatively low threshold voltage equal to 150 V was observed

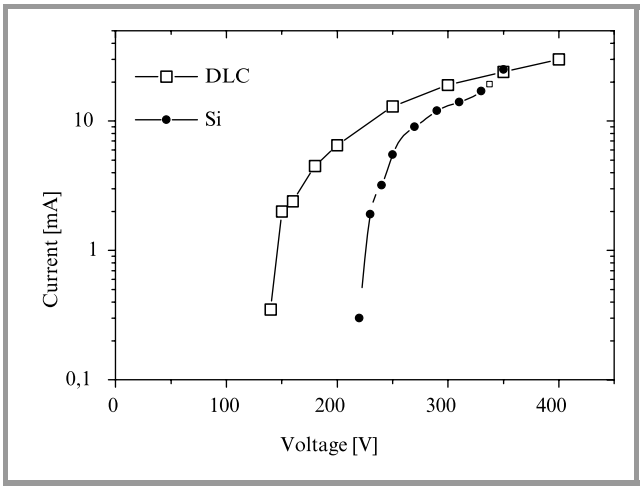


***Fig. 7.*** F-N characteristics of the coated and uncoated silicon emitter arrays.

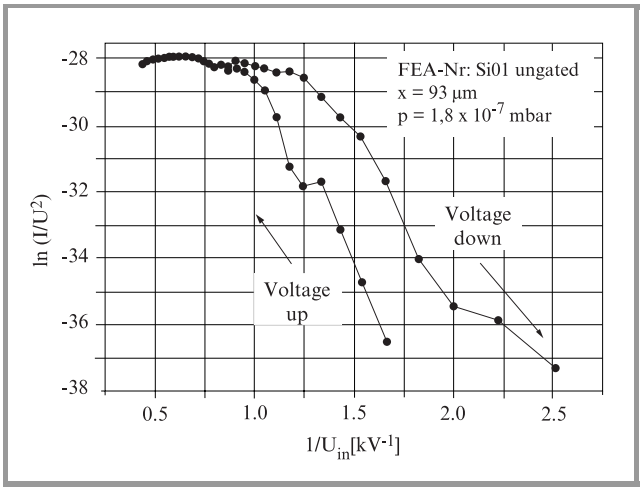


***Fig. 8.*** The hysteresis of the F-N plot was observed (ion sputtering of the tip).

for DLC coated tips, while for uncoated Si tips threshold above 200 V was noted. The maximum current 11 $\mu$A per tip was measured for DLC coated structures, while for uncoated Si tips the maximum current was 9 $\mu$A per tip. It is evident that the DLC coating has a considerable influence

on the emission efficiency. A hysteresis of the F-N plot was observed most probably due to ion sputtering of the tip (Fig. 8).

## 5. Summary

A new silicon micromachining method for fabrication of field emission arrays was developed. The process is simple and allows for self-aligned gate electrode formation. The DLC coated silicon tip array was fabricated using the developed technique. The developed technology could be useful for a production very wide range of field emitter arrays applications such as flat panel displays, high frequency devices, field emission electron guns, field emission cathodes, low energy electron microscope, field emission diodes and field emission triodes. Further investigation of the work function and long time emission stability of the emitter arrays has to be performed.

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**Andrzej Jakubowski** – for biography, see this issue, p. 33.

**Wolfgang Barth, Tomasz Dębski** – for biography, see this issue, p. 38.

Paper

# Adsorption properties of porous silicon

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**Abstract — Porous silicon shows some interesting features for micromechanical applications. Some applications make use of its high surface-to-volume ratio. A capacitive gas or humidity sensor using the adsorption of gases on the porous surface can be easily fabricated. However an opportunity for more sensitive device is given by micromechanical structure. In this paper we report on the piezoresistive cantilever beam structure with porous silicon adsorbing spot as a gas sensor.**

***Keywords — porous silicon, cantilever beam, gas sensor.***

## 1. Introduction - idea of the gas sensing microprobe

Both thermal heating and variations in relative humidity can significantly influence the deflection of a cantilever microbeam. Chemical sensor can be based on the detection of gas adsorption by monitoring the bending or resonance frequency shift of a cantilever beam [1]. The idea of the considered sensor structure is shown schematically in Fig. 1.

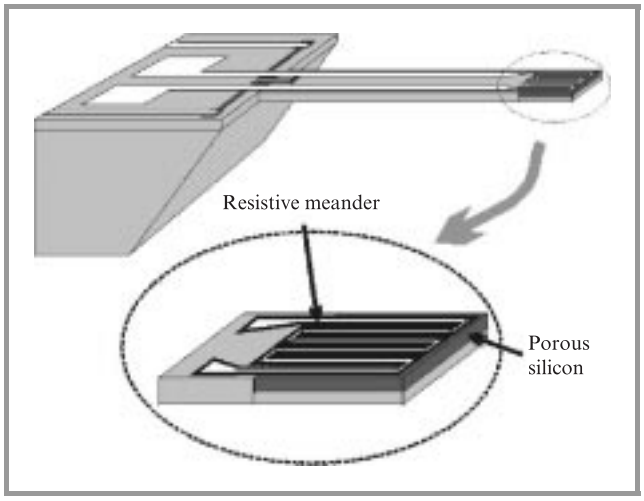


***Fig. 1.*** The idea of piezoresistive cantilever gas sensor with a porous silicon adsorbing spot.

Piezoresistors, necessary for resonance measurement are placed at the support of the cantilever [2] while porous silicon spot is formed on the free end of the beam to obtain maximum sensitivity. Assuming simplified model (see Fig. 2) of the adsorption process on the porous silicon area of the cantilever, elementary calculations of device sensitivity have been performed. Decrease of the resonance frequency due to gas adsorption on the free end of the cantilever beam can be estimated using the formula:

$$\Delta f_0 = \frac{1}{2\pi}\left(\sqrt{\frac{k}{M+\Delta m}} - \sqrt{\frac{k}{M}}\right), \qquad (1)$$

where $M$ is cantilever weight, $\Delta m$ is weight of adsorbed substance and $k$ is beam elasticity coefficient.

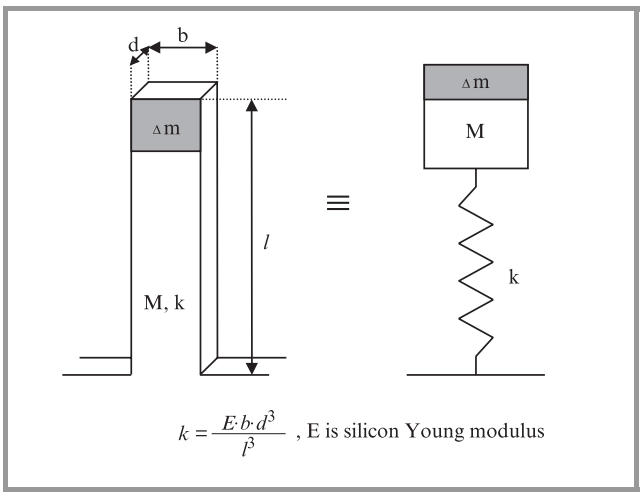


***Fig. 2.*** Simplified model of adsorption process on the porous cantilever.

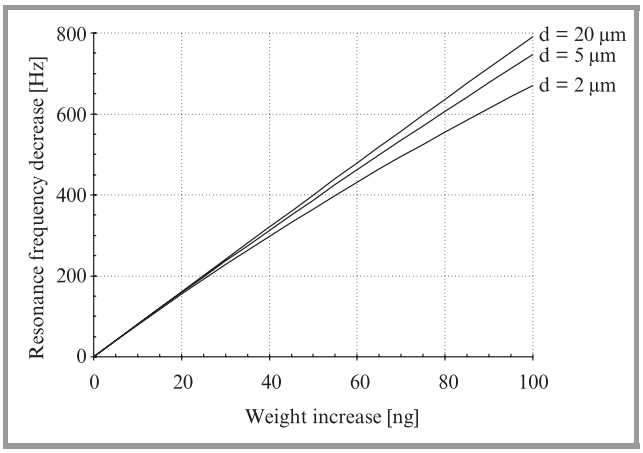


***Fig. 3.*** Resonance frequency decreases due to adsorption for cantilevers (480 x 160 $\mu$m) and 2, 5 or 20 $\mu$m thick.

For the simple beam (480 $\mu$m long, 160 $\mu$m wide and 20 $\mu$m thick) adsorption of 6 ng of substance causes resonance frequency decrease about 50 Hz. The comparison

of resonance frequency shift for similar cantilever differing from each other only in the thickness is shown in Fig. 3.

## 2. Fabrication process

Fabrication of the piezoresistive cantilever based devices is based on double-side silicon bulk/surface micromachining combined with standard CMOS processing. In fabricating the gas sensing microprobe, schematically illustrated in Fig. 4, we start with double side polished <100>-oriented, n-type, $3 \div 7$ Ωcm silicon wafers. After initial cleaning 800 nm of thermal oxide is grown. Standard photolithography defines mask for deep (30 $\mu$m) boron diffusion (Fig. 4a). During basic CMOS processing connecting diffusion paths are formed through boron diffusion from highly *in-situ* boron doped, CVD film (Fig. 4b) and piezoresistors are created through boron implantation (Fig. 4c). Phosphorous diffusion creates $n^+$-type regions, which serve as contacts to the substrate (Fig. 4d). Then backside photolithography with corner compensated pattern and deep silicon wet etching in KOH solution is performed to create $10 \div 20$ $\mu$m thick membrane. The wafer mounted in a chuck for front side protection is etched from the back. Next 100 nm of LPCVD silicon nitride is deposited on front surface and selective anodization is performed in chuck to convert boron-doped spots into porous silicon (Fig. 4e). Full electrical circuit is completed with metal connection and resistive meander (Fig. 4f). Finally thick photoresist is deposited for circuit and tip protection and cantilevers shapes are defined in the membrane by last photolithography and dry plasma etching (Fig. 4g). Devices have to be separated from the wafer mechanically (Fig. 4h).

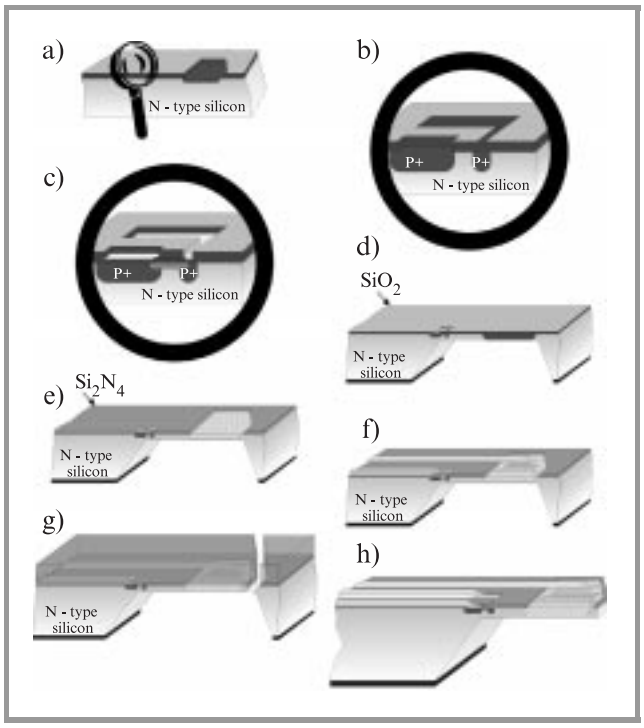


***Fig. 4.*** Gas sensitive piezoresistive cantilever fabrication sequence: a) masking of Si wafer, boron diffusion, b) formation of diffusion paths, c) implantation of piezoresistors, d) bulk micromachining – membrane etching, e) anodization – porous silicon formation, f) formation of metal connections and microheater, g) surface micromachining – deep RIE etching, h) separation of devices.

## 3. Microheater over porous silicon

Porous silicon is obtained by anodization of monocrystalline silicon in hydrofluoric acid solutions. The properties of this material are strongly dependent on the type and resistivity of the silicon and parameters used during the anodization process. Nevertheless, the porous silicon always exhibits extremely high chemical reactivity due to well-developed system of microscopic pores. Figure 5 shows AFM image of a typical porous silicon surface. Nanoporous layers made from lightly p-doped silicon present the highest porosity $(60 \div 80\%)$ and the highest value of the specific surface area (up to 600 $m^2/cm^3$) [3]. These unique properties make the material interesting for gas sensors applications. Usually porous silicon gas sensors make use of the influence of the gas adsorption on the electrical properties (e.g. resistivity) of the porous layer. Complex relation between amount of adsorbed substance and determined electrical parameter as well as rather small sensitivity is the main disadvantages of such sensors. Micromechanical structures give an opportunity for more direct relationships between measured and determined quantities. We have considered possibility of gas adsorption sensing on the basis of weight increase of piezoresistive cantilever beam. In contrast to the bulk structure consisting of the relatively thin porous silicon layer and huge volume of the silicon, the mass of the cantilever beam can be small enough to detect weight change, caused by adsorp-

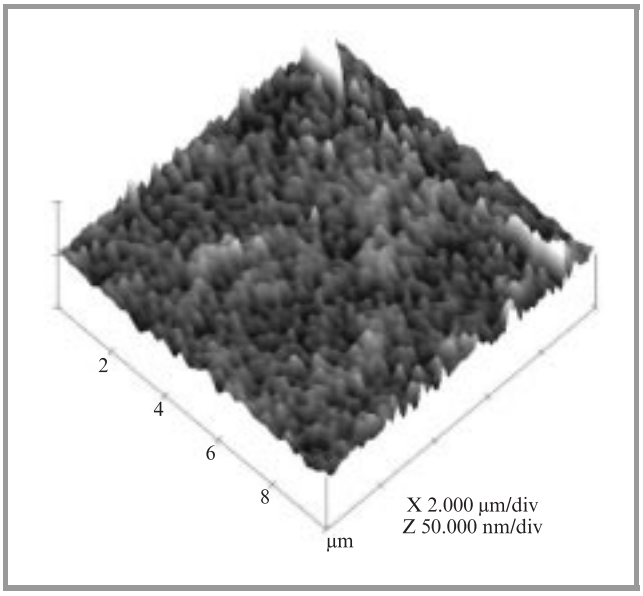


***Fig. 5.*** AFM image of porous silicon surface.

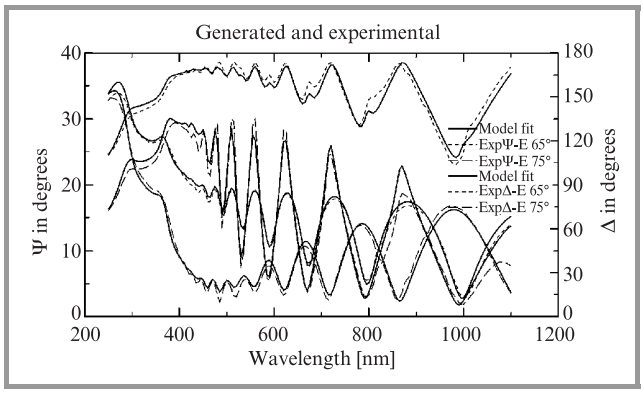


***Fig. 6.*** Elipsometric measurement of porous silicon.

tion of gases on the large internal surface of porous silicon. Particularly sensitive measurements of the cantilever resonance frequency are the only way to observe so small changes (below 1%) of the beam weight. Porous silicon shows various forms of appearance. Porous layer can be characterized with variable angle spectroscopic ellipsometry (Fig. 6). This technique is sensitive to capillary condensation of water in the porous material [4]. Well-developed porous silicon surface is not thermodynamically stable and thus the reduction of the specific area occurs during high temperature process. Therefore thermal budget should be limited after porous silicon formation and anodization process should be arranged at the end of whole processing sequence, e.g. just after membrane etching.


***Fig. 7.*** Cantilever beam integrated with piezoresistors and microheater.

Microheater made of resistive metal meander placed over porous silicon area is integrated with the sensor to outgas the porous area after each measurement, thus enabling a permanent monitoring of rapid changes of the atmosphere. It should be pointed out that different expansion coefficients of two layers (silicon beam coated with oxide) cause the cantilever deflection induced by the adsorption of infrared radiation or electrical power supplied to the microheater [5] (Figs. 7 and 8).

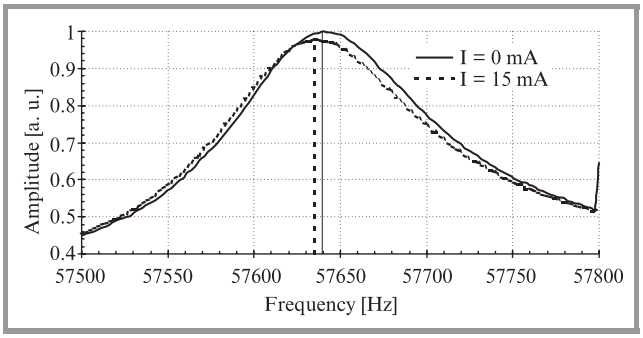


***Fig. 8.*** Shift in the cantilever resonance frequency due to the power supplied to the microheater.

# 4. Conclusions

In this paper, we present a novel piezoresistive cantilever beam sensor with porous silicon spot enabling measurements of the adsorbed substance weight. We have also described the essentials of its fabrication process. The sensitivity of the shift in the cantilever resonance frequency allows estimating amount of adsorbed substance with single nanogram resolution. It suggests applications of such microprobes for humidity and gas detection.

# Acknowledgement

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Paper

# An impact of physical phenomena on admittances of partially-depleted SOI MOSFETs

Daniel Tomaszewski, Lidia Łukasiak, Jan Gibki, and Andrzej Jakubowski

**Abstract — An influence of the selected physical phenomena: impact ionization in silicon and time variation of internal electric field distribution in partially-depleted (PD) SOI MOSFETs on several C-V characteristics of these devices is presented. The role of avalanche multiplication in the so-called „pinch-off" region is discussed in a more detailed way. The analysis is done using a numerical solver of drift-diffusion equations in silicon devices and using an analytical model of the PD SOI MOSFETs. The calculations results exhibit the significance of proper modelling of the phenomena in the floating body area of these devices.**

***Keywords — SOI MOSFET, floating body, avalanche ionization, recombination, displacement current, admittance.***

## 1. Introduction

It is well known, that I-V characteristics of partially depleted silicon-on-insulator (PD SOI) MOSFETs are determined by the balance of internal current components, which originate from different phenomena in intrinsic and extrinsic parts of the device. This was confirmed in several works and by numerical simulations. Obviously the same phenomena influence the C-V characteristics of the PD SOI MOSFETs [1, 2]. Due to the strong impact of these phenomena on the AC data reliable small-signal models of the PD SOI MOSFETs are relevant for the characterization and design purposes.

Below brief discussion of the influence of several phenomena on PD SOI MOSFETs capacitances is presented. It is based on preliminary numerical simulations and on computations made using an analytical small-signal non-quasi-static model of the PD SOI MOSFETs.

## 2. Numerical analysis of the PD SOI MOSFETs capacitances

Numerical simulation is a very valuable tool for detailed investigation of physical phenomena, which determine electrical characteristics of the semiconductor devices. One of the main advantages of this approach is a possibility of selective turning on/off the models of the particular phenomena. Owing to this an engineer may compare electrical characteristics of the device obtained with or without accounting for the given mechanism. Such approach is not possible when experimental data are analysed.

Impact ionization is very important for determining electrical parameters of the PD SOI MOSFETs. A role of impact ionization for I-V and C-V characteristics becomes more clear using the approach mentioned above. Figure 1 shows comparison of $C_{gfs}(V_{DS})$ and $C_{gfd}(V_{DS})$ data of the PD SOI MOSFET, calculated using ATLAS/SPISCES program [3] with avalanche ionization turned on and turned off. Parameters of the simulated device are as follows: L = 0.6 $\mu$m, $t_{Si} \approx 0.2\,\mu$m, $t_{ox,b} \approx 0.4\,\mu$m, $t_{ox,f} \approx 30$ nm, $N_B \approx 5 \cdot 10^{16}$ cm$^{-3}$.

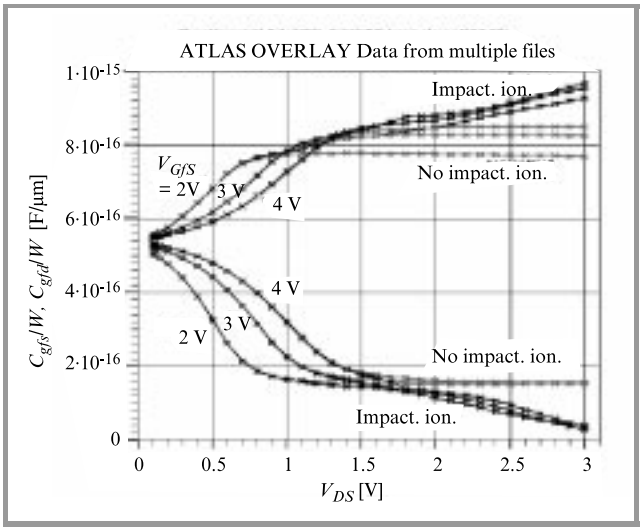


***Fig. 1.*** Influence of the impact ionization in silicon on the front gate-to-source and front gate-to-drain capacitances of the PD SOI MOSFET obtained with numerical simulations [3]. Comparison has been done by switching on/off the impact ionization components in the drift-diffusion equations. The device parameters are mentioned in the text.

For impact ionization turned on the following effects may be distinguished, which may be observed neither in bulk MOSFETs nor in hypothetic PD SOI MOSFETs without avalanche multiplication:

- increase of the $C_{gfs}$ capacitance in saturation range for increasing $V_{DS}$ voltage;
- decrease of the $C_{gfd}$ capacitance in saturation almost below zero farads for increasing $V_{DS}$ voltage.

Of course $C_{gfs}$ and $C_{gfd}$ capacitances consist of intrinsic and extrinsic components [4]. Extrinsic parts are related

to overlap and fringing capacitances and are almost constant. Intrinsic parts result from variation of electric field below the gate. If extrinsic components were „subtracted" from the total $C_{gfd}(V_{DS})$ curve, then it would appear, that intrinsic component of $C_{gfd}$ capacitance became negative. This result is not possible in the conventional MOSFETs, where $C_{gfd}$ capacitances approaches zero farads in saturation range. Moreover Flandre estimated in [1], that a small „plateau" visible in $C_{gfs}$ data (1 V ÷ 2 V, depending on the $V_{GfS}$ value) corresponded to $C_{gfs}$ value of ca. $0.72 \cdot C_{ox,f}$, where $C_{ox,f}$ denotes front gate voltage of the device analysed in [1]. Therefore it would considerably exceed value of $2/3 \cdot C_{ox,f}$, which is typical for bulk transistors. All the effects mentioned above are strictly related to the avalanche ionization in the depletion area of the drain-body junction. It is also worthwile to mention, that $C_{gfs}(V_{DS})$ characteristics of the PD SOI MOSFETs calculated with ionization turned off, differ from the same data obtained for the conventional MOSFETs. A $V_{GfS}$–controlled variation of the $C_{gfs}$ value in the saturation range can be observed only in the hypothetic PD SOI MOSFETs. This effect is probably due to small variations of the body potential, even if a large number of excess holes generated by ionization do not enter the thin Si-film. This may induce appropriate change of width of front gate depletion area and finally a change of $C_{gfs}$ intrinsic component related to coupling between front gate and source through the „pinch-off" region.
The simulator does not allow to switch multiplication on/off selectively, so the characteristics in Fig. 1 reflect the overall effect of the impact ionization in the space-charge regions, surrounding drain-body junction, where high electric field exists. However ionization in the „pinch-off" region is particularly relevant, because number of holes generated there and injected into the floating, quasi-neutral body area is several orders of magnitude higher, than the number of holes generated in the depletion region of the drain body junction. This results from the fact, that drift current component at the interface is much more higher, than the parasitic current flowing in the bulk part of the Si-film.

## 3. Role of displacement currents at the source-body and drain-body junctions

Displacement current components flowing through the extrinsic gate-source and gate-drain capacitances (for both gates) are connected in-parallel with the appropriate intrinsic capacitances. As has been mentioned earlier, they are almost constant, so their effect is self-evident. They simply increase the total capacitances. Moreover, as the currents flowing through them are purely capacitative, they do not influence the character of intrinsic admittances, i.e. they do not modify their partitioning between capacitance and conductance. Therefore for the simplicity it has been assumed here, that gates fringing capacitances may be neglected. Further brief analysis will be concerned with displacement currents at the junctions.

Figures 2 and 3 show fragments of $C_{gfs}(V_{GfS})$ and $C_{gfd}(V_{DS})$ characteristics of the PD SOI MOSFET, obtained using the model [5]. They were calculated for the device parameters, which are given in [6, Table 1]. Data presented in Fig. 2 correspond mainly to the accumulation range and transition between weak and strong inversion, which however is not modelled properly (in this model version subthreshold range is not accounted for). Data shown in Fig. 3 correspond to transition between non-saturation and saturation ranges.

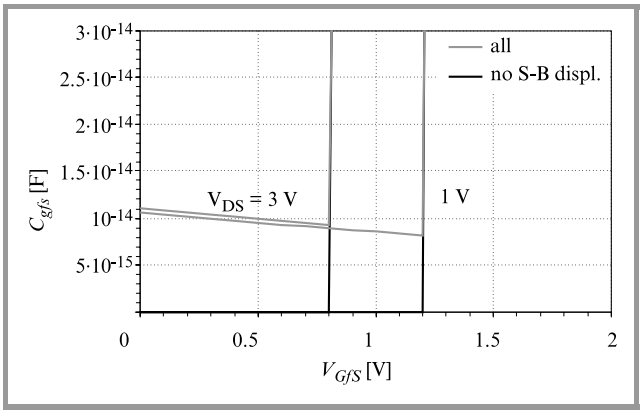


***Fig. 2.*** The influence of the displacement current at the source-body junction for the $C_{gfs}$ capacitances in the accumulation range.

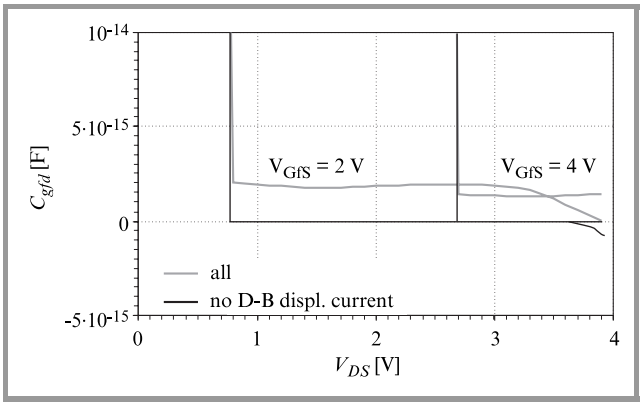


***Fig. 3.*** The effect of the displacement current at the drain-body junction for the $C_{gfd}$ capacitances in the saturation range.

In the accumulation range neglecting of the S-B junction displacement current causes, that $C_{gfs}$ capacitance vanishes. It means, that in this way the only path (except of neglected fringing capacitance) for HF signal propagation from source to front gate becomes closed. Thus in accumulation S-B junction admittance is connected in parallel with other components of the front gate-source admittance. Figure 2 illustrates also decrease of the junction admittance for increasing front gate voltage. It is caused probably by the narrowing of the quasi-neutral part of the Si-film, as front-gate induced depletion region widens.
In the saturation range (Fig. 3) $C_{gfd}$ capacitance calculated using the model [5] is also determined by parasitic compo-

nents related to fringing capacitances (neglected) and admittance of the drain-body junction. As expected in case of neglecting of displacement current component flowing through this junction $C_{gfd}$ vanishes to zero farads. However for sufficiently large drain-source voltage and gate-source voltage equal 2 V decrease of $C_{gfd}$ below zero may be observed. For $V_{GfS}$ = 4 V saturation and „kink" ranges are shifted towards higher values of $V_{DS}$, so effect of impact ionization on $C_{gfd}$ capacitance is not visible. Brief discussion of this effect based on results of numerical computations was presented in the previous section. Its analysis based on computations made using the analytical model is presented in the next section.

# 4. Role of phenomena in the „pinch-off" region

In the saturation range $C_{gfd}$ capacitance calculated using the model [5] is determined by parasitic components related to fringing capacitances (neglected) and admittance of the drain-body junction. This is analogous to the case of conventional MOSFETs. However contrary to bulk devices the D-B junction admittance has not purely capacitative character. In the drain bias range beyond „kink" it behaves rather like RLC circuit [7]. As a result, current components flowing through areas of high electric field induce such phase shift between AC components of the drain voltage and body potential, that intrinsic component of $C_{gfd}$ capacitance becomes negative. Figure 4 illustrates this effect. However turning off the appropriate AC component

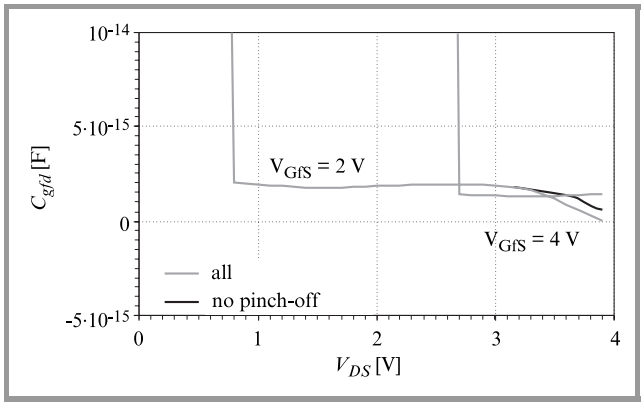


***Fig. 4.*** The influence of the impact ionization in the „pinch-off" region upon the $C_{gfd}$ capacitances in the saturation range. These data are consistent with Fig. 1.

of the drain current does not remove it completely. So a conclusion may be done, that a generally valid balance of all the AC currents in the PD SOI MOSFET makes, that their capacitances differ significantly from the appropriate capacitances of the bulk devices. Even a small difference in phases or amplitudes of currents AC components may induce unusual admittance behaviour.

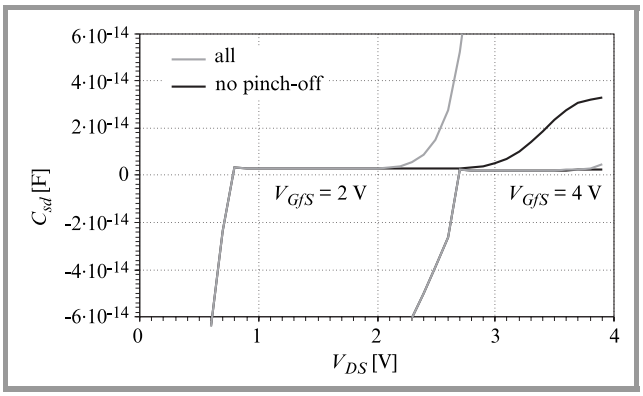


***Fig. 5.*** The influence of the impact ionization in the „pinch-off" region upon the $C_{sd}$ capacitances in the saturation range.

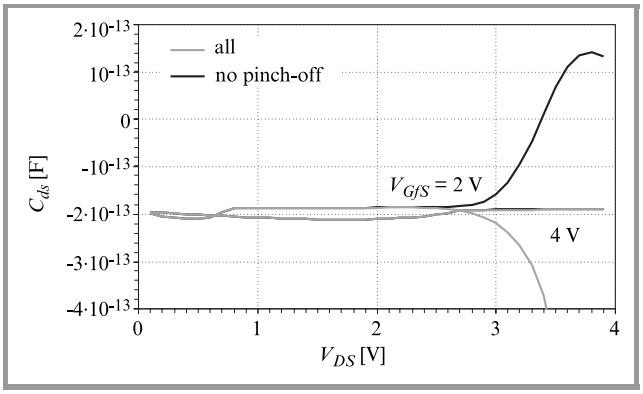


***Fig. 6.*** The influence of the impact ionization in the „pinch-off" region upon the $C_{ds}$ capacitances in the saturation range. The nonreciprocality of the $C_{ds}$ and $C_{sd}$ capacitances is obvious.

Figures 5 and 6 show also effect of impact ionization on $C_{ds}$ and $C_{sd}$ capacitances of the PD SOI MOSFET. It is very difficult to measure these variables, because during the measurement a large current flows between source and drain contacts. Such data are not available in the literature. Only simulated characteristics may be compared and discussed. The data presented in Figs. 5 and 6 show that in the saturation range switching the impact ionization off completely changes character of these capacitances. More detailed analysis of this effect is very difficult and will be presented in future together with comparison with characteristics obtained numerically. The eventual improvement of the model towards better modelling high-frequencies effects should be also considered. These data in Figs. 5 and 6 also illustrate, that both capacitances are non-reciprocal, which is typical for multi-port active devices.

# 5. Conclusions

The small-signal model of the PD SOI MOSFETs shows qualitatively the importance of the following phenomena for the proper modelling of C-V characteristics:

- displacement current at the source-body and drain-body junctions,
- avalanche multiplication of carriers within the „pinch-off" region.

Moreover it may be stated, that generation/recombination phenomena are less critical for the small-signal analysis of these devices.

## Acknowledgment

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Paper

# A model of partially-depleted SOI MOSFETs in the subthreshold range

Daniel Tomaszewski, Lidia Łukasiak, Andrzej Jakubowski, and Krzysztof Domański

**Abstract — A steady-state model of partially-depleted (PD) SOI MOSFETs I-V characteristics in subthreshold range is presented. Phenomena, which must be accounted for in current continuity equation, which is a key equation of the PD SOI MOSFETs model are summarized. A model of diffusion-based conduction in a weakly-inverted channel is described. This model takes into account channel length modulation, drift of carriers in the „pinch-off" region and avalanche multiplication triggered by these carriers. Characteristics of the presented model are shown and briefly discussed.**

***Keywords — SOI MOSFET, subthreshold range, floating body, transconductance.***

## 1. Introduction

Silicon-on-insulator (SOI) CMOS circuits are predestined for operation at low supply bias and at higher temperatures than their conventional counterparts. These advantages result from the reduced area of p-n junctions, what implies lowered level of junction leakage currents. Therefore these devices exhibit lowered level of power consumption. However, proper operation at low current level is possible only when transistors are carefully designed and manufactured. Thus availability of reliable physical models of PD SOI MOSFETs is important. These models may be used for simulation and characterization purposes.

The aim of this work was to develop a steady-state model of I-V characteristics of the PD SOI MOSFETs. Although several models are already known [1–4], they were derived using assumptions, which are in our opinion, not fully reasonable.

## 2. DC models of currents in the Si-film

The proposed model is based on the same idea as previously developed DC model of the PD SOI MOSFETs in the strong inversion range [5]. The main equation, which describes its I-V characteristics expresses a total current continuity condition in the device. It is given with formula (1):

$$I_S + I_D = 0\,, \tag{1}$$

where source and drain currents $I_S$, $I_D$ are given as sums of current components flowing through the electrodes (Eqs. (2), (3))

$$I_S = I_{c,f} + I_{rec,SB} + I_{diff,n,B}(W_{SB})\,, \tag{2}$$

$$I_D = -M_{sat,f}\, I_{c,f} - M_b \left[ I_{gen,DB} + I_{diff,n,B}(L - W_{DB}) \right]. \tag{3}$$

For the given DC bias point Eq. (1) allows to calculate the floating body-source voltage in the device – a key parameter of the presented model. In the above equations the following components may be mentioned:

- $I_{c,f}$ – diffusion current in the weakly inverted channel at the front Si-$SiO_2$ interface; model of this component is described in the next section;
- $I_{diff,n,B}$ – diffusion current in the quasi-neutral part of the thin Si-film; this current is accompanied by the recombination of excess minority carriers (electrons) with the excess majority carriers introduced to the Si-film mainly by the avalanche ionization phenomena in the depletion region of surrounding drain area;
- $I_{rec,SB}$ – current related to recombination within the space-charge region of the source-body junction;
- $I_{gen,DB}$ – current related to generation within the depletion region of the drain-body junction;
- $M_{sat,f}$ – coefficient of avalanche multiplication in the „pinch-off" region at the front Si-$SiO_2$ interface;
- $M_b$ – coefficient of avalanche multiplication in the depletion region of the drain-body junction.

Body diffusion current $I_{diff,n,B}$ at any coordinate $y$ ($W_{SB} \le y \le L - W_{DB}$) is given with the formula (4), where all its parameters have their usual meanings. Factor $W\,(t_{Si} - W_{GfB} - W_{GbB})$ denotes of course area of diffusion current path. Body diffusion current at the edge of the source-body junction depletion area ($y = W_{SB}$) is contained in the source current. The current at the edge of the drain-body junction depletion area ($y = L - W_{DB}$) is contained in the drain current. Moreover,

$$I_{diff,n,B}(y) = W(t_{Si} - W_{GfB} - W_{GbB})\, q \frac{D_{n,B}}{L_{n,B}} n_{B,eq} \times \\ \times \frac{(eV_{BD}/V_{t-1})\,\cosh\frac{y - W_{SB}}{L_{n,B}} - (eV_{BS}/V_{t-1})\,\cosh\frac{L - W_{DB} - y}{L_{n,B}}}{\sinh\frac{L - W_{SB} - W_{DB}}{L_{n,B}}}. \tag{4}$$

Equation (4) is used in models of bipolar transistors to describe transport of minority carriers through base [6]. Moreover, due to the fact, that transistor base is narrow the formula (4) is usually applied in linearized form. However, in case of SOI MOSFETs such approximation cannot be used. The equation (4) was used earlier for the purpose of modelling of PD SOI MOSFETs operation in the strong inversion range [5].

S-B junction recombination and D-B junction generation currents are given with formulae (5) and (6), respectively. They were also used in case of PD SOI MOSFETs in the strong inversion range [5]. They are obtained as solutions of trasport equations in the space-charge areas of the forward or reverse biased p-n junctions, respectively and are based on SRH (Shockley-Read-Hall) model of recombination phenomena. Similarly to the case of diffusion current at the drain generation current is also multiplied by $M_b$

$$I_{rec,SB} = W\left(t_{Si} - W_{Gf,B} - W_{Gb,B}\right)\frac{kTn_i}{2\tau_J}\frac{\sqrt{\exp\frac{V_{BS}}{V_t}-1}}{V_{bi}-V_{BS}}\times \\ \times 2\arctan\frac{\left(\exp\frac{\phi_{F,N}}{V_t}-\exp\frac{V_{BS}-\phi_{F,p}}{V_t}\right)\sqrt{\exp\frac{V_{BS}}{V_t}-1}}{\exp\frac{V_{BS}}{V_t}-1+\left(\exp\frac{\phi_{F,n}}{V_t}+1\right)\left(\exp\frac{V_{BS}-\phi_{F,p}}{V_t}+1\right)}, \quad (5)$$

$$I_{gen,DB} = W\left(t_{Si}-W_{Gf,B}-W_{Gb,B}\right)\frac{kTn_i}{2\tau_J}\frac{W_{DB}}{2\phi_F-V_{BD}}\sqrt{1-\exp\frac{V_{BD}}{V_T}}\times \\ \times \ln\left|\frac{\exp\frac{\phi_F}{V_T}+1-\sqrt{1-\exp\frac{V_{BD}}{V_T}}}{\exp\frac{\phi_F}{V_T}+1+\sqrt{1-\exp\frac{V_{BD}}{V_T}}}\cdot\frac{\exp\frac{V_{BD}-\phi_F}{V_T}+1+\sqrt{1-\exp\frac{V_{BD}}{V_T}}}{\exp\frac{V_{BD}-\phi_F}{V_T}+1-\sqrt{1-\exp\frac{V_{BD}}{V_T}}}\right|. \quad (6)$$

# 3. DC model of current flow at the front interface in the weak inversion range

Well known formula (7) is used in to calculate the current in the weakly inverted channel [7]

$$I_{c,f} = \frac{W}{L_{eff}}\,\mu_{c,f}\,V_t\left[\,Q_{c,f}(L_{eff}) - Q_{c,f}(0)\right]. \quad (7)$$

In the proposed model, however, the channel length modulation is taken into account. This approach is similar to widely used models of MOSFETs operation in saturation range. Intuitively it is obvious, that phenomena in the vicinity of the drain area in subthreshold and saturation ranges should be described in the same way. After all in weak inversion range channel shortening should be even larger than in the saturation range, which is obviously closer to the full strong inversion range. Results of numerical experiments also confirm this thesis [8]. In the presented model three variables: $L_{eff}$, $Q_{c,f}(0)$, $Q_{c,f}(L_{eff})$ require further evaluation.

Under gradual channel approximation (GCA) conditions $Q_{c,f}(0)$ may be obtained through approximate solution of the 1D Poisson equation, which accounts for minority carriers [7]

$$Q_{cf}(0) \approx \\ \approx -\sqrt{2\varepsilon_{Si}qN_B}\frac{\sqrt{V_t}}{2}\exp\left(\frac{-2\phi_F+V_{BS}}{V_t}\right)\frac{\exp\left(\frac{\Psi_{s,f}-\Psi_B}{V_t}\right)-1}{\sqrt{\frac{\Psi_{s,f}-\Psi_B}{V_t}}}, \quad (8)$$

where surface potential at the front interface $\Psi_{s,f}$ may be obtained using depletion approximation:

$$\Psi_{s,f} - \Psi_B = \frac{\gamma_f^2}{4}\cdot\left[\sqrt{1+\frac{4}{\gamma_f^2}\cdot(V_{Gf}-V_{FB,f}-\Psi_B)}-1\right]^2 \quad (9)$$

and $\Psi_B$ denotes potential of the quasi-neutral part of the thin Si-film. Other variables in formulas (8) and (9) have usual meanings.

Similarly to the model of MOSFETs characteristics in the saturation range, at $y = L_{eff}$ GCA conditions remain still valid. Therefore $Q_{c,f}(L_{eff})$) may be obtained using the same method as $Q_{c,f}(0)$. Therefore the following relation may be formulated:

$$Q_{c,f}(L_{eff}) = Q_{c,f}(0)\exp\left(\frac{-V_{c,f}(L_{eff})}{V_t}\right). \quad (10)$$

Here, $V_{c,f}(L_{eff})$ denotes voltage between both ends of the channel. In earlier works [2, 4] minority carriers charge at the drain end of channel was reduced with respect to that at the source according to

$$Q_{c,f}(L) = Q_{c,f}(0)\exp\left(\frac{-V_{DS}}{V_t}\right). \quad (10a)$$

In order to determine mobile carriers charge at the drain end of channel the approach known from the saturation range modelling is used. Similarly to the case of the boundary between strongly inverted channel and „pinch-off" regions the following current continuity condition below threshold at $y = L_{eff}$ may be formulated [7]

$$I_{c,f} = -W\,Q_{c,f}(L_{eff})\,\upsilon_{max}, \quad (11)$$

$$I_{c,f} = \frac{W}{L_{eff}}\,\mu_{c,f}\,V_t\left[Q_{c,f}(L_{eff}) - Q_{c,f}(0)\right]. \quad (12)$$

Equation (11) expresses the condition, that in the area between end of channel and drain carriers travel with maximum available velocity $\upsilon_{max}$. The equations (11) and (12) allow to obtain the following relation between $Q_{c,f}(0)$ and $Q_{c,f}(L_{eff})$ in the subthreshold region:

$$Q_{c,f}(L_{eff}) = \frac{Q_{c,f}(0)}{1+\frac{\upsilon_{max}L_{eff}}{\mu_{c,f}V_t}}. \quad (13)$$

Next, using Eq. (10), $V_{c,f}(L_{eff})$ can be found very easily

$$V_{c,f}(L_{eff}) = V_t\ln\left(1+\frac{\upsilon_{max}\,L_{eff}}{\mu_{c,f}\,V_t}\right). \quad (14)$$

As expected, in the subthreshold region the voltage drop between the end of the weakly inverted channel and the source (analogous to $V_{DS,sat,f}$ – the saturation voltage at the front Si-$SiO_2$ interface) is low and independent of front gate voltage.

As the last variable necessary for calculation of the subthreshold current according to Eq. (7) effective length $L_{eff}$ of the region where GCA is valid must be determined. It may be calculated approximately using 1D solution of the Poisson equation under full depletion conditions. This is

very similar to the method of estimation of channel length modulation in the saturation range and corresponds to the simplest case of zero electric field at the channel end

$$L_{eff} = L - \sqrt{\frac{2\varepsilon_{Si}}{q\,N_B} \cdot \left(V_D - \Psi_{s,f}\right)}\,. \tag{15}$$

# 4. I-V characteristics of the PD SOI MOSFET model in the weak inversion range

I-V characteristics of the PD SOI MOSFET were calculated using the model presented in the previous sections. Parameters of this device are listed in [9, Table 1].
A set of $I(V_{GfS})$ characteristics calculated both for weak and strong inversion and for several values of the drain-source voltage are shown in Fig. 1. These curves illustrate several effects, which are observed both in numerical calculations and in experimental data [2, 3]:

- decrease of the threshold voltage with increasing drain bias,
- increase of the transconductance in the weak inversion range or increasing increase of VDS voltage.

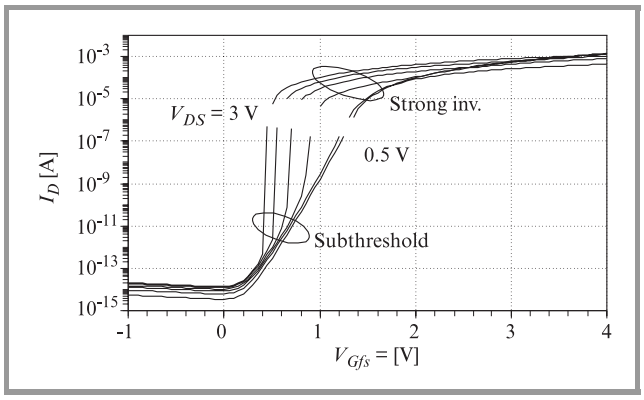


***Fig. 1.*** A family of simulated $I_D(V_{GfS})$ characteristics of the PD SOI MOSFET ($W = 100$ $\mu$m, $L = 9.4$ $\mu$m, $T_{Oxf} = 32.8$ nm, $T_{Oxb} = 400$ nm, $T_{Si} = 150$ nm, $N_B = 9 \cdot 10^{16}$ cm$^{-3}$, $V_{GbS} = 0$ V).

Moreover the curves corresponding to the weak and strong inversion ranges, although not connected together, exhibit quite fine transitions between both ranges. This is probably due to the fact, that channel length modulation in the subthreshold range and current conduction close to drain are accounted for in a more proper way. We hope, that the presented approach could help to avoid applying non-physical fitting procedures [4].
Figure 2 shows the behaviour of the thin Si-film potential for varying front gate voltage and for several drain-source voltages. Again variations of threshold voltage is evident and even much more pronounced, than in case of model with no subthreshold range option. Therefore it may be stated, that even in the weak inversion range, when total current level is low, the floating-body phenomena are also very relevant for the calculation of I-V characteristics of the PD SOI MOSFETs. It results from the fact, that they are still determined by the subtle balance of fluxes of carriers inside the transistor and the channel current in subthreshold range is multiplied by avalanche ionization in the same way as in the strong inversion.

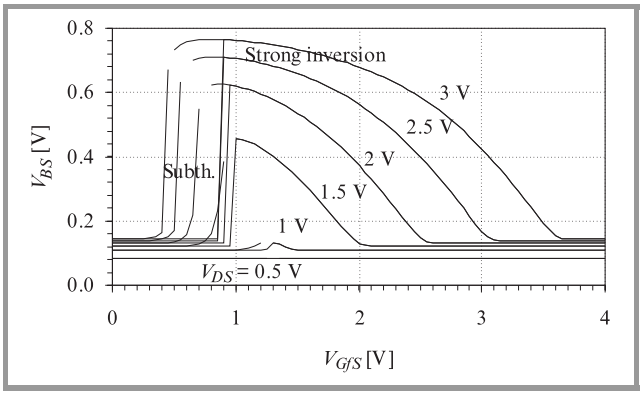


***Fig. 2.*** Comparison of simulated $V_{BS}(V_{GfS})$ characteristics of the PD SOI MOSFET obtained with or without current model in the subthreshold range [5].

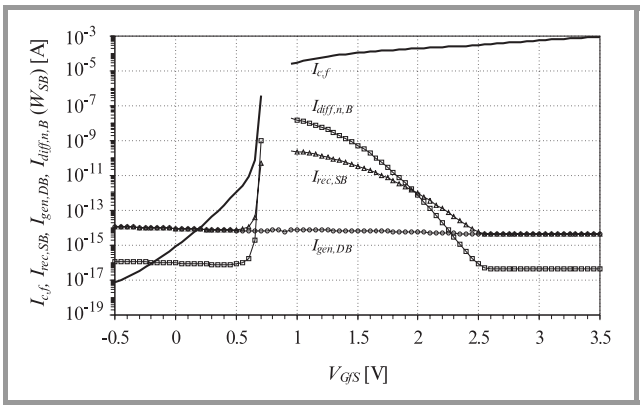


***Fig. 3.*** Comparison of current components in the PD SOI MOSFET (for $V_{DS} = 2$ V): surface diffusion current $I_{c,f}$, bulk diffusion current at the source $I_{diff,n,B}(W_{SB})$, source recombination current $I_{rec,SB}$, and drain generation current $I_{gen,DB}$.

Figure 3 shows comparison of several current components flowing inside the MOSFET in weak and strong inversion ranges: surface diffusion current $I_{c,f}$, bulk diffusion current at the source $I_{diff,n,B}(W_{SB})$, source recombination current $I_{rec,SB}$, and drain generation current $I_{gen,DB}$. The plot shows, that in accumulation range the phenomena in the device are determined entirely by the balance of $I_{diff,n,B}$, $I_{rec,SB}$ and $I_{gen,DB}$ components. The front channel current becomes comparable with them for front gate voltage exceeding 0 V. But it does not reach level, which is sufficient to switch

avalanche-ionization on before $V_{GfS}$ exceeds 0.5 V. Then floating body effects begin to dominate and transistor I-V characteristics exhibit the so-called „kink-effect". In this region a very sharp increase of $I(V_{GfS})$ curve is visible. It is evident that the very high transconductance is strictly correlated with the rapid increase of the body potential, which is in-turn triggered by the avalanche multiplication. Further increase of the front gate voltage results in „smoothing" of the current components variations, because the channel current entirely dominates, so currents balance condition is almost automatically fulfilled. Finally transistors enters the nonsaturation region, when ionization in the „pinch-off" region disappears. Channel current, which dominates is almost proportional to the gate voltage, whereas currents exponentially dependent on body-source voltage decrease by several orders.

# 5. Conclusions

The paper presents a physical steady-state model of the PD SOI MOSFETs I-V characteristics in the subthreshold range. It accounts for majority of physical effects relevant for proper description of transistors operation. Several model equations were derived on the analogy of saturation range modelling approach. Owing to this, pretty good transition between subthreshold and strong inversion ranges was obtained. Moreover the model exhibits significant decrease of $V_{TH,f}$ for increasing $V_{DS}$ voltage and rapid increase of transconductance for increasing $V_{DS}$ voltage.
Further efforts in this area should be directed towards verification of the model using experimental data and results of numerical calculations using eg. ATLAS/SPISCES simulator. Because PD SOI MOSFETs I-V characteristics may suffer from parasitic edge transistors influence the numerical data may be particularly valuable.

# Acknowledgment

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**Andrzej Jakubowski** – for biography, see this issue, p. 33.

**Lidia Łukasiak** – for biography, see this issue, p. 34.

**Krzysztof Domański, Daniel Tomaszewski** – for biography, see this issue, p. 39.

*Paper*

# Comparison of gate leakage current components in metal-insulator-semiconductor structures with high-*k* gate dielectrics

Tomasz Janik, Andrzej Jakubowski, Bogdan Majkusiak,
and Michał Korwin-Pawłowski

**Abstract — Numerical simulations of the gate leakage current in metal-insulator-semiconductor (MIS) structures based on the transfer matrix approach were carried out. They show contribution of different components of this current in MIS structures with best known high-*k* dielectrics such as $Ta_2O_5$ and $TiO_2$. The comparison of the gate leakage current in MIS structures with $SiO_2$ layer as well $Ta_2O_5$ and $TiO_2$ layers is presented as well. Additionally, the minimum Si electron affinity to a gate dielectric which allows to preserve given level of the gate leakage current is proposed.**

***Keywords* — *MIS structures, ultrathin dielectrics, high-k dielectrics.***

## 1. Introduction

High-*k* dielectrics are attractive for microelectronics as they allow to avoid problems with extremely thin $SiO_2$ layer as a gate dielectric in MIS structures. Although some of these dielectrics, e.g. $Ta_2O_5$ and $TiO_2$, have experienced intensive technological exploration, basic physical constants of these materials have not been completely recognized yet. However, as far as best known high-*k* dielectrics are considered, its energy gaps manifest apparently smaller values than the $SiO_2$ band gap [1, 2]. Similarly, Si electron affinity to those dielectrics appears to be significantly smaller than its affinity to $SiO_2$. Consequently, the significant increase of over barrier current flowing through a such dielectric layer becomes possible. Contrary to that, since high-*k* dielectric layers can be fabricated as relatively thick layers in comparison with $SiO_2$ layers, their direct tunneling component is decreased. As a result, the relation between different components of the gate leakage current is changed in comparison to the $SiO_2$ case which finally may affect the gate voltage dependence of this current as well as breakdown and reliability properties of the gate dielectric.

In this work contribution of different current components to the gate leakage current in best known high-*k* dielectrics in MIS structures is analysed. Additionally, the minimum Si electron affinity to a gate dielectric which allows to preserve given level of this current is proposed.

## 2. Gate current components description

Electrostatic properties of a gate dielectric are defined by its electric permittivity $\varepsilon_x$ and thickness $t_x$. In further analysis the same capacitance per unit area of both high-*k* dielectric and $SiO_2$ layer is assumed

$$C_x = C_{ox} \,, \tag{1}$$

where $C_x = \varepsilon_x / t_x$ and $C_{ox} = \varepsilon_{ox} / t_{ox}$ (indexes „*x*" and „*ox*" refer to a high-*k* dielectric and $SiO_2$ layer, respectively). Then

$$t_x = R t_{ox} \,, \tag{2}$$

where $R = \varepsilon_x / \varepsilon_{ox}$ denotes a high-*k* dielectric electric permittivity normalized to the $SiO_2$ electric permittivity.

The quality of the dielectric layer as well as the state of its both surfaces are not addressed in this work. Then, the gate leakage current can be considered as a current of carriers tunneling from the semiconductor substrate to the gate or from the gate to the semiconductor substrate. This current depends on the height and shape of the potential barrier that corresponds to the dielectric layer. The height and shape of the barrier depend in turn on dielectric energy gap $E_{gx}$, the Si-dielectric electron affinity $\chi_{cx}$ and the electric field in the dielectric $F_x$. The energy diagram of the metal-dielectric-semiconductor system is shown in Fig. 1. In further analysis only the electron current flowing from the semiconductor conduction band to the gate is considered. It consists of three components, denoted in Fig. 1: direct tunneling current $J_d$, Fowler-Nordheim tunneling current $J_{FN}$ and over-barrier current $J_{ob}$.

To check a contribution of different components of the gate leakage current flowing through best known high-*k* dielectrics, a numerical simulation of the gate leakage current was carried out. The components of the gate leakage current were calculated with the following formula:

$$J = q \int_{E_0}^{E_1} \left[ N_m(E_x) - N_s(E_x) \right] P(E_x) \, dE_x \tag{3}$$

proper when the transverse electron mass change during the electron move from the semiconductor substrate to the gate is neglected. In Eq. (3) $E_x$ is the electron kinetic energy in

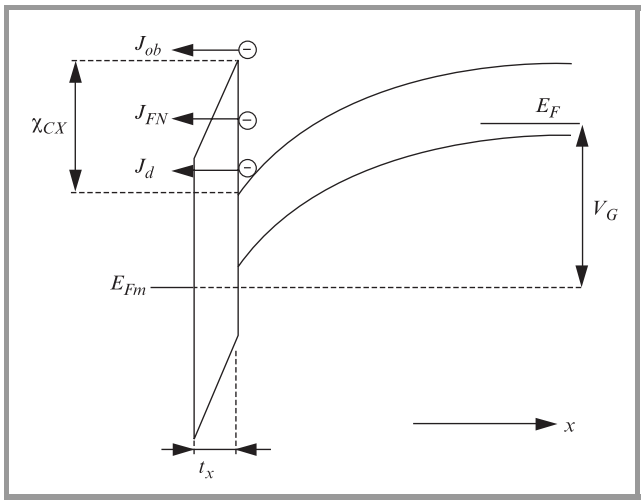


***Fig. 1.*** The energy diagram of the metal-insulator-semiconductor system.

the $x$ direction perpendicular to the semiconductor surface, $P(E_x)$ is the probability of an electron with a given energy $E_x$ transmission from the semiconductor to the gate, and $N_m(E_x) - N_s(E_x)$ is the „supply function" where

$$N_{m,s}(E_x) = \frac{4\pi m^*}{h^3} k_B T \ \ln\left[1 + \exp\left(\frac{E_{Fm,s} - E_x}{K_B T}\right)\right] \quad (4)$$

with $E_F$ as the Fermi potential and indexes $m$ and $s$ refering to the gate and to the semiconductor, respectively [3].
To calculate the probability $P(E_x)$ one needs to know the wavefunction amplitude $F_s$ of an electron which enters the dielectric from the semiconductor-dielectric surface and the wavefunction amplitude $F_m$ of an electron which leaves the dielectric while entering the gate

$$P = \frac{k_m / m_m^*}{k_s / m_s^*} \left|\frac{F_m}{F_s}\right|^2 . \quad (5)$$

Here $m_m^*$ and $m_s^*$ are electron effective masses, and $k_m$ and $k_s$ are electron wavevectors, in the gate and the semiconductor, respectively.
The probability $P(E_x)$ was calculated with the transfer matrix approach. Using this approach, the potential barrier created by a gate dielectric was approximated by the step-like potential barrier. Then, the amplitude of the electron wavefunction $F_{i-1}$ entering the $x_i$ plane between the $(i-1)$-th and $i$-th potential steps is related to the electron wavefunction $F_i$ leaving this plane by the following relation

$$\begin{bmatrix} F_{i-1} \\ R_{i-1} \end{bmatrix} = \begin{bmatrix} \frac{k_{i-1}+k_i}{2k_{i-1}} \exp\left[i(-k_{i-1}+k_i)x_i\right] & \frac{k_{i-1}-k_i}{2k_{i-1}} \exp\left[i(-k_{i-1}-k_i)x_i\right] \\ \frac{k_{i-1}-k_i}{2k_{i-1}} \exp\left[i(k_{i-1}+k_i)x_i\right] & \frac{k_{i-1}+k_i}{2k_{i-1}} \exp\left[i(k_{i-1}-k_i)x_i\right] \end{bmatrix} \begin{bmatrix} F_i \\ R_i \end{bmatrix}, \quad (6)$$

where $R_{i-1}$ and $R_i$ are amplitudes of the electron wavefunctions propagating in opposite direction than the wavefunctions described by $F_{i-1}$ and $F_i$, $k_i$ is the $x$-direction component of the electron wavevector in the $i$-th potential step. The wavevector $k_i$ is calculated using the two band model of the dielectric's potential barrier.
In Eq. (3) the ends of the integration depend on a calculated gate tunnel component. In case of the direct tunneling $E_0 = 0$ and $E_1 = \chi_{cx} - qV_x$, in case of the Fowler-Nordheim tunneling $E_0 = \chi_{cx} - qV_x$ and $E_1 = \chi_{cx}$ and in case of the over barrier component $E_0 = \chi_{cx}$ and $E_1 = \infty$. However, for larger gate voltages, when $qV_x > \chi_{cx}$ there is no direct tunneling component and then $E_0 = 0$ for the Fowler-Nordheim tunneling component.
In simulations the 1 nm equivalent oxide thickness ($t_{eq}$) of high-$k$ dielectrics was assumed, leading, according to Eq. (2), to

$$t_x = R \ \ [\text{nm}] . \quad (7)$$

The following dielectrics were considered: $SiO_2$, $Ta_2O_5$ and $TiO_2$, with its electric permittivity $\varepsilon_x$, energy gap $E_{gx}$ and electron affinity $\chi_{cx}$ according to Table 1. For the $TiO_2$ layer two cases of different electric permittivity were considered: the thin layer permittivity 30 and thick layer permittivity 80. Since the poor availability of published data of electron effective mass values in high-$k$ dielectrics we assumed their value same as in $SiO_2$ layer, i.e., half the free electron mass. For comparison we carried out simulations for a larger value of the electron effective mass in a dielectric which led us to the conclusion that larger the electron mass smaller the Fowler-Nordheim current, significantly smaller the direct tunneling current, practically unchanged the over-barrier current and, consequently, smaller the total gate leakage current.

Table 1
Parameters of the considered dielectrics applied in simulations (parameters of high-$k$ dielectrics after [1])

| Dielectric | $E_{gx}$ [eV] | $\chi_{cx}$ [eV] | $\varepsilon_x$ |
|---|---|---|---|
| $SiO_2$ | 9 | 3.15 | 3.9 |
| $Ta_2O_5$ | 4 | 1.45 | 25 |
| $TiO_2$ | 3.3 | 1.1 | 30, 80, $(30 \div 80)$ |

## 3. Results

In simulations $n^+$-polysilicon gate was assumed. Figures $2 \div 5$ show dependence of the gate leakage current and its components on the gate voltage for the all considered gate dielectrics. In case of $SiO_2$ the direct tunneling component dominates in the total current in a wide range of the gate voltage, up to 3 V. Then, the Fowler-Nordheim tunneling component becomes to dominate and determine the total gate current. In $SiO_2$ case contribution of the over-barrier current in the total gate leakage current is extremely small due to a high potential barrier (3.15 eV) that electrons encounter at the border between the silicon substrate and the $SiO_2$ layer. In case of $Ta_2O_5$ layer the direct tunneling

and Fowler-Nordheim tunneling components dominate in the total current, similarly as in the previous case, but the latter component becomes to dominate for the gate voltage equal to 1.5 V. In case of $TiO_2$ layers the total gate current is determined by the Fowler-Nordheim component in the whole gate voltage range. Additionally, one can see significant reduction of the direct tunneling component. Here, in spite of the fact that the over-barrier current level remains almost unchanged, one can see significant increase of the over-barrier component contribution to the total gate current in comparison with previous cases. This is due to a low potential barrier (1.1 eV) that electrons encounter at the border between the silicon substrate and the $TiO_2$ layer.

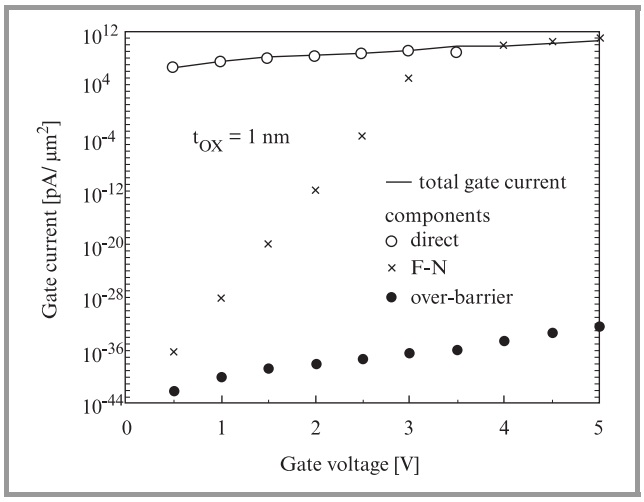


***Fig. 2.*** Dependence of the gate leakage current and its components on the gate voltage in case of MIS structure with $SiO_2$ as a gate dielectric.

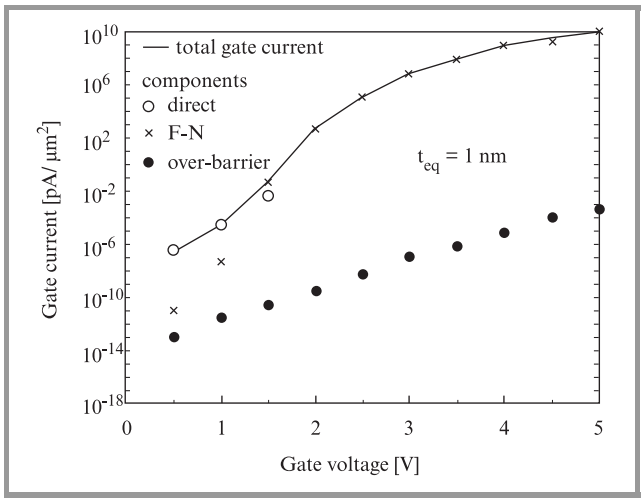


***Fig. 3.*** Dependence of the gate leakage current and its components on the gate voltage in case of MIS structure with $Ta_2O_5$ as a gate dielectric.

The gate leakage current normalized to the $SiO_2$ layer current for structures with different dielectrics is shown in Fig. 6. One can see significant dominance of the $SiO_2$ layer current within the range of small and moderate voltages up to 3 V. The leakage current of the $TiO_2$ layer with the electric permittivity 30 exceeds the $SiO_2$ layer current if the gate voltage is increased above 3 V. However, one must remember that in 1 nm thick $SiO_2$ layer the breakdown will occur for the gate voltage larger than the flat-band voltage by about 1.5 V, which in the case of the assumed n+-polysilicon gate gives the gate voltage approximately equal to 0.5 V.

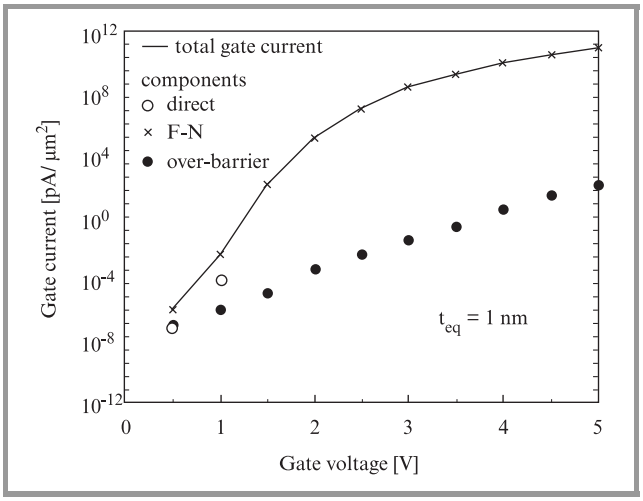


***Fig. 4.*** Dependence of the gate leakage current and its components on the gate voltage in case of MIS structure with $TiO_2$ with electric permittivity 30 as a gate dielectric.

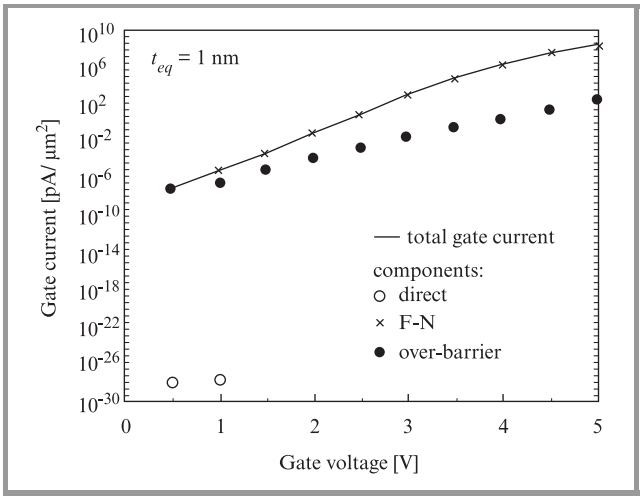


***Fig. 5.*** Dependence of the gate leakage current and its components on the gate voltage in case of MIS structure with $TiO_2$ with electric permittivity 80 as a gate dielectric.

The minimum Si-dielectric electron affinity which ensures the flow of the same electron leakage current as the current flowing through the $SiO_2$ layer is shown in Fig. 7. One can see results of a numerical simulation for the 1 V gate voltage (the curve denoted as „total current limit"), tending to be a standard supply voltage in future IC generations.

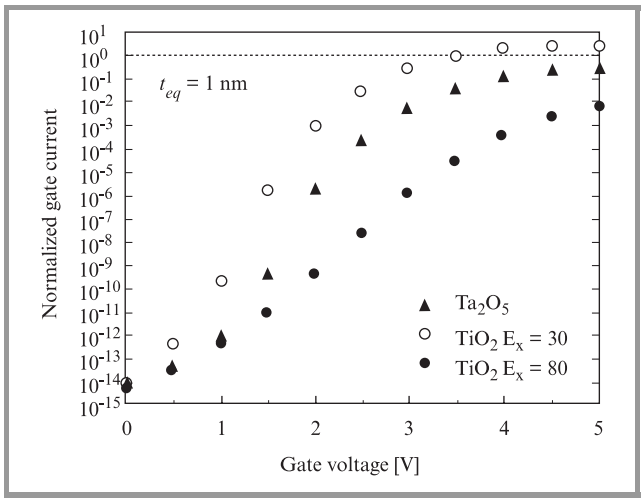


***Fig. 6.*** Gate voltage dependence of the gate leakage current normalized to the $SiO_2$ layer current for MIS structures with different dielectrics.

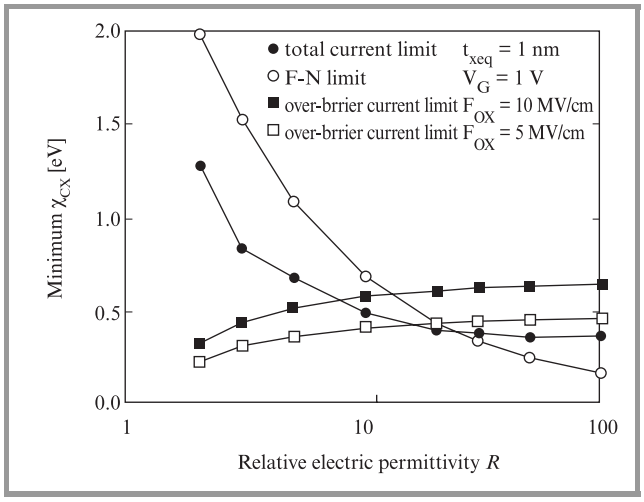


***Fig. 7.*** The minimum Si-dielectric electron affinity that ensures the flow of the same electron leakage current as in the case of $SiO_2$ layer.

Since, as was shown in the previous figures, in case of $TiO_2$ layers Fowler-Nordheim current dominates for this voltage, results obtained with analytical approximated condition for the Fowler-Nordheim current level conservation (see Appendix 1) are also presented. For comparison, results of analogous condition for the over-barrier current level conservation (see Appendix 2) are presented in the figure as well. As seen in Fig. 5, this component becomes significant in the case of the $TiO_2$ layer with electric permittivity 80 for gate voltages smaller than 1 V.

## 4. Conclusions

The analysis presented in the work shows the contribution of different current components to the gate leakage current in best known high-$k$ dielectrics. In case of $Ta_2O_5$ layer the structure of this current is similar to the $SiO_2$ case with the Fowler-Nordheim component dominance for large gate voltages and direct tunneling component dominance for small gate voltages. Contrary to that, in $TiO_2$ case the direct tunneling component has practically no impact on the total current which is now determined by the Fowler-Nordheim component. Here, the over-barrier current component becomes significant for low gate voltages. Although the total current level is significantly lower than in $SiO_2$ case, the difference in the structure of this current may result in the breakdown and reliability behavior different than in $SiO_2$ case.

A minimum value of Si-dielectric electron affinity is limited to 0.4 eV for dielectrics with their electric permittivity as large as tens of $SiO_2$ electric permittivity. This limit results from the Fowler-Nordheim and over-barrier components of the gate current.

Finally, we wish to underline that there is still a need for more complex exploration of basic physical parameters of high-$k$ dielectrics. There is especially large uncertainty about Si electron affinity to those dielectrics as well as their electron effective masses. In the gate leakage current analyses these parameters are as important as the electron permittivity. Their better knowledge will help to eliminate some materials, or to propose new ones, before spending a lot of money and time on technological experiments.

## Appendix 1. Fowler-Nordheim tunneling

Fowler-Nordheim tunneling is given by the following formula

$$J_x = A_x F_x^2 \exp\left(-C_x \frac{\chi_{cx}^{3/2}}{F_x}\right), \tag{8}$$

where $A_x$ and $C_x$ are constants depending on an electron effective mass in a given insulator and $A_x$ depends additionally on the Si-insulator electron affinity $\chi_{cx}$. If we consider only the exponential factor, the following condition must be fulfilled to preserve the constant value of the F-N current

$$C_x \frac{\chi_{cx}^{3/2}}{F_x} = C_{ox} \frac{\chi_{cox}^{3/2}}{F_{ox}}. \tag{9}$$

Under assumption that both the gate voltage and the semiconductor voltage drop remain unchanged

$$V_x = F_x t_x = V_{ox} = F_{ox} t_{ox}, \tag{10}$$

where $V_{ox}$ is the voltage drop on the $SiO_2$ layer.
Then

$$F_x = \frac{F_{ox}}{R}. \tag{11}$$

Taking advantage of Eqs. (1), (9) and (11) we get

$$\chi_{cx}^{3/2} = \frac{\chi_{cox}^{3/2}}{R} \tag{12}$$

and consequently

$$\chi_{cox} - \chi_{cx} \leq \left(1 - R^{-2/3}\right) \chi_{cox}. \tag{13}$$

# Appendix 2. The over-barrier current

The over-barrier current is given by the following formula

$$J_x = A_x T^2 \exp\left(-q\,\frac{\chi_{cx} - \sqrt{\frac{qF_x}{4\pi\varepsilon_x}}}{k_B T}\right), \tag{14}$$

where $T$ is the absolute temperature, $k_B$ is the Boltzmann constant and $A_x$ is the Richardson constant. Similarly to the F-N case we consider only the exponential factor

$$\chi_{cx} - \sqrt{\frac{qF_x}{4\pi\varepsilon_x}} = \chi_{cox} - \sqrt{\frac{qF_{ox}}{4\pi\varepsilon_{ox}}}. \tag{15}$$

Then, according to Eqs. (2) and (11)

$$\chi_{cox} - \chi_{cx} = \sqrt{\frac{qF_{ox}}{4\pi\varepsilon_{ox}}} - \sqrt{\frac{qF_{ox}}{4\pi R^2\varepsilon_{ox}}} \tag{16}$$

and finally

$$\chi_{cox} - \chi_{cx} = \sqrt{\frac{qF_{ox}}{4\pi\varepsilon_{ox}}}\left(1 - \frac{1}{R}\right). \tag{17}$$

Since $\varepsilon_{ox} = 3.45 \cdot 10^{-13}$ F/cm:

$$\chi_{cox} - \chi_{cx} \le 0.2\sqrt{F_{ox}\,[\mathrm{MV/cm}]}\left(1 - \frac{1}{R}\right)\ [\mathrm{eV}], \tag{18}$$

which for $R > 10$ gives

$$\chi_{cox} - \chi_{cx} \le 0.2\sqrt{F_{ox}\,[\mathrm{MV/cm}]}\ [\mathrm{eV}]. \tag{19}$$

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**Andrzej Jakubowski** – for biography, see this issue, p. 33.

Paper

# Reliability of MIS transistors with plasma deposited $Al_2O_3$ gate dielectric film

Jan Szmidt, Aleksander Werbowy, Emil Dusiński, and Krzysztof Zdunek

**Abstract — The paper presents the parameters of MIS transistors with plasma deposited thin film aluminum oxide gate insulator. $Al_2O_3$ films were synthesized by means of the low-energy, low-temperature reactive pulse plasma (RPP) method. Investigated transistors, with channel width to length (*W/L*) ratios of 200/10 [$\mu$m/$\mu$m] and 200/20 [$\mu$m/$\mu$m] were manufactured in a standard microelectronic technological laboratory. In order to determine the most important parameters of produced devices there were measured their electrical characteristics. The distribution of the threshold voltage values was studied on a representative set of over two hundred structures.**

***Keywords — MIS transistor, reliability, $Al_2O_3$ films, RPP method.***

## 1. Introduction

Dielectric films perform various functions in MIS devices. They are used as: semiconductor surface passivation layers, masks in ion diffusion processes, protective layers against environment and electric isolation in some areas of MIS structures. In this paper, we would like to present the results of investigation of the performance of MIS transistors with aluminum oxide $Al_2O_3$ dielectric film playing the role of the gate insulator. Since the properties of gate insulator substantially determine the electrical characteristics of transistors, fabrication technology of dielectric films must ensure their highest quality. Currently the basic semiconductor materials are silicon (Si) and its natural dielectric – silicon dioxide ($SiO_2$). However, besides well-known advantages, $SiO_2$ has also certain shortcomings, among which the most important are:

1) easiness of ion and impurity migration, particularly at elevated temperatures and strong electric fields;
2) low radiation resistance.

Under certain circumstances, these features may result in instability of parameters of Si-$SiO_2$ structures and in effect – in instability of their electrical characteristics. Therefore, one can observe a growing interest in alternative dielectric materials, among which is aluminum oxide. Today $Al_2O_3$ is the third (after $SiO_2$ and $Si_3N_4$) most explored and simultaneously very promising dielectric material. As compared to $SiO_2$, aluminum oxide is characterized by much lower ion and impurity migration, is more radiation resistant [1] (it can be used in nuclear medicine and aerospace applications), shows higher dielectric constant value and its technology is less complicated. $Al_2O_3$ has been investigated at least since the late 60-ties [2], mainly as the one of insulating films in nonvolatile memories (in MAOS devices) [3]. Now electronics again is witnessing a comeback of the interest in this material. Primarily, because its dielectric constant value ($7.5 \div 9$) is higher than that of $SiO_2$ ($3.5 \div 4.3$) what is very attractive from the point of view of advanced MIS devices (like for instance DRAM structures). Moreover, $Al_2O_3$ has a large bandgap width (9.5 eV) which makes it very promising dielectric material for wide bandgap semiconductors (such as SiC, GaN or diamond), particularly in heterojunction bipolar transistor (HBT) structures and high-power and high-temperature electronic devices. Finally, the renaissance of the interest in $Al_2O_3$ can be also to some extent attributed to very dynamic development of its deposition methods, particularly the plasma-based ones. These techniques, in general, enable obtaining (at low-temperature and low-energy conditions) of sufficiently pure and stoichiometric dielectric layers.

Table 1
Properties of $SiO_2$, $Si_3N_4$ and $Al_2O_3$ films

| Parameter | Material | | |
|---|---|---|---|
| | $SiO_2$ | $Si_3N_4$ | $Al_2O_3$ |
| Energy gap $E_G$ [eV] | 8.5 | 5.1 | 9.5 |
| Density [g/cm$^3$] | $1.8 \div 2.4$ | $3.0 \div 3.2$ | $3.43 \div 3.9$ |
| Dielectric constant | $3.5 \div 4.3$ | $4.8 \div 7.4$ | $7.0 \div 9.0$ |
| Resistivity [$\Omega$cm] | $10^{12} \div 10^{17}$ | $10^{13} \div 10^{15}$ | $10^{11} \div 10^{16}$ |
| Dielectric strength [V/cm] | $1 \div 20 \cdot 10^6$ | $10^7$ | $2 \div 12 \cdot 10^6$ |
| Thermal coefficient of linear expansion $k$ $[10^{-6}\mathrm{K}^{-1}]$ | 0.5 | $2 \div 4$ | 8 |
| Refractive index $n$ | $1.32 \div 1.5$ | $1.95 \div 2.05$ | $1.55 \div 1.8$ |

Unfortunately, aluminum oxide has also a few disadvantages. Perhaps the most important is its large thermal coefficient of linear expansion with respect to Si. It makes that $Al_2O_3$ films cannot be used in situations when the gradient of the temperature during technological processes or during device operation is changing, what practically occurs usually. However, from the point of view of wide bandgap semiconductors this problem is less critical, as their thermal coefficients of linear expansion $k$ are higher as well (e.g.

for SiC $k \geq 4 \cdot 10^{-6}$ [$K^{-1}$], for GaN $\geq 5.6 \cdot 10^{-6}$ [$K^{-1}$] whereas for $SiO_2$ $k = 0.5 \cdot 10^{-6}$ [$K^{-1}$]).
For all these reasons, in certain applications $Al_2O_3$ may be seriously considered an alternative to $SiO_2$. Table 1 shows a comparison of the most important properties of $SiO_2$, $Si_3N_4$ and $Al_2O_3$ dielectric films.

## 2. Experimental details

As substrates, there were used Si p-type $<100>$ $8.7 \div 9.8$ Ωcm wafers. Prior to $Al_2O_3$ deposition process they were chemically cleaned according to the standard procedure, consisting of the following steps:

- preliminary cleaning in a solution of hydrogen dioxide and sulfuric acid $H_2O_2$ + $H_2SO_4$ mixed at the ratio1:2,
- removal of organic impurities in a mixture of $H_2O$ + $NH_4OH$ + $H_2O_2$ (5:1:1),
- removal of thin silicon dioxide layer in a mixture of HF + $H_2O$ (1:50),
- removal of other impurities in a mixture of $H_2O$ + HCl + $H_2O_2$ (6:1:1).

Aluminum oxide films were obtained by means of reactive-pulse-plasma technique [4]. Characteristic of this method is the specific way of plasma generation. It is induced at room temperature in a coaxial accelerator by electrical impulses of controlled frequency and voltage, what results in formation of small crystallites of synthesized material, which subsequently are being „frozen" on the substrate's surface. In the case of $Al_2O_3$ films deposition, the Al source is an aluminum internal electrode and alundum bushing. The plasma-generating gas is oxygen ($O_2$) [5]. In order to ensure a higher uniformity of produced layers, during the deposition process the substrates are kept on a rotation table. The process parameters are presented in Table 2.

Table 2
Technological parameters of $Al_2O_3$ films synthesis process (RPP method)

| Parameter | Value |
|---|---|
| Pressure [Pa] | 40 |
| Temperature [°C] | $< 150$ |
| Plasma-generating gas | $O_2$ |
| Voltage [kV] | 3.5 |
| Number of plasma impulses | 2000 |
| Frequency [Hz] | 0.2 |

After deposition, the thickness and refractive index of $Al_2O_3$ film was measured ellipsometrically (Gaertner L116). Other technological processes (photolithography I, etching of $Al_2O_3$ film, diffusion of phosphorus, aluminum metallization, photolithography II) were carried out in a clean-room standard technological laboratory. It is worth noting, that aluminum oxide dielectric films can be efficiently and selectively etched in a buffer of hydrofluoric acid (Fig. 1).

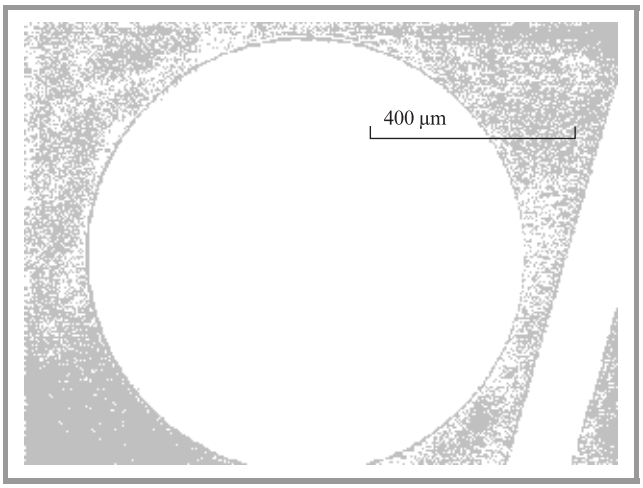


***Fig. 1.*** $Al_2O_3$ film etched in HF buffer.

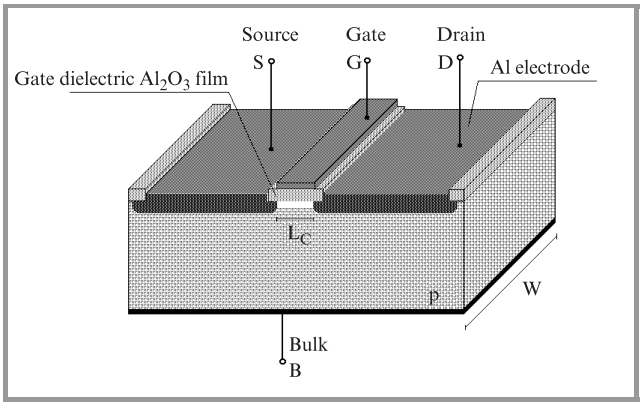


***Fig. 2.*** The structure of investigated MIS transistor.

As a result of the processes mentioned above, on several wafers there were obtained chips containing transistors (Fig. 2) with varying channel dimensions. Under the same technological conditions and on the identical Si substrates there was also produced a number of simple MIS capacitor test structures with $Al_2O_3$ dielectric layers and metal (Al) dot contacts (each of 0.75 mm diameter). Measurements of their electrical characteristics as well as measurements of transient and output electrical characteristics of 211 transistors enabled extraction and analysis of some of the most important parameters of produced structures.

## 3. Results and discussion

Obtained $Al_2O_3$ dielectric films had mixed amorphous-nanocrystalline structure with predominant $\gamma$ – type phase of aluminum oxide [5]. Measurements of electrical characteristics of MIS capacitors allowed extraction of some

parameters of investigated material (dielectric constant $\varepsilon_{ri}$, effective charge $Q_{eff}$, resistivity $\rho$ and interface trap density $D_{it}$ – see Table 3) from well-known relationships:

$$\varepsilon_{ri} = \frac{C_{\max} t_i}{\varepsilon_0 A} , \tag{1}$$

where $C_{\max}$ is the capacitance of a MIS structure in accumulation, $t_i$ is dielectric film thickness and $A$ denotes the gate area of a MIS structure (in our case $A = 4.42 \cdot 10^{-3}$ cm$^2$);

$$Q_{eff} = \frac{\varepsilon_{ri} \left(\varphi_{MS} - U_{FB}\right)}{t_i} , \tag{2}$$

where $\varphi_{MS}$ is the work-function difference (as the Si substrates and Al gate electrodes were used, the $\varphi_{MS}$ was assumed to be equal to – 0.6 – $\varphi_F$) whereas $U_{FB}$ denotes the flat band voltage of MIS structure;

$$\rho\,|_{U=\text{const}} = \frac{UA}{It_i} . \tag{3}$$

Table 3
Properties of produced $Al_2O_3$ films

| Parameter | Value |
|---|---|
| Thickness $t_{ox}$ [nm] | 317 |
| Refractive index $n$ | 1.6 |
| Dielectric constant $\varepsilon_{ri}$ | $4.8 \div 11.8$ |
| Effective charge $Q_{eff}$ [C/cm$^2$] | $1.76 \cdot 10^{-7}$ |
| Resistivity $\rho$ [$\Omega$cm] | $\sim 10^9$ |
| Interface trap density $D_{it}$ [eV$^{-1}$cm$^{-2}$] | $2.62 \cdot 10^{12}$ |

Interface trap density $D_{it}$ was estimated by means of simplified version of so-called Terman method, proposed in [6], which allows determining $D_{it}$ in the middle-band voltage state of MIS structure.

Output conductances $g_D$, transconductances $g_m$, threshold voltage values $V_{TH}$ of the obtained MIS transistors as well as the mean yield for the whole batch were extracted from the measurements of their transient and output characteristics.

Figures $3 \div 6$ show the electrical characteristics and conductances of the investigated structures. As it can be seen, in general they do not depart in character from the curves usually observed for typical MOS transistor structures. The value of transconductance $g_m$ (Fig. 4) is quite high and in accord with the theory. Note that characteristics presented in Fig. 4 are the extreme ones, what demonstrates relatively small scattering of all measured curves. Similar remarks apply to observed output conductance $g_D$ characteristics (Fig. 6). Thus, the basic parameters of the MIS transistor with plasma deposited $Al_2O_3$ films can be considered satisfactory.

Another problem analysed was the quality of obtained transistors. Characteristic of the RPP process is step-like (pulse) film growth. Additionally, the propagation of plasma has also a certain influence on the film thickness and quality, which both depend on the distance between the electrodes and the substrate. In order to ensure the better

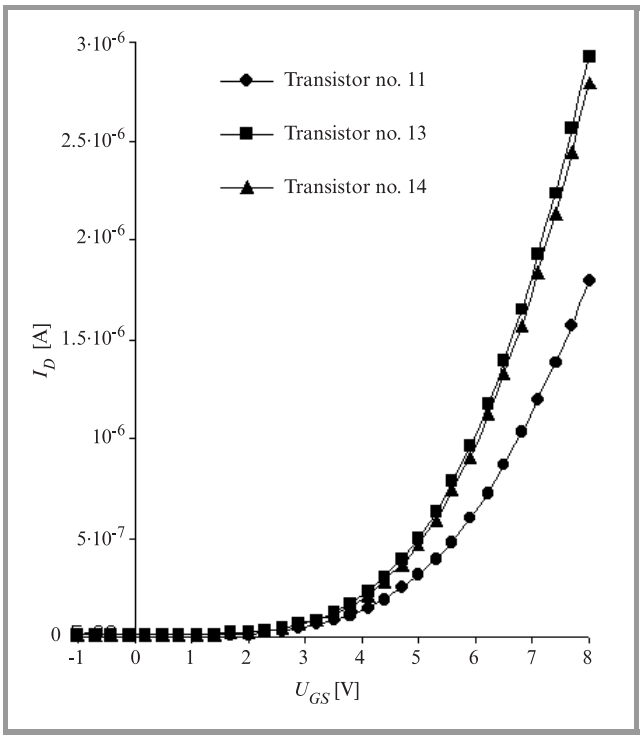


***Fig. 3.*** Transient $I_D = f(U_{GS})$ characteristics of investigated MIS transistors.

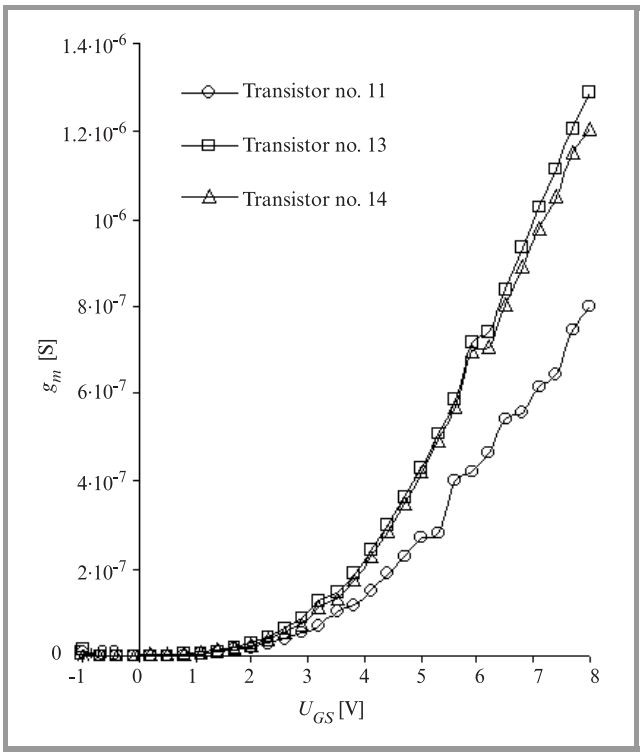


***Fig. 4.*** Transconductance $g_m = f(U_{GS})$ characteristics of investigated MIS transistors.

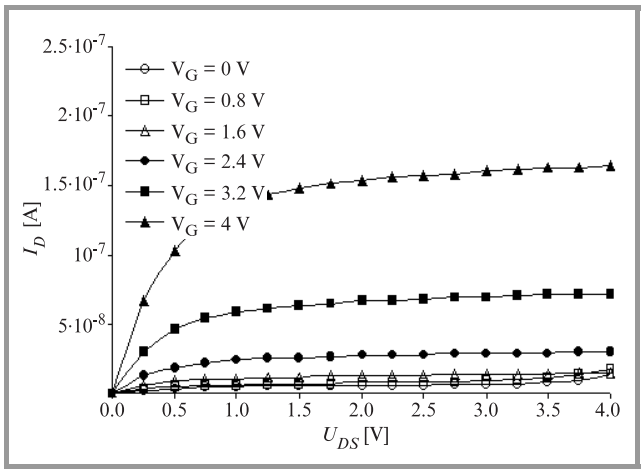


***Fig. 5.*** Output $I_D = f(U_{DS})$ characteristics of investigated MIS transistors.

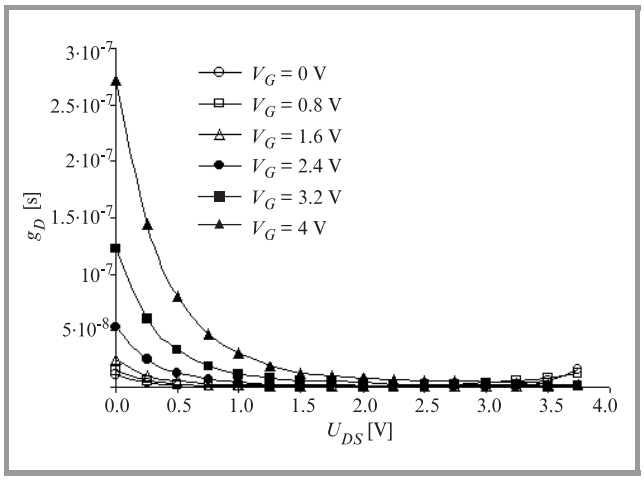


***Fig. 6.*** Conductance $g_D = f(U_{DS})$ characteristics of investigated MIS transistors.

quality of layers and higher homogeneity of their thickness, the rotation table was used. The distribution of transistor threshold voltage $V_{TH}$ values was assumed to be the determinant of the homogeneity of the electrical properties of investigated devices. Corresponding results are shown in Figs. $7 \div 9$. The histogram in Fig. 7 shows typical distribution of $V_{TH}$ values. It has well-marked maximum around $2.5 \div 3$ V. Obviously, the situation pictured in this figure leaves much to be desired, especially because of the considerable scatter of results. Undoubtedly, more accurate adjusting of the technological process parameters might bring the substantial improvement here.

3D and 2D distribution maps of the $V_{TH}$ values variation over the surface show that despite substrate's rotation during $Al_2O_3$ deposition process there are observed dramatic changes in $V_{TH}$ even between neighboring transistors. On the other hand, especially in the central part of the wafer there are relatively large areas with structures of similar threshold voltage values ($V_{TH}$ variations visible in the vicinity of the substrate's border can be considered a fringe effect). All these effect, most likely should be attributed to the lack of structural uniformity of produced layers, what certainly indicates the necessity of some improvements in technology (e.g. changing of wafers rotation rate etc.). But this task can be not that easy, as inhomogeneity of the material structure is closely associated with the very nature of the applied plasma-chemical processes. Relationships between plasma properties and particularly between its homogeneity, chemical reactions occurring in such environment and homogeneity of deposited film are very difficult to be grasped and modeled. So far, it has not been a very important problem, but there is no doubt that it will be.

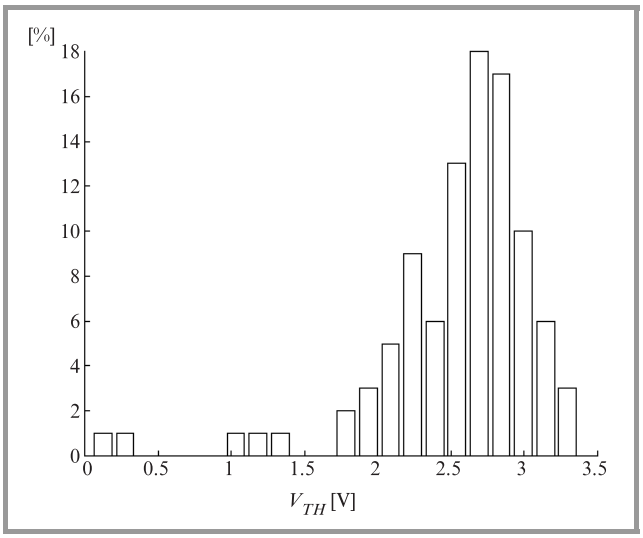


***Fig. 7.*** Histogram of the threshold voltage $V_{TH}$ values (for measured 107 transistors with 200/20 $W/L$ ratio).

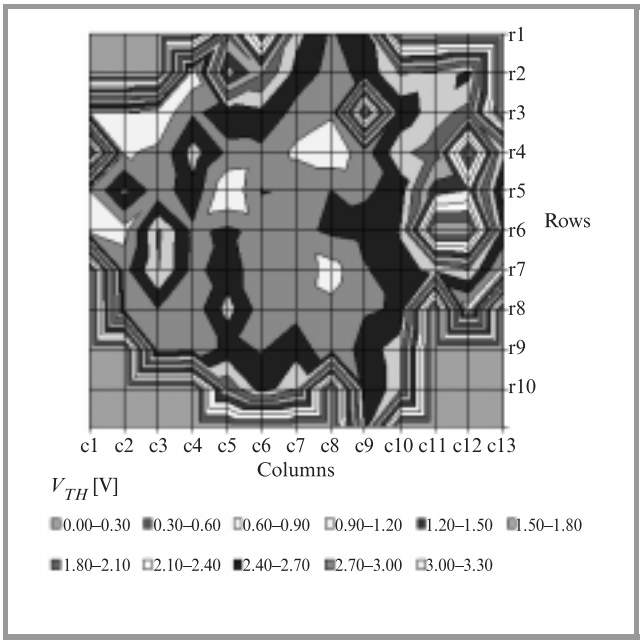


***Fig. 8.*** 3D distribution map of the threshold voltage $V_{TH}$ value variations over the substrate's surface.

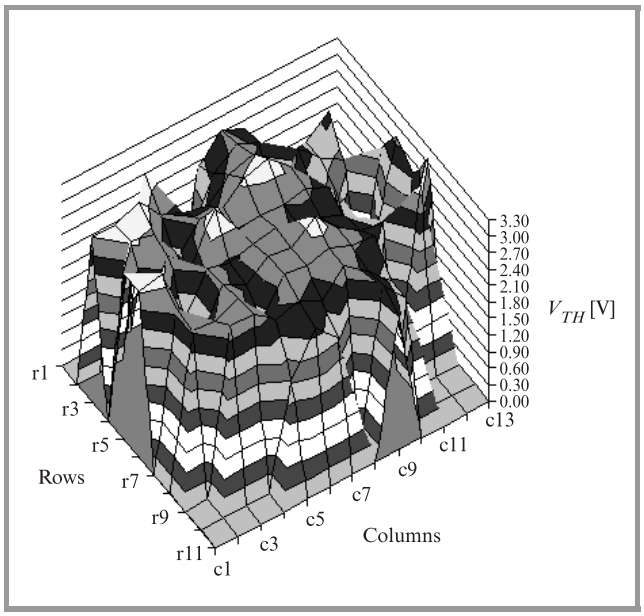


***Fig. 9.*** 2D distribution map of the threshold voltage $V_{TH}$ value variations over the substrate's surface.

It is also worth noting that the yield of the whole batch of investigated transistors was 73%. It is very promising result, indicating that the RPP technique can be applied to fabrication of that kind of electronic structures.
To sum up, it should be stated that as for the present stage of the research on $Al_2O_3$ gate dielectric films, the obtained results are quite satisfactory. However, the practical application of this material requires further improvement of the deposition process and better understanding of some fundamental issues related to the physics and chemistry of used technology.

# 4. Conclusions

After measuring of 211 MIS transistors with plasma deposited $Al_2O_3$ films (104 pcs with $W/L$ ratio = = 200/10 [$\mu$m/$\mu$m] and 107 pcs with $W/L$ ratio = = 200/20 [$\mu$m/$\mu$m]), we found that:

1) fabricated transistors have reproducible electrical characteristics (Figs. 3 and 5) and $Al_2O_3$ films show satisfactory properties and parameters (Table 3);

2) $Al_2O_3$ films can be selectively etched in HF buffer (there also exists possibility of their selective removal by means of so-called „lift off" process);

3) examined MIS transistors with $Al_2O_3$ films show satisfactory values of $V_{TH}$, $g_m$ and $g_D$ parameters (Figs. 4, 6 and 7);

4) as for the present stage of the technology development the distribution of the threshold voltage $V_{TH}$ values is acceptable;

5) though a certain number of produced transistors did not work, the mean yield for the whole batch was 73%.

# Acknowledgements

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Paper

# Metastability problems in amorphous silicon

Stanisław M. Pietruszko and Marek Kostana

**Abstract — The results of study of the influence of boron and phosphorous doping and hydrogen content on transport properties and thermally induced metastability of LPCVD a-Si are reported. The thermally induced metastability has been observed in both unhydrogenated and hydrogenated P-doped a-Si films. Metastability is a barrier for wide application of a-Si such solar cells. In this paper we report our studies on the effect of thermally induced metastability in LPCVD a-Si as a function of implanted boron and phosphorous concentration. We have investigated films unhydrogenated and hydrogenated by ion implantation. The results are qualitatively agreed with bond breaking model.**

***Keywords — amorphous silicon, metastability, thermal quenching.***

## 1. Introduction

Amorphous silicon and its alloys, due to their physical properties and their manufacturability, have attracted rapidly growing interest in the recent years. A major advantage of amorphous over crystalline technology is dramatically reduced cost so low that some consumer applications like solar cells, thin film transistors, etc. Solar cells are applied in telecommunication for supply electricity for base stations far away from electric grid. However, the performance of a-Si-based devices is limited by reversible, metastable changes induced by light, high-energy particles, carrier injection, the accumulation of carriers at a-Si interfaces, and thermal quenching [1]. All of these effects are reversible by annealing to a sufficiently high temperature, and all are believed to be caused by the same degradation mechanism [2].

Since the discovery of metastable effects in a-Si:H, there is strong circumstantial evidence for the role of hydrogen and dopants, although complete proof is still lacking. The evidence stems primarily from the observation of hydrogen motion at the same temperature as the metastability effects. The activation energy of defect annealing is comparable with that of hydrogen diffusion. Furthermore, the doping trends are the same – dopants which result in a large hydrogen diffusion coefficient also lead to faster defect relaxation. In the other hand hydrogen makes doping possible by passivating large number of dangling bond defects caused by bonding disorder.

Kind and magnitude of metastable changes is dependent on both hydrogen and dopant such phosphorous or boron. In doped hydrogenated amorphous silicon, there are coexistence of two different phenomena: the reversible increase of dangling bonds density and the reversible increase of doping efficiency. These effects depend on the kind of excitation applied to a film (light soaking, rapid cooling, or bias), and on the doping level, and the type of dopant. Therefore it is important to study influence of hydrogen and dopants on metastability in amorphous silicon to understand reasons of metastable phenomena.

There are several barriers to the study of metastability in low-hydrogen-concentration a-Si. Most a-Si is grown from hydrogen-bearing precursor gases, and hydrogen content is difficult to reduce to below a few atomic percent. Implantation of hydrogen to LPCVD a-Si films with very low hydrogen content (0.06 at.% H) allowed us to investigate films with low and high hydrogen content. In this paper we report our studies of effect of rapid quenching in LPCVD a-Si unhydrogenated films and hydrogenated as a function of phosphorous concentration. Variation of P concentration over five orders of magnitude with different hydrogen contents help us examine the role of dopant in metastability phenomenon.

## 2. Experimental

LPCVD a-Si films (0.5 $\mu$m thick) are grown on oxidised crystalline silicon substrate at 560°C. As-grown, undoped films contain $\sim 0.06$ at.% hydrogen (SIMS) and spin density is $10^{19}$ cm$^{-3}$ (ESR). These films are phosphorous or boron doped by ion implantation (different doses from $10^{11}$ to $10^{17}$ ions/cm$^2$ at 150 keV). The average doping concentration, given by the ratio of the implanted dose to the amorphous film thickness, is from $2 \cdot 10^{15}$ to $2 \cdot 10^{21}$ cm$^{-3}$. One set of films was further implanted with hydrogen doses corresponding to 12 at.% of hydrogen content. Ion implantation was done at three energies 25, 40, 60 keV to ensure uniform distribution. Further, films were annealed at 400°C for 20 hours in nitrogen atmosphere. It was possible since FTIR measurements showed, that hydrogen starts effuse from these samples only after annealing at 425°C for 2 hours. The slow cooling and quenching were done after annealing for one hour at 400°C. The conductivity measurements are done in coplanar geometry using aluminium electrodes 0.1 mm apart. Dark conductivity versus reciprocal temperature is measured from 300 to 590 K with a heating rate of 1.5 K/min. More details about conductivity measurements and quenching are given elsewhere [3]. The activation energies, $E_A$ were determined from the slope of the least square fit of the data to $\sigma = \sigma_0 \exp(-E_A/kT)$.

## 3. Results

Figures 1 and 2 show the logarithm of conductivity versus reciprocal temperature (1000/T) of hydrogenated a-Si films

(12 at.%) with different boron and phosphorous concentrations after slow cooling (filled points) and quenching (open points). The curves shifted for clarity. The metastability effect and its dependence on dopants doses can be clearly seen.

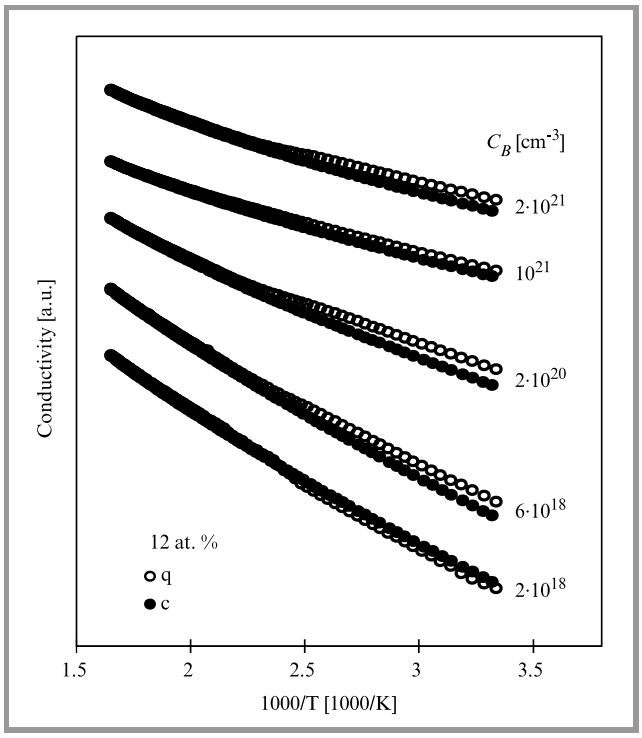


***Fig. 1.*** The logarithm of conductivity versus reciprocal temperature of hydrogenated a-Si films (12 at.%) with different boron concentration after slow cooling (filled points) and quenching (open points). The curves shifted for clarity.

The room temperature dark conductivity, $\sigma_{300}$, of as-grown films (0.06 at.% H) is about $1\cdot10^{-6}\Omega^{-1}\text{cm}^{-1}$ (Fig. 3) and remains constant up to phosphorous concentration $6\cdot10^{19}$ cm$^{-3}$, then increases to $8\cdot10^{-2}$ for the highest P concentration ($2\cdot10^{21}$ cm$^{-3}$). In the case of boron doped films $\sigma_{300}$ remains constant up to boron concentration $2\cdot10^{17}$ cm$^{-3}$ then decrease to $10^{-8}\Omega^{-1}$ cm$^{-1}$ for $C_B = 2\cdot10^{18}$ cm$^{-3}$ and further increase to $10^{-2}\Omega^{-1}$ cm$^{-1}$ for highest boron concentration ($2\cdot10^{21}$ cm$^{-3}$). Since $\sigma_{300}$ begins increasing for phosphorous and boron concentration which is approximately equal to the measured spin density of $10^{19}$ cm$^{-3}$, we suggest that dopants passivates dangling bonds in unhydrogenated material. When most of them are passivated, phosphorous or boron atoms become active dopant. Existence of minimum of conductivity for $C_B = 2\cdot10^{18}$ cm$^{-3}$ suggest that in such doped films Fermi level is located in half of mobility gap. In the case of hydrogenated ($C_H$ = 12 at.%) films, room temperature dark conductivity $3\cdot10^{-9}$ for lowest concentration of phosphorous slowly increases to $10^{-2}\Omega^{-1}$ cm$^{-1}$ for the highest P concentration. Similarly for B doped films $\sigma_{300}$ increase from $2\cdot10^{-8}\Omega^{-1}$ cm$^{-1}$ to $10^{-3}\Omega^{-1}$ cm$^{-1}$ with increasing of $C_B$ in the range of $2\cdot10^{18}\div2\cdot10^{21}$ cm$^{-3}$,

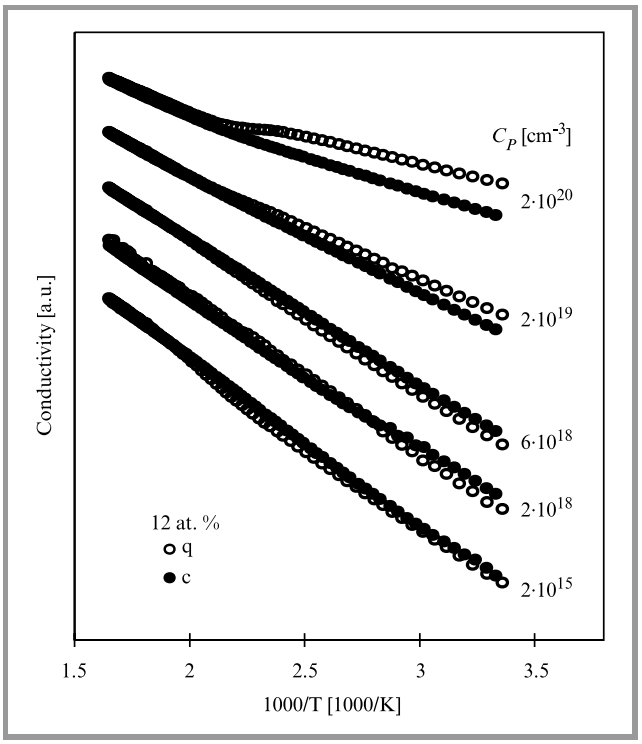


***Fig. 2.*** The logarithm of conductivity versus reciprocal temperature of hydrogenated a-Si films (12 at.%) with different phosphorous concentration after slow cooling (filled points) and quenching (open points). The curves shifted for clarity.

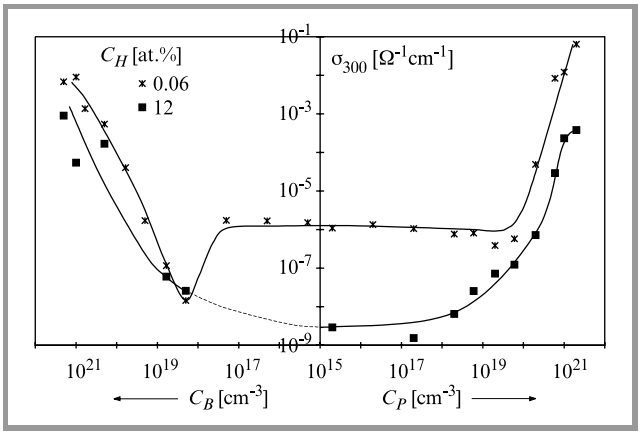


***Fig. 3.*** The room temperature dark conductivity, $\sigma_{300}$ versus phosphorous and boron concentration of unhydrogenated and hydrogenated (12 at.%) a-Si films.

but we do not know how it changes for low boron concentration (up to $2\cdot10^{18}$). Significant difference in room temperature conductivity between films unhydrogenated and hydrogenated films for same dopant concentration above $6\cdot10^{19}$ cm$^{-3}$ suggests that hydrogen passivated dangling bonds of a-Si network, so the conductivity decreased to the level comparable with glow discharge a-Si films. We suggest that it can be connected with deactivation of dopants by hydrogen [3].

The activation energy, $E_A$ is shown in Fig. 4. For unhydrogenated films, $E_A$ is in order of 0.2 eV and remains constant up to P concentration of $10^{19}$ cm$^{-3}$, then it jumps to 0.6 eV for P concentration of $2 \cdot 10^{19}$ cm$^{-3}$ (what corresponds to increase of $\sigma_{RT300}$), and decreases to 0.2 eV for the highest phosphorous concentration. In the case of boron doped films $E_A$ change similarly but jump is smaller, from 0.2 eV to 0.35 eV for $C_B = 2 \cdot 10^{19}$ cm$^{-3}$. We suggest that there is change of mechanism of carrier transport at the room temperature for the dopant concentration higher that spin density in as-grown films ($10^{19}$ cm$^{-3}$). For hydrogenated films is about 0.65 eV for lowest P concentration and remains constant up to $6 \cdot 10^{18}$ cm$^{-3}$, then activation energy $E_A$ decreases to 0.25 eV for the highest P concentration. In the case of boron doped films $E_A$ decrease from 0.6 eV to 0.27 eV with increasing of B concentration from $2 \cdot 10^{18}$ cm$^{-3}$ up to $2 \cdot 10^{21}$ cm$^{-3}$. The dependence of the activation energy on dopant concentration is correlated with the dependence of the room temperature dark conductivity. Again, the suggested the passivation of dopants by hydrogen can be seen.

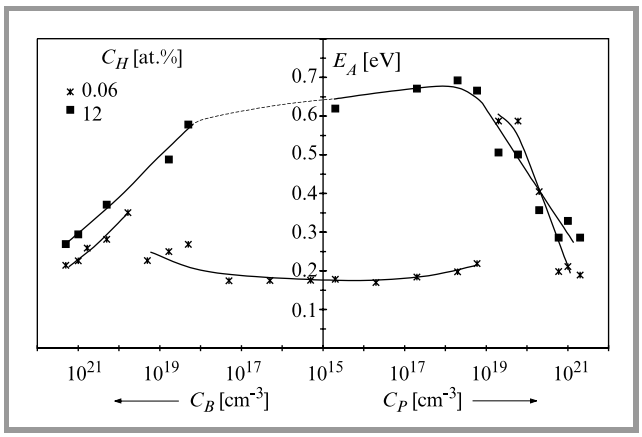


***Fig. 4.*** The activation energy, $E_A$ versus phosphorous and boron concentration of unhydrogenated and hydrogenated (12 at.%) a-Si.

The dependence of the ratio of room temperature conductivity after quenching, $\sigma_{300q}$ and after slow cooling, $\sigma_{300c}$ as a function of dopant content is shown in Fig. 5. In the case of unhydrogenated films the ratio of $\sigma_{300q}/\sigma_{300c}$ is about 1 up to P concentration $6 \cdot 10^{18}$ cm$^{-3}$ and up to B concentration $2 \cdot 10^{19}$ cm$^{-3}$. Then increases to 2.4 and 2 for $C_P = 10^{20}$ cm$^{-3}$ and $C_B = 10^{20}$ cm$^{-3}$, respectively. Further increasing of dopant concentration causes decreasing of the ratio of $\sigma_{300q}/\sigma_{300c}$. In the case of hydrogenated (12 at.%) films the ratio of $\sigma_{300q}/\sigma_{300c}$ is below 1 up to P concentration $6 \cdot 10^{18}$ cm$^{-3}$ and up to B concentration $2 \cdot 10^{18}$ cm$^{-3}$. Then increases to 4 and 3 for $C_P = 10^{20}$ cm$^{-3}$ and $C_B = 2 \cdot 10^{20}$ cm$^{-3}$, respectively. Further increasing of dopant concentration causes decreasing of the ratio of $\sigma_{300q}/\sigma_{300c}$.

Similar trends are observed in difference between the activation energy after slow cooling and quenching, $\Delta E_A$ (Fig. 6) which is between -30 and 0 meV up to $C_P = 2 \cdot 10^{-19}$ cm$^{-3}$ and $C_B = 2 \cdot 10^{-19}$ cm$^{-3}$. Further increasing of dopant concentration causes increasing of $\Delta E_A$ to 40 meV and 20 meV for $C_P = 2 \cdot 10^{20}$ cm$^{-3}$ and $C_B = 2 \cdot 10^{20}$ cm$^{-3}$, respectively. $\Delta E_A$ decrease for higher dopant concentration. In the case of hydrogenated (12 at.%) films in difference between the activation energy after slow cooling and quenching decrease from 60 meV to 10 meV and from 50 meV to 20 meV with increasing of $C_P$ from $2 \cdot 10^{18}$ cm$^{-3}$ to $10^{21}$ cm$^{-3}$ and $C_B$ from $2 \cdot 10^{20}$ cm$^{-3}$ to $10^{21}$ cm$^{-3}$, respectively. Behavior of $\Delta E_A$ in these films with lower dopant concentration is not clear.

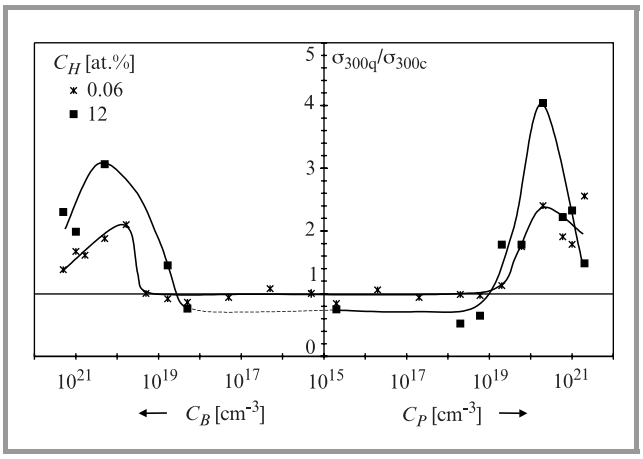


***Fig. 5.*** The ratio of room temperature dark conductivity versus phosphorous and boron concentration of unhydrogenated and hydrogenated (12 at.%) a-Si films.

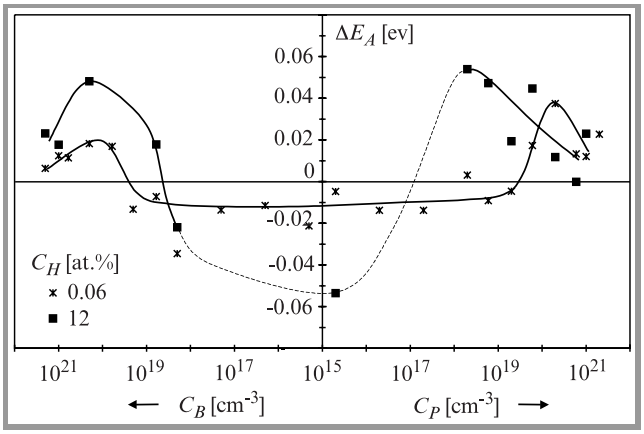


***Fig. 6.*** Difference between the activation energy after slow cooling and quenching versus phosphorous and boron concentration of unhydrogenated and hydrogenated (12 at.%) a-Si films.

# 4. Conclusion

We have observed a reversible thermal induced metastable effect in LPCVD unhydrogenated and hydrogenated doped with different doses of phosphorous and boron amorphous silicon films. In unhydrogenated films metastable effects shows up above the concentration of dopant which is comparable to the spin density ($10^{19}$ cm$^{-3}$) in as-grown films.

Quenching causes increase of room temperature dark conductivity and decrease of low temperature activation energy. Magnitude of these changes increases with hydrogen content. In hydrogenated films, the thermally induced metastability can be seen for the low P and B concentration range; quenching causes decrease of room temperature dark conductivity and increase of low temperature activation energy. For the higher P concentrations changes in both parameters are opposite and rapidly increase with phosphorous concentration.

These results qualitatively agree with bond breaking model [4]. In this model excitation (light, quenching) causes breaking of bond Si-H. If a nearest neighbour of such bond is weak bond Si-Si it can lead to produce new dangling bond, and macroscopically to increase of dangling bond density. If a nearest neighbour of Si-H bond is an inactive atom of dopant, breaking of such bond can cause activate of this atom, and macroscopically lead to metastable increasing of doping efficiency. There is coexistence of these two effects. Which effect dominates depends on concentration of hydrogen and dopants.

In our unhydrogenated films there is no metastability up to $2 \cdot 10^{19}$ cm$^{-3}$ P concentration, but above this concentration dominate metastable increasing of doping efficiency. In hydrogenated films (12 at.%) up to P concentration $6 \cdot 10^{18}$ cm$^{-3}$ and B concentration $2 \cdot 10^{18}$ cm$^{-3}$ dominate creating of dangling bonds, then metastable increasing of doping efficiency. Decreasing of in difference between the activation energy after slow cooling and quenching and decreasing of the ratio of room temperature conductivity after quenching and after slow cooling with increasing of dopant concentration in highly doped films is difficult to explain and require further investigations.

## Acknowlegment

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*Regular paper*

# Implementation of the block cipher Rijndael using Altera FPGA

Piotr Mroczkowski

**Abstract — A short description of the block cipher Rijndael is presented. Hardware implementation by means of the FPGA (field programmable gate array) technology is evaluated. Implementation results compared with other hardware implementations are summarized.**

***Keywords — block cipher, Rijndael, Altera FPGA.***

## 1. Introduction

It has been announced recently that the cryptographic algorithm named Rijndael is the winner of the Advanced Encryption Standard competition. This international contest was organized by the National Institute of Standards and Technology. In September 1997, NIST opened a formal call for algorithms. A group of fifteen AES candidate algorithms were announced in August 1998. Next, all algorithms were subject to assessment process performed by various groups of cryptographic researchers throughout the world. In August 2000, NIST selected five algorithms: Mars, RC6, Rijndael, Serpent, Twofish as the final competitors. These algorithms were subject to further analysis prior to the selection of the best algorithm for the AES. Finally, on October 2, 2000, NIST announced that the Rijndael algorithm was the winner.

The primary criteria chosen by NIST to appoint the winner for the AES included security, efficiency in hardware and software, flexibility. The most important measure was the resistance against all known and unknown attacks, but after a thorough research it appeared that all algorithms considered in second phase were robust. The results of software implementation were also comparable. Under such circumstances the efficiency of hardware implementation seemed to be an important factor of the overall score.

Hardware implementations are designed and coded in hardware description language (for example AHDL – Altera hardware description language) and may be done using the FPGA devices. Altera's devices (FLEX 10K) consist of thousands of universal building blocks (called macrocells), dedicated memory blocks (called embedded array blocks – EABs) connected by means of programmable interconnectors. Block ciphers seem to fit extremely well the characteristics of the FPGAs. The fine-granularity of FPGA matches very well the operations required by block algorithms such as bit-permutations, bit-substitution, look-up table reads and boolean functions. The EABs are suitable for implementing large S-boxes (such as $8 \times 8$ S-boxes used in Rijndael).

## 2. Description of the Rijndael cipher

The Rijndael algorithm, which falls into the block cipher category, has been designed by Joan Daemen and Vincent Rijmen and its specification is given in [1].

The length of the block and the length of the key can be independently specified to 128, 192 and 256 bits. The structure of the variant of encryption algorithm with 128-bit length of the block and the key is presented in Fig. 1.

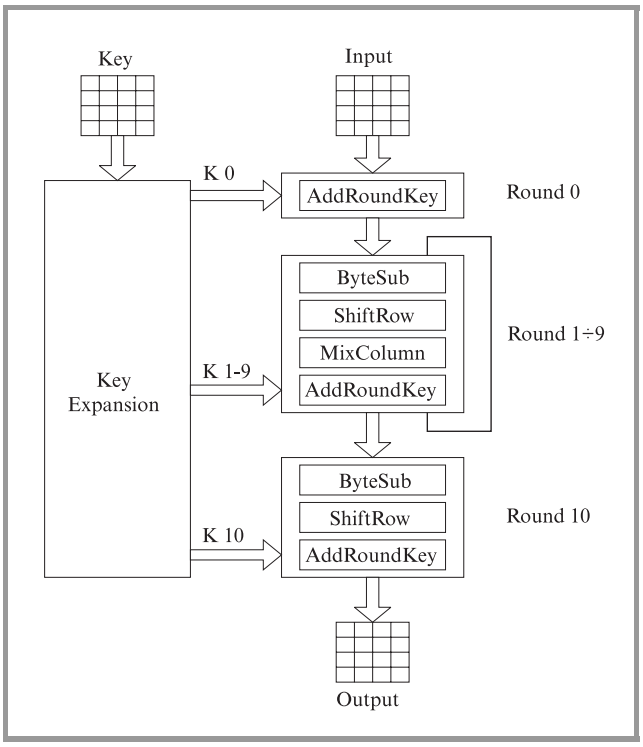


***Fig. 1.*** The encryption algorithm.

An input block of data and the intermediate cipher results are represented by a square matrix with $4 \times 4$ of byte dimension (so-called the state). The state is presented in Fig. 2.

The cipher input bytes are mapped onto the state bytes in the order $a_{0,0}$, $a_{1,0}$, $a_{2,0}$, $a_{3,0}$, $a_{1,0}$, $a_{1,1}$, $a_{1,2}$, $a_{1,3}$, ... At the end of the cipher operation, the cipher output is extracted from the state by taking the state bytes in the same order.

Every round except the initial (Round 0) and final (Round 10) ones consists of four transformations:

1. ByteSub – a single nonlinear transformation, which is applied to each byte of the data.

2. ShiftRow – which cyclically reorders the bytes of row.
3. MixColumn – a linear transformation applied to columns of the matrix.
4. AddRoundKey – which mixes the round key and the intermediate data.

Prior to the first round the transformation AddRoundKey is performed by using the main key as the round key (Round 0). Next, nine basic rounds (Round $1 \div 9$) consisted of all four transformations are performed. In the final round (Round 10) the transformation MixColumn is skipped.
The decryption algorithm with the 128-bit data and key option is presented in Fig. 3.

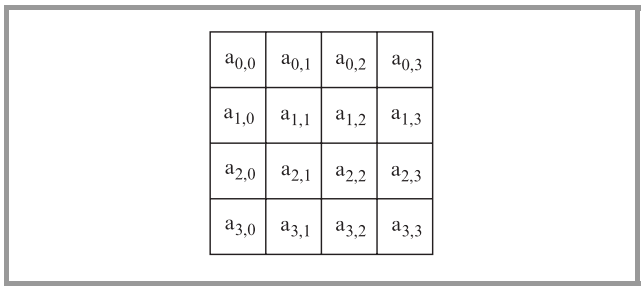


***Fig. 2.*** Example of the state.

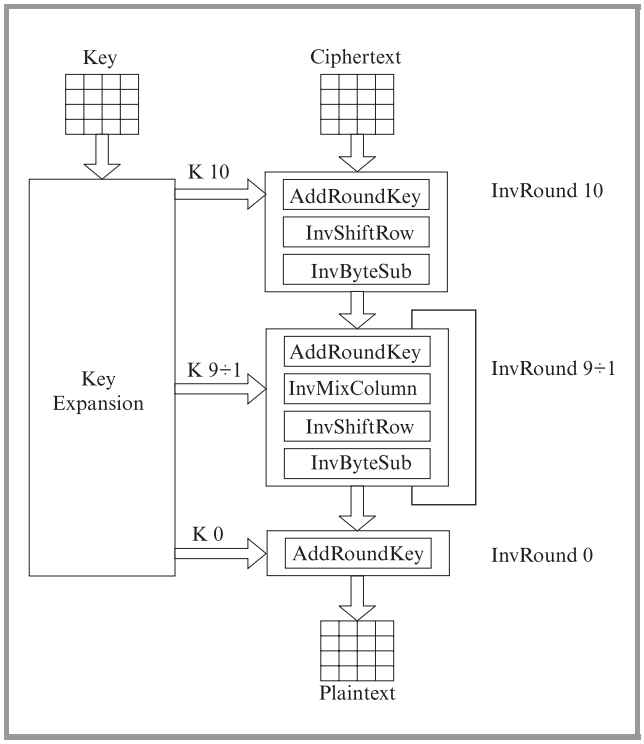


***Fig. 3.*** The decryption algorithm.

In the first step of the decryption algorithm the inversion of the final encryption round is performed (InvRound 10), next nine inversions of the basic encryption rounds (InvRound $9 \div 1$), and in the last step the transformation AddRoundKey is calculated (InvRound 0). In the decryption round all transformations of the encryption round are inverted in the reverse order.

### *2.1. ByteSub (InvByteSub) transformation*

The ByteSub transformation is the byte substitution, operating on each of the state bytes independently. Each byte is considered as representing coefficients of a polynomial of degree less then 8 over GF($2^8$). Firstly, we calculate the inversion of this polynomial modulo ($x^8 + x^4 + x^3 + x + 1$), then we multiply the result by a fixed matrix and add a fixed polynomial (an affine transformation). The affine transformation is defined by:

$$\begin{bmatrix} y_0 \\ y_1 \\ y_2 \\ y_3 \\ y_4 \\ y_5 \\ y_6 \\ y_7 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \times \begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \\ 0 \\ 1 \\ 1 \\ 0 \end{bmatrix}$$

The inversion and affine transformations create a substitution table (S-box).
The InvByteSub transformation is obtained by the inverse, affine mapping followed by taking the inversion over GF($2^8$).
The inverse affine transformation and inversion create an inverse substitution table (InvS-box).
The effect of the ByteSub (InvByteSub) transformation on the state is presented in Fig. 4.

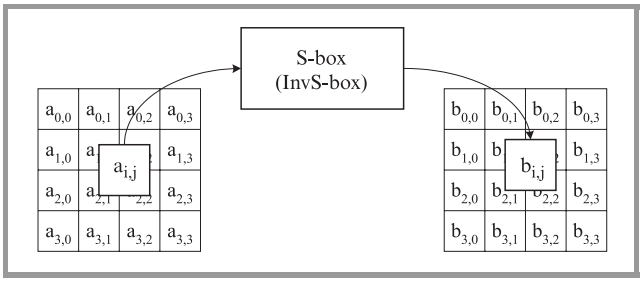


***Fig. 4.*** The ByteSub (InvByteSub) transformation.

### *2.2. ShiftRow (InvShiftRow) transformation*

In the ShiftRow transformation the bytes in the rows of the state are cyclically shifted over different offsets according to the following rule. Bytes in the first row are not shifted, in the second are shifted by 1 byte, in the third by 2 bytes, and in the last one by 3 bytes to the left (Fig. 5).
In the InvShiftRow, bytes in the first row are not shifted, in the second are shifted by 3 bytes, in the third over 2 bytes and in the last one by 1 byte to the left (Fig. 6).

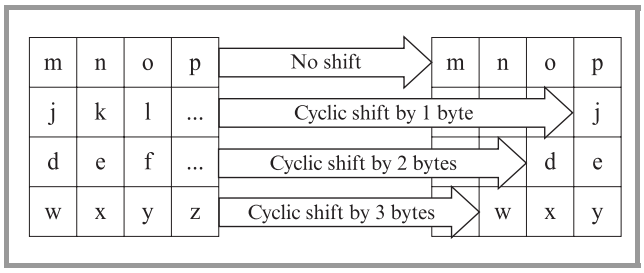


***Fig. 5.*** The ShiftRow transformation.

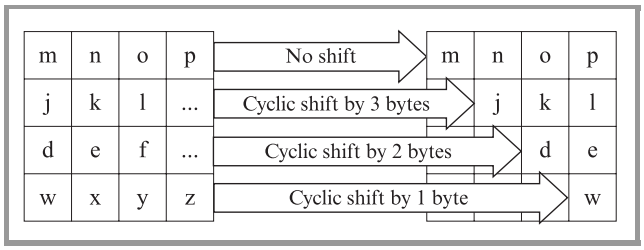


***Fig. 6.*** The InvShiftRow transformation.

### *2.3. MixColumn (InvMixColumn) transformation*

In the MixColumn transformation, the bytes located in the columns of the state, are considered as coefficients of polynomials of degree less then 4 over GF($2^8$) field and multiplied modulo $(x^4+1)$ with a fixed polynomial $c(x) = \text{'03'}x^3 + \text{'01'}x^2 + \text{'01'}x + \text{'02'}$, where '03' denotes a hexadecimal value. Figure 7 illustrates the effect of the MixColumn transformation on the state.

In the InvMixColumn transformation, the polynomials of degree less then 4 over GF($2^8$), which coefficients are the elements in the columns of the state, are multiplied modulo $(x^4+1)$ by a fixed polynomial $d(x) = \text{'0}B\text{'}x^3 + \text{'0}D\text{'}x^2 + \text{'09'}x + \text{'0}E\text{'}$, where '0$B$', '0$D$,'09', '0$E$' denote hexadecimal values. Figure 7 illustrates the effect of the InvMixColumn transformation on the state.

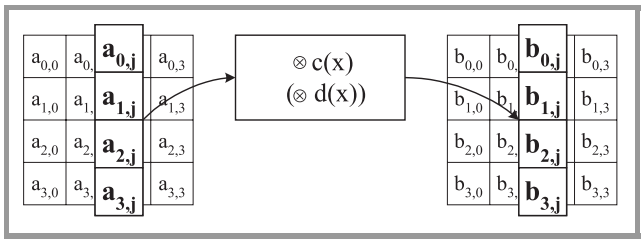


***Fig. 7.*** The MixColumn (InvMixColumn) transformation.

### *2.4. The AddRoundKey transformation*

In the AddRoundKey mapping, the 128-bit round key, which is derived from the key by the KeyExpansion algorithm, is bytewise XORed with the state.

### *2.5. Key Expansion*

The round key (subkey) of each round is derived from the main key using the KeyExpansion algorithm [1]. The encryption (decryption) algorithm needs eleven 128-bit subkeys, which are denoted K0 ÷ K10 (the first subkey K0 is the main key). The round keys are derived as follows: let us denote the bytes of the expanded key by $B_0, B_1, B_2, \ldots, B_{175}$ where the main key is $B_0, B_1, B_2, \ldots, B_{15}$ (K0 = $B_0, B_1, \ldots, B_{15}$). Then the expanded key is derived from the formulae:

$$B_n = \begin{cases} B_{n-16} \oplus \text{SubByte}(B_{n-3}) \oplus RC[\frac{n}{16}], & \text{if (n mod 16)} = 0; \\ B_{n-16} \oplus \text{SubByte}(B_{n-3}), & \text{if (n mod 16)} \in \{1,2\}; \\ B_{n-16} \oplus \text{SubByte}(B_{n-7}), & \text{if (n mod 16)} = 3; \\ B_{n-16} \oplus B_{n-4}, & \text{otherwise;} \end{cases}$$

where:
SubByte($B$) is a function that returns a byte, which is the result of applying the ByteSub transformation for one byte;
$RC[i]$ – an element over GF($2^8$), which represents round constants and is defined by:
$RC[1]$ = '01';
$RC[i] = x \cdot (RC[i-1]) = x^{(i-1)}$.
Round keys are taken from the expanded key in the following way: the first subkey consists of the first 16 bytes (K0 = $B_0 \ldots B_{15}$), the second one of the following 16 bytes (K1 = $B_{16} \ldots B_{31}$), and so on.

## 3. Field programmable gate array implementation of the Rijndael cipher

### *3.1. Encryption and decryption units*

The encryption algorithm implementation is designed to perform the subkey generation and the round calculations in parallel. Firstly, the initial (Round 0) round (input data

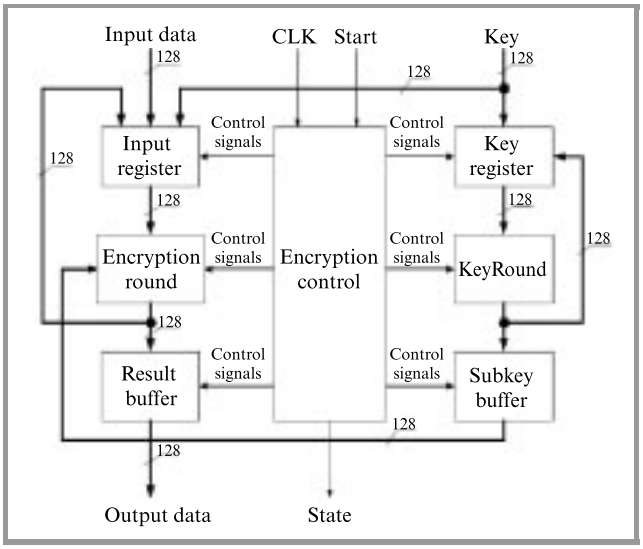


***Fig. 8.*** The encryption unit.

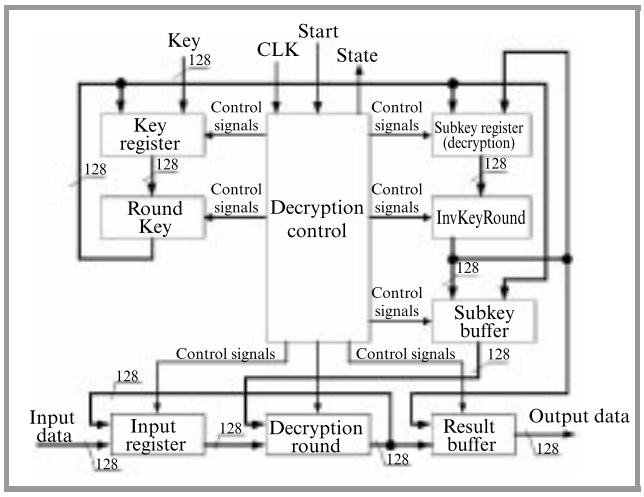


*Fig. 9.* The decryption unit.

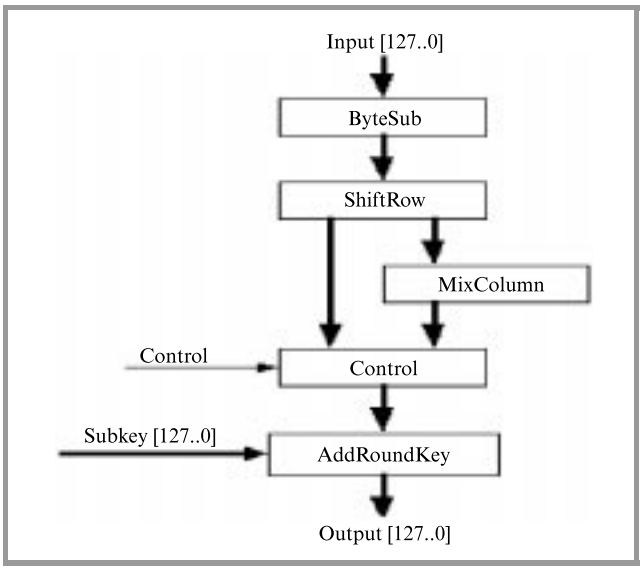


*Fig. 10.* The encryption round.

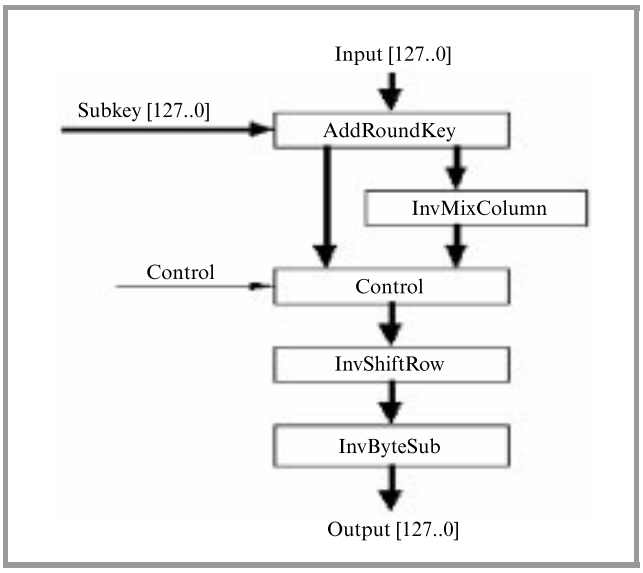


*Fig. 11.* The decryption round.

EXOR-ed with the main key) is performed and the subkey for the round number one is calculated. Then the round transformations are performed and the subkey for next round is calculated. The advantage of such design is that there is no need for storing the subkeys; they are calculated on the fly and discarded after using. The encryption unit is presented in Fig. 8.

The decryption algorithm is implemented in the similar way. Firstly, the tenth subkey (K10) is calculated, then calculations of the inversion of the final round (InvRound 10) and the subkey generation for the next decryption round (K9) are performed simultaneously. The decryption unit is presented in Fig. 9.

### *3.2. Round transformation implementations*

Basic encryption round consists of the following transformations: ByteSub, ShiftRow, MixColumn, AddRoundKey (the final encryption round does not contain the MixColumn transformation). The round implementation is designed to work both in basic round mode and in the final round mode. The encryption round scheme is presented in Fig. 10.

The basic decryption round (which is the inversion of the basic encryption round) consists of the following transformations: AddRoundKey, InvMixColumn, InvShiftRow, InvByteSub. The first decryption round (InvRound 10 – which is the inversion of the final encryption round) does not contain the InvMixColumn transformation. The decryption round implementation is designed in similar way as the encryption round and its scheme is presented in Fig. 11.

The nonlinear ByteSub (InvByteSub, respectively) transformation contains 16 S-boxes (InvS-boxes, respectively), working in parallel. The 128-bit input block is divided into 16 bytes. Each byte forms the input data of the S-box (InvS-box, respectively). The byte outputs of all S-boxes (InvS-boxes, respectively) are then concatenated and form the output of the ByteSub (InvByteSub, respectively) transformation.

The S-box transforms the input byte to the inverse byte by performing the arithmetic operation defined over the finite field GF($2^8$) (the value '00' is mapped in '00') and then forms the input for the affine transformation. For inverse transformation, the process runs in the opposite direction. The S-box (InvS-box, respectively) was implemented by using the build-in EAB memory which emulate the ROM memory with the configuration of $256 \times 8$ bits. The implementation of the S-box needs one EAB block, i.e. 2048 bits. The access memory time in this implementation is approx. 18 ns.

In the ShiftRow (InvShiftRow, respectively) transformation, the 128-bit input block is divided into 16 bytes denoted as *Aij*[7..0], where *i,j* $\in \{0,1,2,3\}$. The bytes *Aij*[7..0] are the elements of the table representing the intermediate state of encrypted (or decrypted) block. The output of the ShiftRow (InvShiftRow) transformation is composed of the bytes *Bij*[7..0], where *i,j* $\in \{0,1,2,3\}$. The implementations of these transformations perform the byte shift, as shown in Figs. 12 and 13.

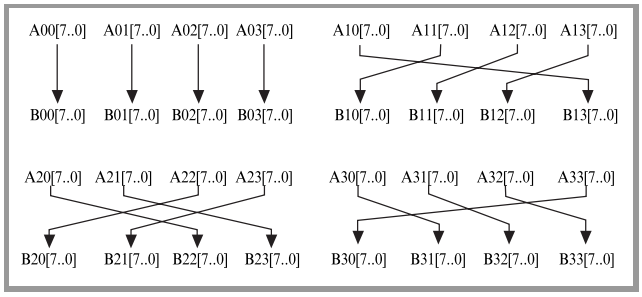


***Fig. 12.*** The ShiftRow transformation.

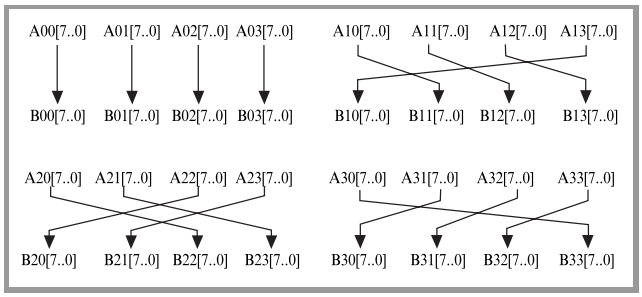


***Fig. 13.*** The InvShiftRow transformation.

In the MixColumn (InvMixColumn, respectively) transformation, the 128-bit input block is divided into 16 bytes denoted as *Aij*[7..0], where *i,j* $\in \{0,1,2,3\}$, and the output bytes are denoted as *Bij*[7..0]. The bytes *Aij*[7..0], while the index *j* is fixed and $i \in \{0,1,2,3\}$, correspond to the column of the table representing the intermediate state of the transformed block and they are viewed as the coefficients of polynomial over the field $GF(2^8)$ of degree smaller then four. This polynomial is multiplied by the fixed polynomial $c(x)$ = '03'$x^3$ + '01'$x^2$ + '01'$x$ + '02' modulo $(x^4+1)$. In the case of decryption the inverse polynomial $d(x)$ is used: $d(x)$ = '0B'$x^3$ + '0D'$x^2$ + '09'$x$ + '0E'. The results of this modular multiplication form the column *Bij*[7..0] (index *j* is fixed and $i \in \{0,1,2,3\}$) of the transformed state. These transformations were implemented as bit-oriented EXOR operations.

The AddRoundKey transformations have the block text as the input value and EXOR-ed it with the value of the subkey of the given round.

The logical unit denoted as KeyRound (InvKeyRound, respectively) calculates the subkeys of subsequent rounds of the encryption (decryption, respectively) algorithm. It is controlled by signals from the logic unit EncryptionControl (DecryptionControl, respectively) and input values of the subkey. The functional description of the logical units KeyRound and InvKeyRound are depicted in Figs. 14 and 15, respectively.

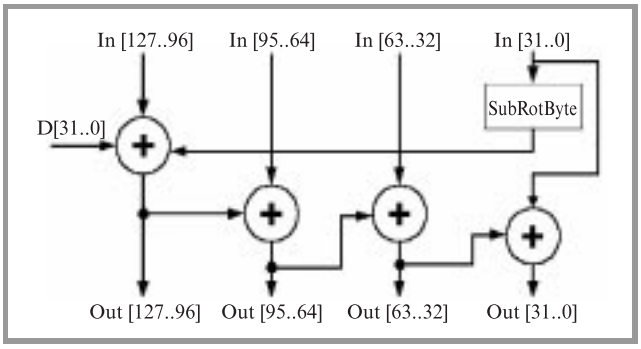


***Fig. 14.*** The logical unit KeyRound.

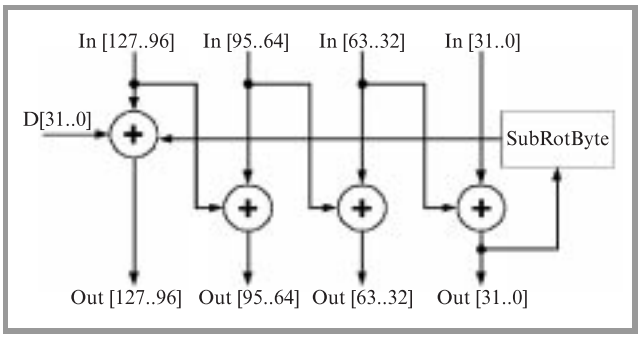


***Fig. 15.*** The logical unit InvKeyRound.

The round constants D[31..0] (see Figs. 14 and 15) have values depending on the round number, as presented in Table 1.

Table 1
The values of the constants D[31..0]

| The encryption round number | The decryption round number | D[31..0](hex) |
|---|---|---|
| 1 | 10 | 01000000 |
| 2 | 9 | 02000000 |
| 3 | 8 | 04000000 |
| 4 | 7 | 08000000 |
| 5 | 6 | 10000000 |
| 6 | 5 | 20000000 |
| 7 | 4 | 40000000 |
| 8 | 3 | 80000000 |
| 9 | 2 | 1B000000 |
| 10 | 1 | 36000000 |

The logical unit SubRotByte has 32 inputs and 32 outputs. It performs two operations: RotByte and SubByte. The RotByte transformation is a cyclic bytes rotation in 32-bit word by one byte position to the left. The SubByte transformation consists of four parallel S-boxes applied to the 32-bit input word.

### *3.3. Implementation results*

The encryption and decryption algorithms have been implemented in two separable chips denoted as EPF10K250AGC599-1 (this type of Altera chip has 20 blocks of the EAB memory which can be used to implement $256 \times 8$ bit ROM configuration). The results of logic circuit synthesis are given in Table 2.

Table 2
The logic circuit synthesis results for encryption and decryption process

| The logical unit | Input pins | Output pins | Bidir pins | Memory [bit] | LCs |
|---|---|---|---|---|---|
| Encryption round | – | – | – | 32768 | 388 |
| KeyRound | – | – | – | 8192 | 138 |
| The other logic blocks | – | – | – | 0 | 506 |
| **Encryption** | **258** | **129** | **0** | **40960** | **1032** |
| Decryption round | – | – | – | 32768 | 798 |
| InvKeyRound | – | – | – | 8192 | 139 |
| RoundKey | – | – | – | 0 | 1475 |
| The other logic blocks | – | – | – | 0 | 473 |
| **Decryption** | **258** | **129** | **0** | **40960** | **2885** |

It appears from the table that the decryption algorithm is more complicated than the encryption one (see also Figs. 8 and 9). In result, the logic circuit synthesis for the decryption unit requires over twice as many macrocells the encryption unit. It is worth to observe that before the main part of decryption process the tenth subkey should be calculated. The RoundKey unit performed this operation requires ca 1475 macrocells. Moreover, the decryption round needs twice as many macrocells as the encryption round because the polynomial $d(x)$ used in InvMixColumn transformation is more complicated then the polynomial $c(x)$ used in MixColumn transformation.

The speed of encryption and/or decryption implementation depends mainly on the frequency of the external clock applied to the chip. According to the characteristics the minimal clock cycle is 22 ns (45.45 MHz) for the encryption chip and 24 ns (41.66 MHz) for the decryption chip. The encryption or decryption operation is performed in 21 clock cycles. In the implementation of the Rijndael algorithm with 128-bit encrypted blocks and 128-bit key presented here, the speed of 268 Mbps for encryption and 248 Mbps for decryption has been achieved (Table 3).

Table 3
The speed of encryption and decryption process

| Hardware implementation (Altera) | The encryption unit [Mbps] | The decryption unit [Mbps] |
|---|---|---|
| The process speed | 268 | 248 |

Hardware implementations of the Rijndael, based on Altera FLEX FPGA devices were also developed by two other groups working independently: Microsonic [2] and GMU (George Mason University) [3]. The results of implementing Rijndael using FLEX 10K130E and FLEX 10K250A devices are summarized in Fig. 16.

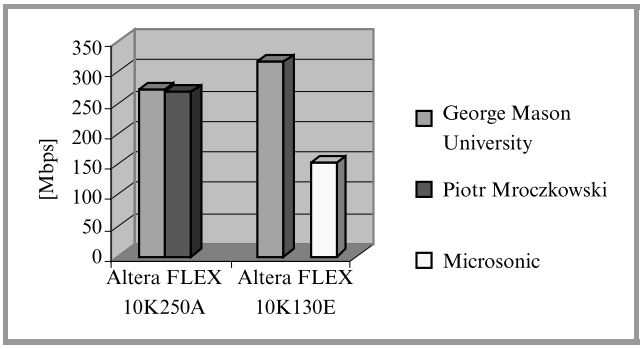


***Fig. 16.*** Comparison of chosen hardware implementations of the Rijndael cipher.

The Figure shows similar performance achieved by GMU group and the Author. However, this is not the case when comparing performance of implementations using FLEX 10K130E devices achieved by Microsonic and GMU group.

## 4. Conclusions

The Rijndael cipher seems to be very suitable for hardware implementations using Altera FLEX 10K devices. Especially, the EABs fit very well for implementing large S-boxes, such as $8 \times 8$ S-boxes used in Rijndael. The achieved speed is about four times greater than for software implementations reported. The further progress can be possibly made with the pipeline architecture.

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[5] V. Rijmen, the private communications,
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[1] Y. Namihira, „Relationship between nonlinear effective area and modefield diameter for dispersion shifted fibres", *Electron. Lett.*, vol. 30, no. 3, pp. 262–264, 1994.

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