Invited paper

Semiconductor cleaning technology for next generation material systems

Jerzy Ruzyllo

Abstract— This paper gives a brief overview of the challenges wafer cleaning technology is facing in the light of advanced silicon technology moving in the direction of non-planar device structures and the need for modified cleans for semiconductors other than silicon. In the former case, the key issue is related to cleaning and conditioning of vertical surfaces in next generation CMOS gate structure as well as deep 3D geometries in MEMS devices. In the latter, an accelerated pace at which semiconductors other than silicon are being introduced into the mainstream manufacturing calls for the development of material specific wafer cleaning technologies. Examples of the problems related to each challenge are considered.

Keywords— III-V compounds, FinFET, IC manufacturing, MEMS, MOS gate stack, semiconductor cleaning.

1. Introduction

Wafer cleaning is the most frequently applied processing step in high-end silicon IC manufacturing. As such, chemistry and implementation of Si cleaning operations are very well established and backed by many years of extensive research, as well as significant industrial tool base. As a result, silicon cleaning technology is by far the most mature among all semiconductors of any practical importance. The first complete, based on scientific considerations cleaning recipe specifically designed to clear Si surface from particles, metallic, and organic contaminants was proposed in 1970 [1]. Since then, silicon cleaning technology was undergoing continuous evolutionary modifications. Surprisingly, state-of-the-art Si cleaning still relies on roughly the same set of chemical solutions, but the way they are prepared and delivered to the wafer is very different from the one proposed originally. In addition, selected surface cleaning/conditioning functions that were traditionally performed by wet cleaning chemistries are now carried in the gas-phase [2].

What is important to the point being made in this paper, however, is that as advanced as they currently are, silicon cleaning methods cannot meet all the diversified emerging needs of semiconductor technology across the spectrum of materials and device structures both in terms of implementation methods and chemistries. Two key challenges are reviewed in this paper. First challenge is related to the growing importance of non-planar silicon devices such as next generation MOS gate stacks, micro-electro-mechanical system (MEMS) devices, and nanowires. Cleaning operations implemented in the traditional way may not be entirely effective in these cases. Second challenge results from the increasingly broad use in practical applications of semiconductor materials other than silicon. The re-emergence of germanium (Ge) as a possible replacement for silicon in selected applications, growing importance of IV-IV compounds (SiGe, SiC), and inevitable continued growth of technology of III-V compounds such as GaAs, GaN, and InSb for instance, underscores this trend.

2. Non-planar silicon based devices

The issue of non-planarity of silicon surfaces in device fabrication is likely to challenge standard wafer cleaning technology on at least three different fronts.

2.1. Next generation CMOS technology

A challenge at hand in cutting edge digital CMOS technology is to maintain adequate capacitance density of gate structure needed to sustain high drive current. One approach is to use gate dielectrics featuring dielectric constant higher than that of SiO_2, while the other is to increase gate area without increasing the area of the cell by structuring MOS gate 3-dimensionally. As the latter approach appears to be the one that will provide better long-term solutions, the interest in processing 3D MOS gate structures is growing. Regardless of what specific configuration will become a standard, all will involve pre-gate oxidation cleaning and conditioning of post-RIE vertical walls engraved in silicon. For example, one possible solution considered involves formation of the thin "fin"-like strip of Si and forming an MOS gate structure around it as shown in Fig. 1. Starting with silicon-on-insulator (SOI) substrate (Fig. 1a), the fin as shown in Fig. 1b is formed by reactive ion etching (RIE).

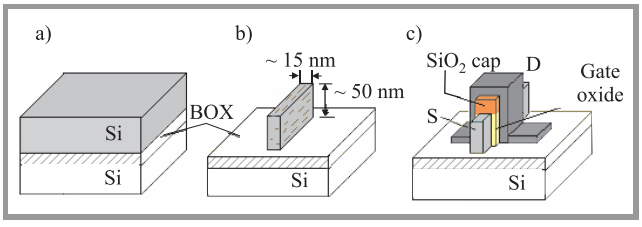

Fig. 1. The SOI substrate (a) in which a "fin" is defined by RIE (b), and then MOS gate is built around it (c).

Surrounded at both sides by the gate oxide and gate contact such a "fin" will eventually become a channel in the FinFET structure (Fig. 1c).
In the processing of the vertical surfaces of the "fin" in FinFETs [3] (Fig. 1b), or in other structures with working sidewalls [4], or in the processing of U-shaped trenches in UMOSFETs [5], the challenge is to assure defect-free SiO_2-Si interface formed on the surfaces defined by the damaging RIE process. Furthermore, a drastic departure from surface flatness in next generation MOS gate structures creates obvious problems in particle removal.

2.2. MEMS technology

Due to the advantageous mechanical properties of Si increasingly complex micro-electro-mechanical systems are possible. Specific feature of MEMS manufacturing is that it includes deep etching of elaborate 3D features, as well as demanding release processes such as those shown in Fig. 2 where buried oxide (BOX) in SOI wafer is deep

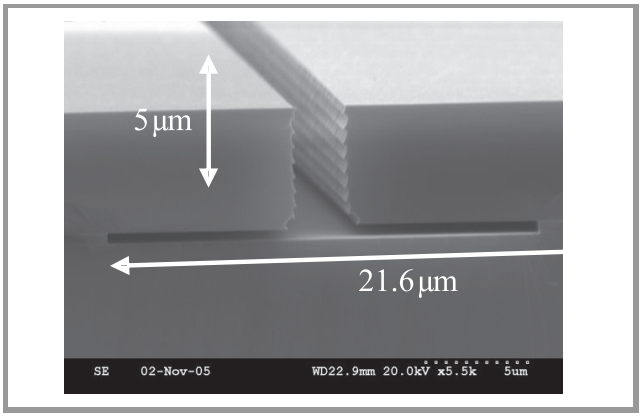

Fig. 2. SOI wafer with "buried oxide" etched laterally.

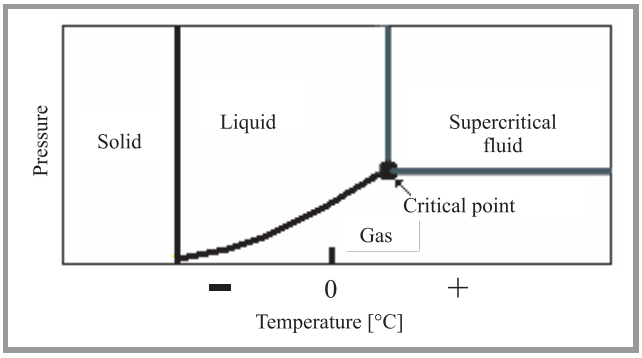

Fig. 3. Definition of the supercritical fluid phase.

etched laterally. Removal of possible etch residues from such extremely confined geometrical features and assuring stiction-free operation of beams and membranes cannot be accomplished using conventional wet cleaning and etching technology. The anhydrous HF/methanol (AHF/MeOH) [6] sacrificial oxide etch process has been investigated as a viable solution to the latter [7]. Solution to the MEMS cleaning problems comes in the form of a supercritical fluid cleaning technology [8]. Once in the supercritical state, a fluid features essentially no surface tension, and hence, features no limitations regarding geometries it can penetrate. Due to these characteristics, a supercritical cleaning technology becomes a standard in the processing of highly confined semiconductor structures. Figure 3 shows under what conditions in terms of temperature and pressure liquids and gases can be transformed into a state of supercritical fluid. The most common supercritical carrier of cleaning chemistries is CO_2 for which a critical point is at 31°C and 73 atm.

2.3. Silicon nanowires

In the continued push toward faster and more efficient switching devices, silicon nano-geometry structures that depart from conventional planar technology, such as silicon nanowires, are aggressively pursued. Making functional devices out of nanowires requires subjecting them to a standard fabrication sequence. Figure 4 shows loosely scattered Si nanowires released after an anisotropic bottom-up growth process and a single wire mounted in between two metal contacts. Considering extreme fragility of nanowires and a size that makes their handling very difficult, the use of conventional fabrication methods is in this case severely restricted. In particular, those restrictions apply to wet cleaning operations which, due to the problems of nanowire han-

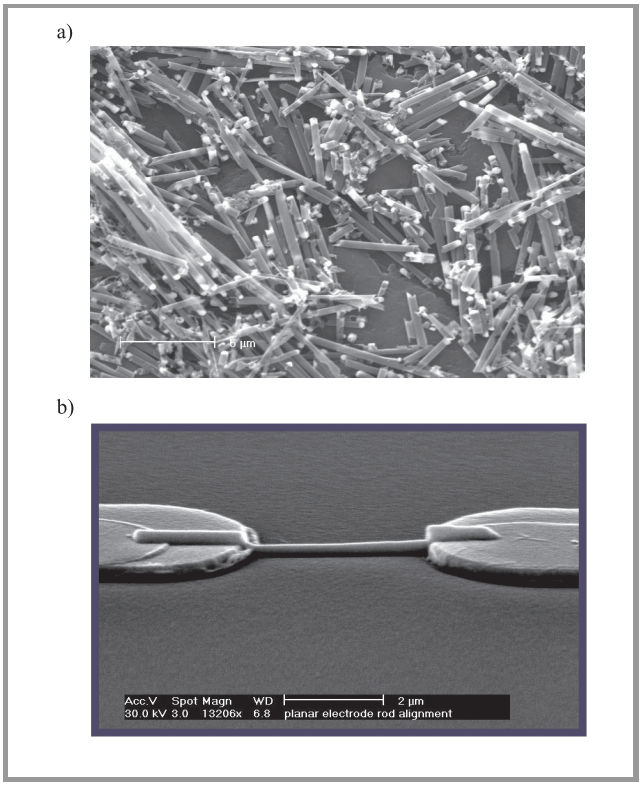

Fig. 4. (a) Silicon wires after growth and release and (b) single wire mounted between two contacts (*Courtesy Redwing Research Group, Penn State University*).

dling in liquids, are incompatible with nanowire processing. Also, anisotropic dry cleaning methods (derivatives of sputtering and RIE) are not suitable in this application. The isotropic gas-phase methods based on HF vapor, e.g., AHF/MeOH process [6, 9] or remote plasma [10] may offer workable solutions to the problem of nanowire cleaning and surface conditioning.

3. Semiconductors other than silicon

Due to its outstanding crystal quality, excellent oxidation characteristics, manufacturability, abundance, relatively low cost, and adequate electronic properties silicon was for the last 40 years, and will remain in the future, a dominant semiconductor used in device manufacturing. However, growing needs for improved performance in specific electronic (e.g., high-temperature, high-power, as well as ultra-high speed) and photonic (e.g., emission of blue light or UV detection) applications, require significantly improved manufacturing technology in the range of semiconductors other than silicon. Examples of such materials include germanium, Ge, due to its electron mobility higher than that of Si and prospects for integration with high-*k* gate dielectrics, silicon germanium, SiGe, needed to process strained-channel Si MOSFETs, as well as silicon carbide, SiC, for its wide energy gap. Also of growing interest are III-V semiconductors beyond the most advanced GaAs such as GaN for its wide, direct band gap, and indium antimonide, InSb, for its electron mobility of 80 000 cm^2/Vs to name just two. Figure 5 shows key characteristics of selected elemental and compound semiconductors [11].

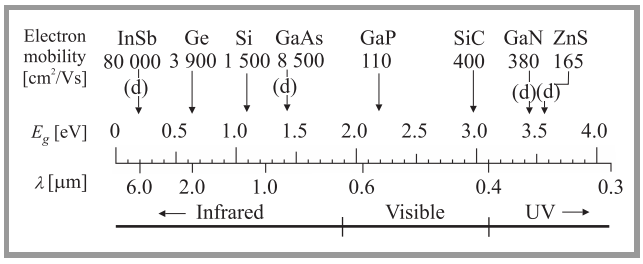

Fig. 5. Energy band gap, type of the energy gap, and cut-off wavelengths for various semiconductors.

Surface cleaning is becoming a growing issue in the processing of semiconductors other than silicon. This is because for the most part inferior quality of the substrate crystal rather than cleanliness of its surface was until recently a dominant factor defining manufacturing yield in those materials. With the improvements in the quality of single-crystal substrates of various semiconductors the paradigm is shifting and much closer attention to the cleaning technology is being paid.

In general, technology of surface cleaning of materials other than silicon attempts to draw from the pool of Si cleaning chemistries and to use high performance cleaning infrastructure developed over the last 40 years for silicon. While there is no significant barrier regarding the latter task, implementation of the former is not a straightforward matter. This is because due to the differences in the chemical compositions, various semiconductors not always respond in the desired fashion to the cleaning chemistries successfully used in silicon processing. To illustrate the nature of the problem we shall consider cleaning-related issues in the case of germanium, Ge, and silicon carbide, SiC.

Germanium is re-emerging as an alternative to silicon semiconductor in those applications in which outstanding characteristics of silicon's native oxide, SiO_2, are not coming into play and in which higher electron mobility of Ge may be beneficial. Specifically, Ge in conjunction with high-*k* gate dielectrics may offer advantages over the Si based MOS gates. However, processing of Ge-HfO_2 gate stacks for instance, requires surface termination prior to high-*k* deposition different than in the case of silicon. One approach is to Si-passivate germanium surface through an anneal in SiH_4. Also, plasma PH_3 treatment at 400°C given to Ge in situ prior to HfO_2 deposition was reported to improve the characteristics of both NMOS and PMOSFETs [12].

As far as standard cleaning operations such as native oxide etching, particle and metallic contaminant removal are concerned, the response of Ge surface to the Si cleaning chemistries varies depending on application. In the case of particle deposition and removal for instance, it was established that Ge surface acts in the same way as Si surface [13]. Situation is different in the case of Ge native oxide, GeO_2, which in contrast to Si native oxide SiO_2, cannot be removed entirely using HF-based chemistries [14, 15]. Furthermore, the metallic contaminant deposition and removal was shown to be driven in the case of Ge by somewhat different mechanisms than in the case of Si substrates. Most notably, in the case of Ge it does depend on the pH of solution, and, unlike in the case of Si, all common metallic contaminants can be removed from the Ge surface using HF:H_2O solution [16].

In contrast to elemental semiconductors such as Si and Ge, silicon carbide, SiC, represents a class of man-made binary semiconductor compounds in which each element features often drastically different chemical characteristics. In the case of SiC for instance, oxidized Si forms a solid SiO_2, while oxidized carbon forms gaseous compounds CO and CO_2. Hence, the response of compound semiconductors to cleaning chemistries may not be entirely isotropic. In spite of it, due to the fact that SiC is a chemical derivative of Si, cleaning chemistries used in Si processing are rather arbitrarily adopted to process SiC surfaces. It turns out that such an automatic transfer of cleaning technology from Si to SiC may not necessarily produce the desired results. To exemplify this point let us refer to the results of the experiments in which roughness of SiC surface exposed to various cleaning chemistries was monitored [17]. The results, summarized in Fig. 6, indicate sensitivity of SiC

surface roughness to various cleaning chemistries different both quantitatively and qualitatively than that of Si.

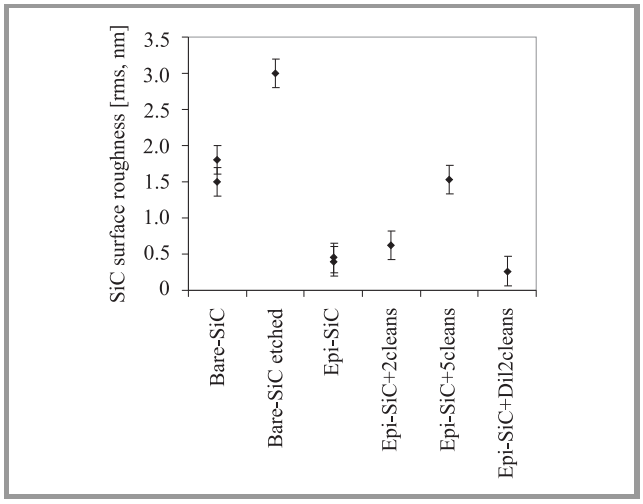

Fig. 6. Changes of SiC surface roughness as a result of various chemical surface treatments.

An analysis supported by experiments similar to the one given above for SiC should be carried out for other compound semiconductors, III-V in particular. The results are very likely to demonstrate that the needs regarding cleaning technology vary from material to material, and hence, for each semiconductor material of interest, the dedicated cleaning recipes should be developed.

4. Summary

The purpose of this overview was to demonstrate the challenges cleaning and surface conditioning technology is facing as on the one hand silicon technology goes non-planar and on the other, semiconductors other than silicon are being pursued more actively than ever before in a range of applications. The discussion presented leads to the following observations:

– silicon cleaning technology both in terms of chemistries as well as tools used is a foundation upon which any new developments responding to the emerging needs of semiconductor cleaning will be based;

– silicon cleaning chemistries are not always compatible with all semiconductors that may be of the commercial importance, and hence, dedicated cleaning technology must be investigated and developed for each of them;

– innovative solutions are needed to cope with surface cleaning and conditioning needs in emerging non-planar device manufacturing such as 3D MOS gates, MEMS, nanowires, and nanotubes.

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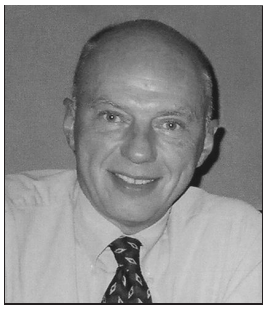

Jerzy Ruzyllo is a Professor of electrical engineering and materials science and engineering at Penn State University in the United States and holds a title of Professor in Poland. He received his Ph.D. degree in 1977 from the Warsaw University of Technology, Poland, where he also served on the faculty before joining Penn State. His experience and professional interests are in research and teaching in the area of semiconductor materials and device processing. He is a Fellow of IEEE and a Fellow of the Electrochemical Society.
e-mail: jxr6@psu.edu
Department of Electrical Engineering
Penn State University
University Park, PA 16802, USA