Invited paper

Low frequency noise in Si and Si/SiGe/Si PMOSFETs

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Abstract— Measurements of $1/f$ noise in Si and $Si_{0.64}Ge_{0.36}$ PMOSFETs have been compared with theoretical models of carrier tunnelling into the oxide. Reduced noise is observed in the heterostructure device as compared to the Si control. We suggest that this is primarily associated with an energy dependent density of oxide trap states and a displacement of the Fermi level at the SiO_2 interface in the heterostructure relative to Si. The present study also emphasizes the important role of transconductance enhancement in the dynamic threshold mode in lowering the input referred voltage noise.

Keywords— electronic noise, silicon germanium heterostructures, MOSFET, dynamic threshold mode.

1. Introduction

Low frequency noise limits the performance of analogue CMOS circuits and could ultimately degrade the noise margin in digital CMOS circuits. Si/SiGe/Si PMOS devices offer low noise solutions with enhanced maximum voltage gain for analogue applications; however, a consensus is yet to emerge on the detailed mechanism of noise reduction. In this paper, we summarize our previous measurements on this system which have led us to suggest that the origin of the noise reduction lies in the energy dependent density of oxide trap states and the suppression of carrier number fluctuations [1]. New data is presented in support of this contention and the important role of transconductance enhancement in the dynamic threshold (DT) mode (gate connected to body) as opposed to body tied (BT) mode (source connected to body) operation is illustrated.

2. Experimental results

Figure 1 shows the devices on which measurements were made, which were fabricated in a 0.5 μm process [2]. The carrier mobility in these devices, Fig. 2, depends on silicon cap thickness, which strongly suggests that alloy scattering is not a dominant mobility limiting process and this conclusion is supported by our other work [3].

The normalised current noise power spectral density (PSD) S_I/I^2 of a SiGe device is shown in Fig. 3, together with that of a surface channel Si control having the same vertical doping profile. The noise in the SiGe device is clearly much reduced as compared to the control – by an order of magnitude in the low frequency region where $1/f$ noise dominates. The corresponding PSDs for resistance fluctua-

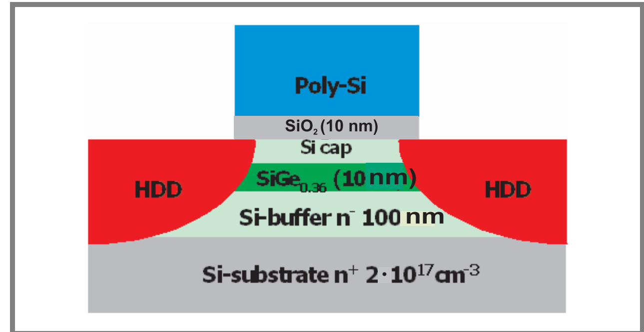

Fig. 1. Schematic diagram of PMOSFET devices used. The Si control is identical apart from the alloy layer.

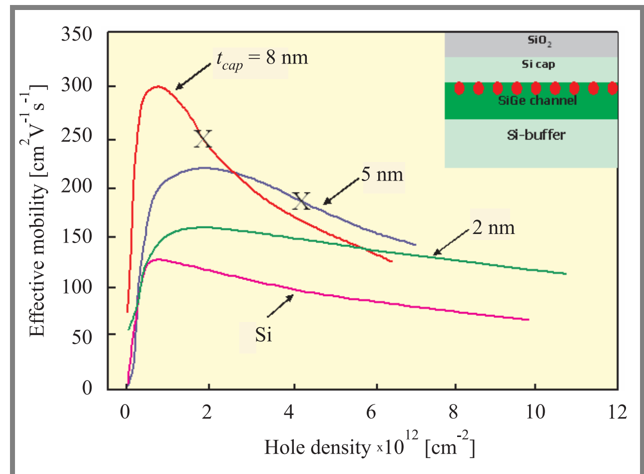

Fig. 2. Room temperature hole mobility for three different cap thicknesses, demonstrating clearly that alloy scattering is not a dominant mobility limiting mechanism [2].

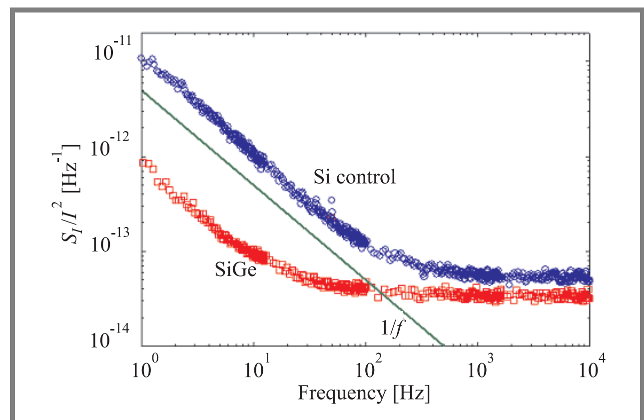

Fig. 3. Current noise power spectral density, demonstrating that SiGe devices display lower noise than Si control ($V_{GT} = -3.5$ V, $L = 40$ μm, $W = 40$ μm, $T = 300$ K, $V_{DS} = -50$ mV) [1].

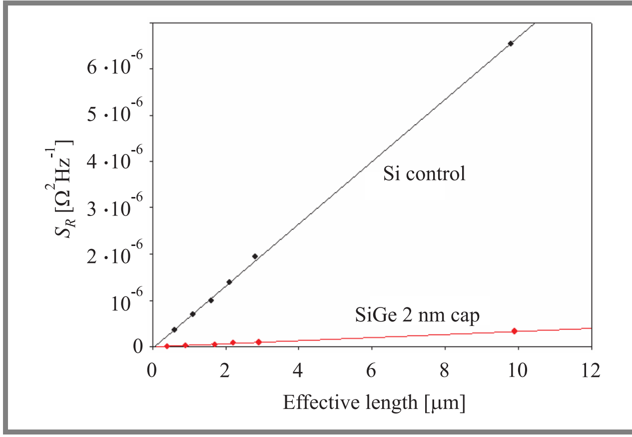

Fig. 4. Resistance fluctuations at 10 Hz as a function of gate length ($V_{GT} = -3.5$ V, $W = 40$ μm, $V_{DS} = -50$ mV). Extrapolation to zero gate length demonstrates that source and drain do not contribute noise. Noise is attributed to channel only [1].

tions S_R are plotted as a function of gate length L in Fig. 4, where a linear variation with L and extrapolation through the origin indicate that the noise may be attributed solely to the channel [4].

3. Comparison with noise models

We will now examine whether our noise data can be interpreted in terms of the commonly applied number fluctuation theory combined with correlated mobility fluctuations. There are three possible expressions that could be applied: for carrier number fluctuations (CNF) only [5, 6]

$$\frac{S_{I_D}}{I_D^2} = \left(\frac{R_N}{N_s}\right)^2 \frac{N_{ox}(E_F)\mathrm{k}T}{WL\gamma f}. \tag{1}$$

If the associated oxide charge variations give rise to correlated mobility fluctuations (CMF1) [5, 6] then the normalised current noise PSD is

$$\frac{S_{I_D}}{I_D^2} = \left(\frac{R_N}{N_s} + \alpha\mu\right)^2 \frac{N_{ox}(E_F)\mathrm{k}T}{WL\gamma f}. \tag{2}$$

Alternatively, the carrier number fluctuations can lead to fluctuations in total mobility (CMF2) [7]

$$\left(\frac{\Delta I_D}{I_D}\right)^2 = \left(\frac{\Delta N}{N}\right)^2 \left(1 + \frac{N}{\mu}\left(\frac{d\mu}{dN}\right)\right)^2, \tag{3}$$

where α is a factor associated with correlated mobility fluctuations, N_S is the sheet density of carriers in the inversion layer and N their total number. The term $R_N = C_{inv}/(C_{ox} + C_D + C_{inv})$ is associated with carrier number fluctuations, C_{inv}, C_{ox} and C_D are the inversion, oxide and depletion capacitance, respectively; μ is the effective mobility, $N_{ox}(E_F)$ the volume density of oxide traps per unit energy at the Fermi level, W the device width, and γ is the attenuation coefficient of the carrier wavefunction into the oxide.

We have tried to fit our data for the silicon control, using Eqs. (1), (2) or (3) and making the commonly used assumption [5] that the density of oxide trap states N_{ox} is independent of energy. This is shown in Fig. 5, where the normalised current PSD is plotted against current. The fact that none of these equations fits the data is attributed to the failure of this assumption.

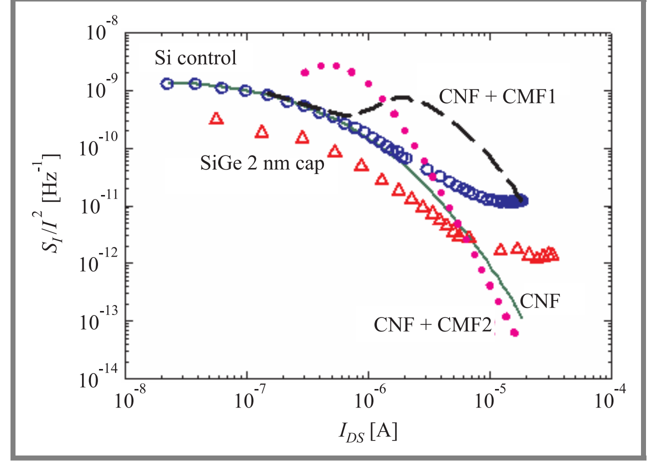

Fig. 5. Attempts to fit the experimental noise data from the Si control with models based on carrier number fluctuations and carrier mobility fluctuations as described in the text, assuming an energy independent density of oxide traps [1].

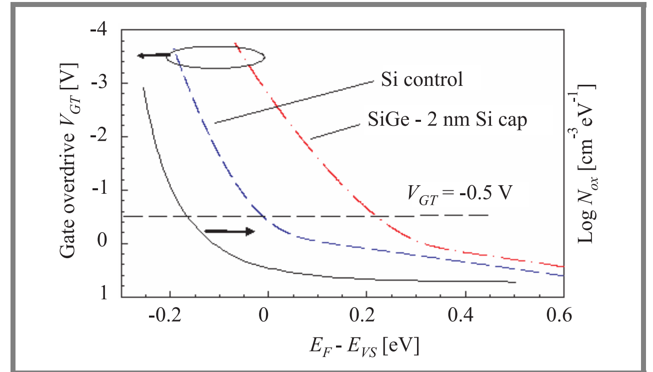

Fig. 6. Showing the displacement of the Fermi energy from the valence band edge as gate overdrive V_{GT} varies in the Si and SiGe devices, together with a schematic view of the variation in density of oxide traps across the band gap. For the same gate overdrive (dashed line shows case at $V_{GT} = -0.5$ V), the Fermi level in the SiGe device lies closer to mid-gap, where N_{ox} has a lower value, than in the Si control. Hence carrier tunnelling at E_F is into a reduced density of final states and the $1/f$ noise is therefore suppressed in the SiGe.

Chroboczek and Ghibaudo [5] have used equation Eq. (2) with N_{ox} constant, and on this basis attribute the suppression of noise in the buried channel to relatively weak scattering from oxide charge fluctuations, i.e., α small. While this is undoubtedly the case, we look for a more complete description of the behaviour. It is assumed that N_{ox} varies with energy roughly as shown schematically in Fig. 6. Since, for the same gate overdrive, the Fermi level in

the SiGe device lies closer to mid-gap than for the Si control, carriers at the Fermi level tunnel into a smaller number of oxide states for the alloy. Hence, the $1/f$ noise is suppressed in the alloy channel. Thus, there is the possibility that both mechanisms of noise suppression contribute. Thinking purely in terms of number fluctuations, S_I/I^2 should vary as $(g_m/I)^2$ if N_{ox} is constant [5]. This model is compared with the experimental results in Fig. 7,

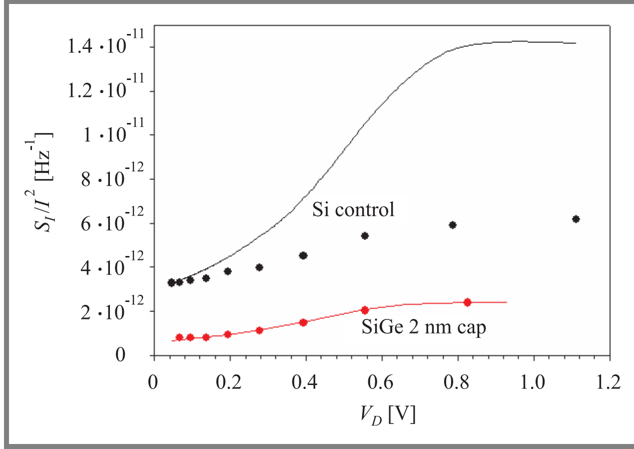

Fig. 7. Comparison of current noise PSD at 1 Hz (points) with a CNF model where $S_I/I^2 \propto (g_m/I)^2$ only. The discrepancy may be interpreted as N_{ox} varying with energy as in Fig. 6 ($V_{GT} = -3.5$ V, $W = 40$ μm, $L = 40$ μm).

where S_I/I^2 is plotted against drain voltage V_{DS}, and found to produce good agreement for the SiGe, but not for the Si devices. The effect of increasing the drain voltage is to raise the Fermi level closer to mid-gap, making the increase in noise with V_{DS} smaller than it would be if N_{ox} were independent of energy. If we accept Fig. 6 as a rough guide, then it is to be expected that the deviation from the theoretical $(g_m/I)^2$ curve is likely to be greater in Si, for which the variation of E_F spans the range where N_{ox} is rapidly varying, than in SiGe where N_{ox} only varies slowly over the energy range of interest. It is tentatively proposed that the observed behaviour provides further support for our model.

4. Dynamic threshold mode

Further improvements in performance are provided by DTMOS operation, with the gate (as opposed to the source) contact connected to the transistor body. As seen in Figs. 8, 9 and 10, the subthreshold swing, transconductance and maximum voltage gain all improve in both the SiGe and Si devices. The current noise in the SiGe and Si devices is independent of the mode of operation, as shown in Fig. 11. However, it is the input referred voltage noise $S_V = S_I/g_m^2$, shown in Fig. 12, which is important for circuit applications. Whereas this is equal to the flatband voltage fluctuation in the BT mode, and is therefore ultimately independent of g_m, in the DT mode of operation

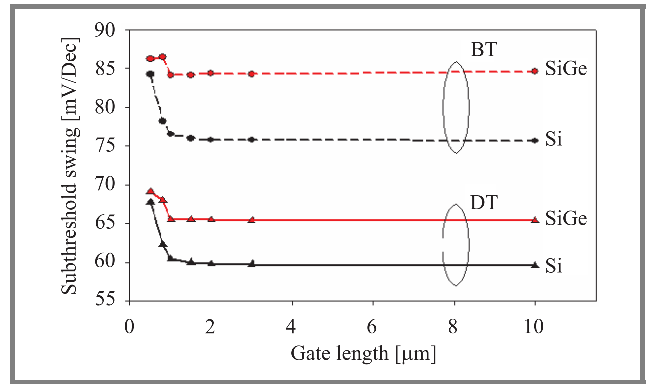

Fig. 8. Subthreshold swing in body tied and dynamic threshold modes as a function of gate length.

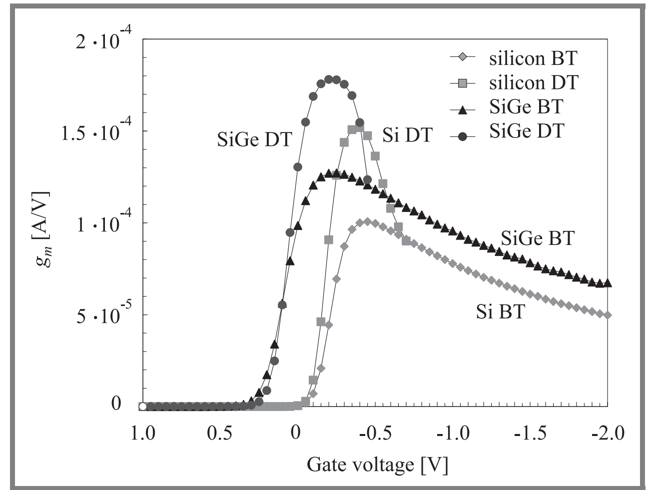

Fig. 9. Transconductance (g_m) as a function of gate voltage, showing particular enhancement in DT operation ($L = 3$ μm, $W = 160$ μm, $V_{DS} = -50$ mV).

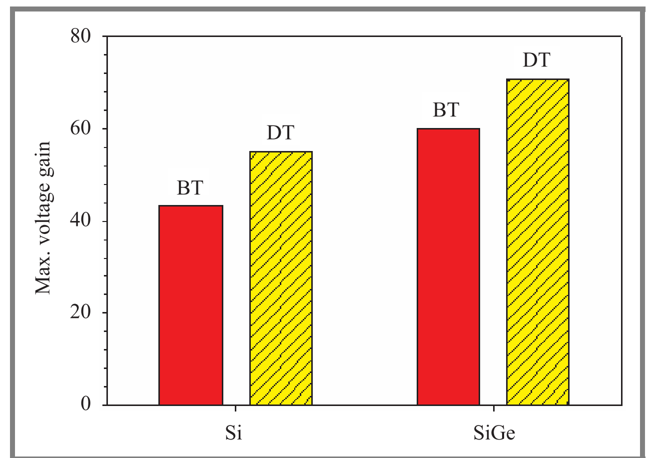

Fig. 10. Maximum voltage gain improved both by alloy channel and operation in DT mode.

Haendler *et al.* [8] predict a transconductance enhancement factor $(1+\eta)$ with $\eta = dV_T/dV_G$, where V_T is the threshold voltage and V_G is the gate voltage. We can extract values of γ from the experimental data in two

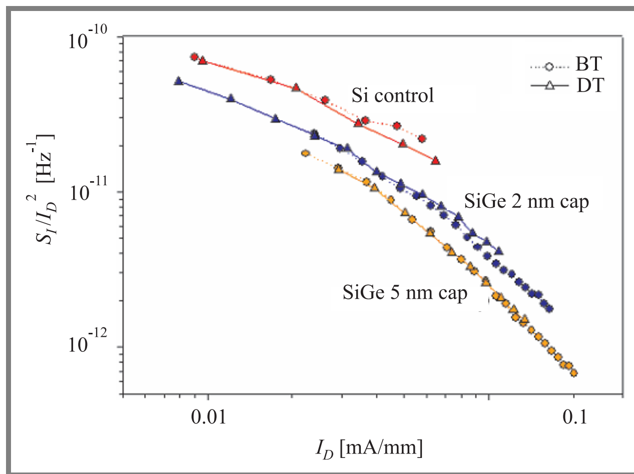

Fig. 11. Normalised current noise power spectral density at 1 Hz showing no variation between BT or DT mode for any of the devices studied ($V_{DS} = -50$ mV, $L = 40$ μm, $W = 40$ μm).

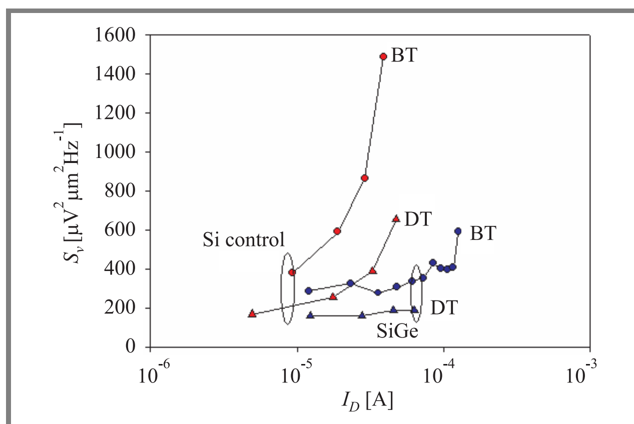

Fig. 12. Input referred voltage noise at 1 Hz, $S_v = S_I/g_m^2$. The enhanced g_m reduces S_v ($L = 3$ μm, $W = 160$ μm, $V_{DS} = -50$ mV).

ways: from the ratio of peak transconductance (Fig. 9), $\eta = 0.52$ for the Si device and 0.34 for SiGe, whereas from the threshold voltage shift with gate voltage, $\eta = 0.26$ and 0.30, respectively. A possible explanation for this discrepancy in the Si case lies in the original paper on DT action by Assaderaghi *et al.* [9], in which it is noted that the effective field is lowered by DTMOS action, which could lead to enhanced mobility and impact beneficially on transconductance. As pointed out by Takagi *et al.* [10], a SiGe device will have a larger value of η for the same threshold voltage, which points the way to further improvements in noise performance for a suitably designed DT mode device.

5. Conclusions

Measurements of $1/f$ noise in Si and Si/SiGe/Si MOSFETs have been compared with theoretical models of carrier number fluctuations due to tunnelling into the gate oxide. Analysis of the data suggests that the reduced noise in the heterostructure device as compared to Si is primarily associated with an energy dependent density of oxide trap states and a displacement of the Fermi level at the SiO_2/Si interface in the heterostucture relative to the Si control. High transconductance associated with dynamic threshold mode operation will further lower the input referred voltage noise, offering important benefits for circuit operation.

References

[1] M. J. Prest *et al.* "Low-frequency noise mechanisms in Si and pseudomorphic SiGe p-channel field-effect transistors", *Appl. Phys. Lett.*, vol. 85, pp. 6019–6021, 2004.

[2] M. J. Palmer *et al.*, "Effective mobilities in pseudomorphic Si/SiGe/Si p-channel metal-oxide-semiconductor field-effect transistors with thin silicon capping layer", *Appl. Phys. Lett.*, vol. 78, pp. 1424–1426, 2001.

[3] T. E. Whall and E. H. C. Parker, "Si/SiGe/Si pMOS performance – alloy scattering and other considerations", *Thin Solid Films*, vol. 368, pp. 297–301, 2000.

[4] X. Li and L. K. J. Vandamme, "1/f noise in series resistance of LDD MOSTs", *Solid State Electron.*, vol. 35, pp. 1471–1475, 1992.

[5] J. A. Chroboczek and G. Ghibaudo, "Low frequency noise in SiGe-base heterojunction bipolar transistors and SiGe-channel metal oxide semiconductor field effect transistors", *Microelectron. Reliab.*, vol. 40, pp. 1897–1903, 2000.

[6] A. Pacelli *et al.*, "Quantum effects on the extraction of MOS oxide traps by $1/f$ noise measurements", *IEEE Trans. Electron Dev.*, vol. 46, pp. 1029–1035, 1999.

[7] S. Martin, G. P. Li, H. Guan, and S. D'Souza, "A BSIM3-based flat-band voltage perturbation model for RTS and $1/f$ noise", *IEEE Electron Dev. Lett.*, vol. 21, pp. 30–33, 2000.

[8] S. Haendler, J. Jomaah, G. Ghibaudo, and F. Balestra, "Improved analysis of low frequency noise in dynamic threshold MOS/SOI transistors", *Microelectron. Reliab.*, vol. 41, pp. 855–860, 2001.

[9] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI", *IEEE Trans. Electron Dev.*, vol. 44, pp. 414–422, 1997.

[10] T. Takagi, A. Inoue, Y. Hara, Y. Kanzawa, and M. Kubo, "A novel high performance SiGe channel heterostructure dynamic threshold pMOSFET (HDTMOS)", *IEEE Electron Device Lett.*, vol. 22, pp. 206–208, 2001.

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