Paper

Applying shallow nitrogen implantation from rf plasma for dual gate oxide technology

Tomasz Bieniek, Romuald B. Beck, Andrzej Jakubowski, Grzegorz Głuszko, Piotr Konarski, and Michał Ćwil

Abstract—The goal of this work was to study nitrogen implantation from plasma with the aim of applying it in dual gate oxide technology and to examine the influence of the rf power of plasma and that of oxidation type. The obtained structures were examined by means of ellipsometry, SIMS and electrical characterization methods.

Keywords—CMOS, dual gate oxide, gate stack, oxynitride, plasma implantation.

1. Introduction

According to the ITRS roadmap [1] the reduction of the gate dielectric thickness is one of the ways to ensure the increasing level of packing and performance of silicon integrated circuits. In mixed logic/memory circuits manufactured as system on a chip, two different thicknesses of dielectric layers are required. The most advanced solution would be to form both dielectric layers simultaneously, in a single process. This may be possible if oxidation of a silicon layer is preceded with local nitrogen implantation, since the rate of oxidation depends on the nitrogen implantation dose and its profile (e.g., [2, 3]).

The experiments presented in this work are a part of a broader study that examines the possibility of fabricating very thin dielectric layers using ultrashallow nitrogen implantation from rf plasma. As opposed to the methods presented in the literature so far, where classical implanters or the IIIP technique were used for ultrashallow implantation, our process is performed in a typical Oxford plasma technology plasma enhanced chemical vapour deposition (PECVD) planar plasma reactor. The choice of nitrogen source and process parameters for plasma implantation was based on the results of previous studies [4–6].

In this work nitrogen implantation carried out from NH_3 plasma has been immediately followed by either thermal or plasma oxidation process. In this way the influence of oxidation type could be examined.

The aim of this work was to study the feasibility of dual gate oxide technology (Fig. 1) based on rf plasma implantation, as well as to investigate the influence of rf power during implantation and that of oxidation type (conventional versus plasma).

The thickness and nitrogen profile of the obtained layers were investigated by means of ellipsometry and secondary ion mass spectrometry (SIMS) measurements. Test structures were fabricated using NMOS technology with Al gate and electrical characterization was performed to determine selected electrophysical parameters, such as: effective charge and interface trap density, insulating properties and breakdown behavior.

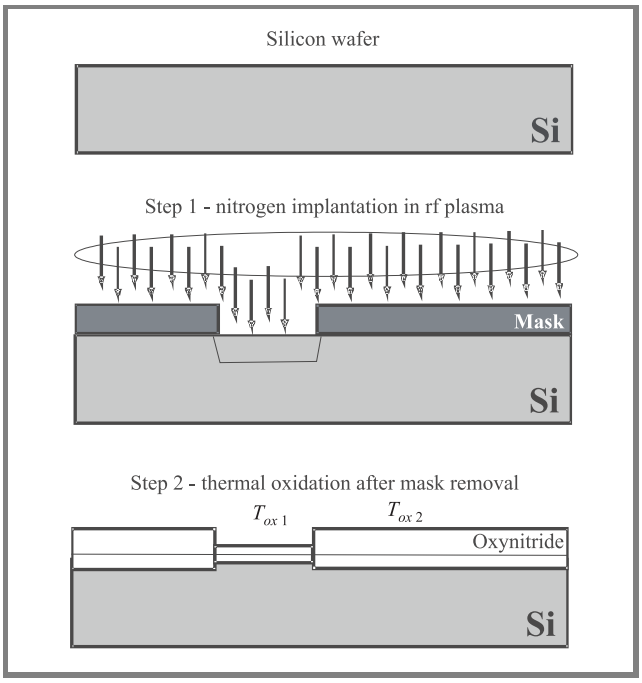


Fig. 1. Dual gate oxide technology – two oxynitride layers with different thickness obtained in a single oxidation process.

2. Experimental

The experiments in this study were carried out in two steps. In the first one, the process of nitrogen implantation from ammonia (NH_3) plasma was performed at 350°C in a PECVD system. The rf power was varied between 100 W, 200 W and 300 W. In the second step, the samples were oxidized either thermally or using a plasma process. Thermal oxidation was performed in dry oxygen diluted in argon (50 ml/min O_2 in 1 l/min Ar) at 1000°C (samples 2–4 in Table 1). Low temperature (350°C) plasma oxidation was performed in oxygen at rf power of 100 W (sample 6 in Table 1). The parameters of thermal and plasma oxidation were chosen based on the results of previous studies [4–6].

Table 1
Summary of process parameters

Parameters	Only thermal oxidation	100 W implantation + thermal oxidation	200 W implantation + thermal oxidation	300 W implantation + thermal oxidation	Only plasma oxidation	100 W implantation + plasma oxidation
Sample no.	1	2	3	4	5	6
Step 1 – nitrogen plasma ion implantation, 350°C, NH_3						
Implantation	no	yes	yes	yes	no	yes
Rf power [W]	no	100	200	300	no	100
Step 2 – oxidation						
Type	Thermal, dry oxygen diluted in Ar, 1000°C				Plasma, 350°C	

Table 2
Results of electrical characterization of NMOS test structures

Parameters	Only thermal oxidation	100 W implantation + thermal oxidation	200 W implantation + thermal oxidation	300 W implantation + thermal oxidation	Only plasma oxidation	100 W implantation + plasma oxidation
Sample no.	1	2	3	4	5	6
Optical thickness D_{ox_opt} [Å]	93	55	49	53	40	40
EOT from *C-V* (@1 MHz)	104	60	38	89	46	75
Effective dielectric constant ε_{eff}	3.4	3.4	4.6	2.2	3.3	2.0
D_{itmb} [1/eV cm^2]	$3.21 \cdot 10^{12}$	$4.93 \cdot 10^{12}$	$8.93 \cdot 10^{12}$	$4.11 \cdot 10^{12}$	$6.19 \cdot 10^{12}$	$3.12 \cdot 10^{12}$
Q_{eff}/q [cm^{-2}]	$4.82 \cdot 10^{11}$	$9.35 \cdot 10^{11}$	$3.12 \cdot 10^{12}$	$1.64 \cdot 10^{12}$	$1.34 \cdot 10^{12}$	$6.93 \cdot 10^{12}$
$Q_{eff}/q/D_{ox\_opt}$ [1/cm^2 Å]	$5.35 \cdot 10^{9}$	$1.70 \cdot 10^{10}$	$6.37 \cdot 10^{10}$	$3.10 \cdot 10^{10}$	$3.36 \cdot 10^{10}$	$1.73 \cdot 10^{11}$
Q_{eff} [C/cm^2]	$7.71 \cdot 10^{-8}$	$1.50 \cdot 10^{-7}$	$5.00 \cdot 10^{-7}$	$2.63 \cdot 10^{-7}$	$2.15 \cdot 10^{-7}$	$1.11 \cdot 10^{-6}$
U_{FB} [V]	–1.15	–1.20	–1.48	–1.60	–1.21	–3.34
E_{BR} [MV/cm] (50%)	13.2	11.3	12.0	19.2	13.8	13.8

To have the necessary reference data, two samples were subjected to either thermal (sample 1) or plasma (sample 5) oxidation only (no nitrogen implantation). The technological experiments performed in the course of this study are summarized in Table 1.

Thickness and composition of the obtained layers were then studied by means of ellipsometry, and ULE-SIMS (ultra-low-energy-SIMS), while electrophysical properties were evaluated based on electrical characterization (*C-V* and *I-V* characteristics analysis) of NMOS test structures with the investigated ultra-thin silicon oxynitride layers as gate dielectric.

3. Results

The results obtained in this work and summarized in Tables 1 and 2 confirm that nitrogen implantation does takes place even at very low rf plasma energies (even at 100 W – see Fig. 2). Subsequent thermal oxidation formed ultra-thin oxynitride layers with the composition and thickness dependent on the conditions of the implantation process.

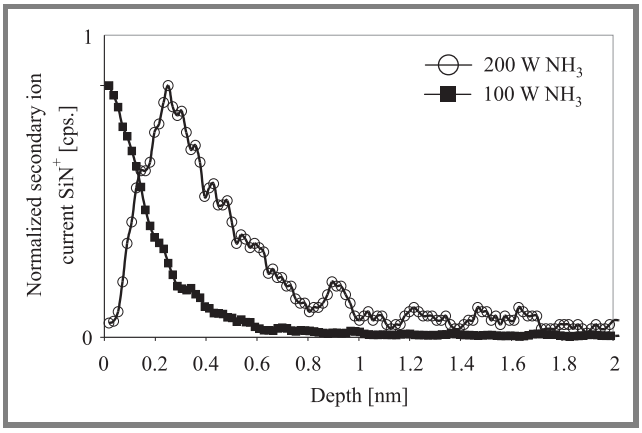


Fig. 2. Examples of nitrogen profiles of the layers formed by means of nitrogen implantation at different levels of rf power followed by plasma oxidation as obtained from ULE-SIMS [7].

During oxynitride layer formation two contradictory effects have significant influence upon the composition and final thickness of the layer.

Nitrogen implantation results in a significant decrease of the thermal oxidation rate, as can be seen in Table 2 (compare the thickness of all nitrogen implanted and thermally oxidized samples with that of sample 1).

Results obtained by ULE – SIMS (see Fig. 2) demonstrate that both, nitrogen profile and content may be controlled by rf plasma power used for implantation. Depending on this power the maximum of the nitrogen profile may be located just at the top surface of the layer or still within the layer – no further than 1.0 nm from its top (see Fig. 2).

A profile of this depth is difficult (if not impossible) to obtain by other techniques. The depth correlates well with the desired final thickness of the oxynitride layer. This means that when the formation of ultra-thin oxynitride layer is finished (that is after oxidation) the nitrogen profile will not extend into the device channel region.

Analysis of electrical characteristics of NMOS test structures indicates correlation between rf power used for nitrogen implantation and electrical properties of the Si/SiO_xN_y system.

Ellipsometric measurements indicate crucial difference between the thermal and plasma oxidation. For plasma oxidation no difference between the implanted and non-implanted samples was observed (see Table 2) while for thermal oxidation big difference between the implanted and non-implanted samples can be noticed. Almost no difference may, however, be noticed between the implanted samples despite varying rf power used. The whole picture changes if the electrical thickness is taken into consideration.

The equivalent oxide thickness (EOT) values (electrical thickness evaluated from the high frequency *C-V* characteristics assuming the dielectric permittivity is that of silicon dioxide) depend on rf power during implantation. The obvious and intuitive explanation to this observation is that this reflects the dependence of the efficiency of the nitrogen implantation (thus, the composition of the layer) on implantation conditions. In fact a comparison of the optical thickness and EOT leads to the conclusion that the effective dielectric constant of the layer is higher than that of thermal oxide only in one case (implantation at 200 W), which can be attributed to the significant presence of nitrogen in the layer (see Table 2). For the other cases, i.e., 100 W and 300 W, as well as the reference one, the effective dielectric constant values are lower than that of thermal oxide.

The case of thermal oxide proves that one should treat this comparison with highest care[1]. It is our strong belief that we should refer in our discussion to the observed trends in the effective dielectric constant values, rather than to the absolute values.

Following this approach one notices that the effective dielectric constant reaches maximum in the 200 W case. The dramatic drop of this parameter for 300 W could be interpreted as too much damage caused by nitrogen implantation during the first stage of layer formation. It is interesting, however, to realize that sample 4 has proved to be overall superior (as will be shown below) to all the other samples in terms of electrical properties (the lowest leakage current, highest critical electric field, well defined *C-V* curve and relatively low charge densities). The reason of this discrepancy is not yet known.

For plasma oxidized samples the situation is different. Although, as mentioned above, the optical thickness of the layer is the same, the EOT values differ significantly. Remembering the discussion presented above we may still state that some changes in the layer composition must take place as a result of nitrogen plasma implantation prior to plasma oxidation. Although such a drastic change in EOT would certainly be good enough to obtain satisfactory dual gate oxide technology, its value decreases instead of its required rise. Thus, instead of relaxing technological problems with formation of ultra-thin gate dielectric layer, application of this method to perform dual gate oxide technology would create even more serious difficulties.

Typical electrical characteristics of NMOS test devices manufactured for the purpose of this study are presented in Figs. 3–5. High frequency *C-V* curves are shown in Fig. 3. In general, the differences in maximum capacitance are the obvious consequence of different thickness and composition of the studied oxynitride layers and – to a certain extent – of different leakage currents. In order to

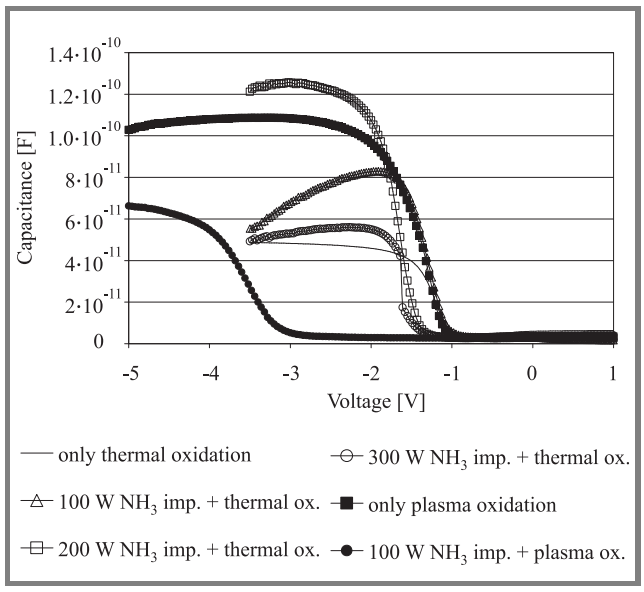


Fig. 3. High frequency (1 MHz) *C-V* curves of NMOS test structures with the gate dielectric layers produced under different plasma parameters (varied rf power and oxidation type – see Table 1).

[1]The optical thickness is evaluated from the ellipsometric measurements assuming silicon dioxide refractive index value, due to the low sensitivity of the ellipsometric curves for very low layer thickness. EOT, on the other hand, is evaluated assuming the dielectric constant of thick film thermal silicon dioxide. Neither of the two assumptions is true in the case of the examined samples, even for the reference sample 1 (this is only 10 nm layer). In fact, the significant decrease in the sensitivity of ellipsometric curves makes the former assumption certainly less critical than the latter. One should also keep in mind that for ultra-thin layers optical thickness tends to differ (is usually smaller) from electrical thickness (evaluated from *C-V* curves).

prevent the errors in EOT and all other electrical parameter calculations we used the estimation method of $C_{\max}$ as presented in [8]. A simple and intuitively obvious dependence has also been found between rf plasma power and the densities of the effective charge Q_{eff} interface traps at midgap D_{itmb}. Both parameters show maximum at 200 W. In fact, sample 4 (rf during plasma implantation 300 W) has superior trapping and effective charge density to all other samples subjected to the plasma implantation and only marginally worse than those of the reference thermal oxide. This result is promising for the dual gate oxide technology.

For plasma oxidation case, the situation is more complicated. Although the systems resulting from plasma nitrogen implantation and plasma oxidation are on a par with reference thermal oxide in terms of trapping properties, the effective charge density is certainly the highest among all samples studied (more than one order of magnitude higher than in the reference thermally oxidized gate oxide).

Typical *I-V* curves of individual samples studied in this work are shown in Fig. 4. The analysis of *I-V* curves yields a surprising result. Samples implanted at the highest rf power (300 W; sample 4) have the best insulating properties, better even than the reference thermal oxide (especially for high electric fields). Samples prepared using only plasma processes, that is plasma oxidation only (sample 5) or plasma implantation followed by plasma oxidation (sample 6) exhibit comparable *I-V* behavior, similar also to that of sample 1 (thermal oxidation only) for medium and higher electric fields, although their current is almost two orders of magnitude higher for low electric fields. Samples 2 and 3, implanted at 100 W and 200 W of rf power exhibit the highest leakage currents.

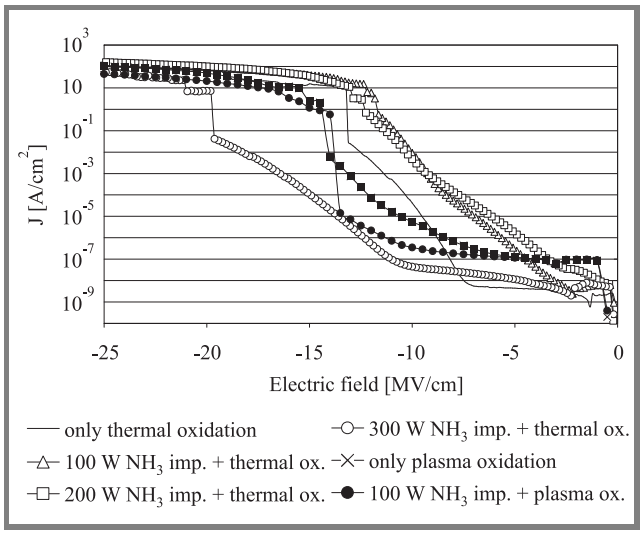


Fig. 4. The *I-V* curves of NMOS test structures; gate dielectric layers were produced with different process parameters (varied rf power and oxidation type – see Table 1).

In all studied samples breakdown events were well defined, thus the Weibull plots could be created for each sample (see Fig. 5). Oxynitride layer formed by means of implantation from NH_3 at 300 W and subsequent thermal oxidation (sample 4) was the best in terms of critical electric field with E_{BR} as high as 19 MV/cm. E_{BR} values of other samples vary between 11 MV/cm and 14 MV/cm (see Table 2). This means that in each case, the breakdown properties of the obtained SiON layers are superior to the defect free thermal oxides (10 MV/cm). It is interesting to realize that the plots for samples that underwent plasma oxidation are almost identical, whether they were or not subjected to nitrogen implantation.

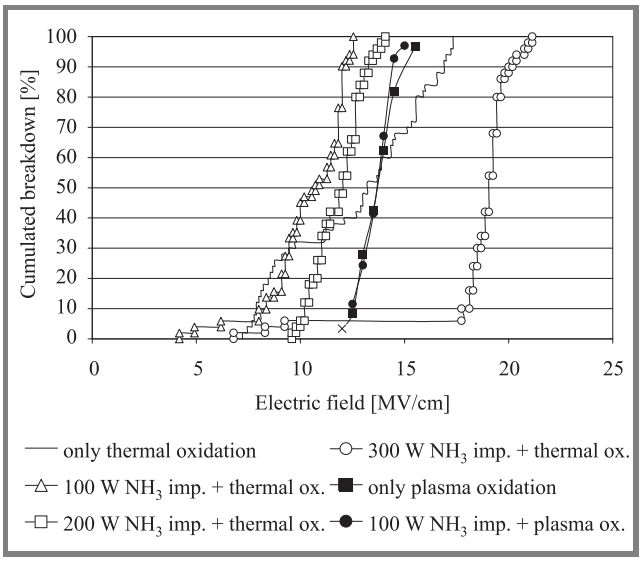


Fig. 5. Weibull plots of NMOS test structures; gate dielectric layers were produced with different process parameters (varied rf power and oxidation type – see Table 1).

Another interesting feature of the presented Weibull plots is their abruptness indicating that for each layer type all breakdowns took place under similar stressing voltage conditions. Therefore, it may be concluded, that we are dealing with intrinsic breakdown (characteristic of layers with almost no defects) or with one caused by one type of defects only (in the case where the intrinsic breakdown field is even higher for this type of material).

4. Summary

The experiments performed indicate that dual gate oxide technology based on ultrashallow implantation of nitrogen is feasible. From the two approaches to dual gate oxide technology studied in this work, the combination of nitrogen implantation with thermal oxidation is definitely more promising, because significant reduction of the final oxynitride layer thickness due to plasma implantation was observed.

Variation of rf power indicates that the highest investigated value of this parameter (300 W) results in a superior quality of the ultra-thin gate dielectric layer, comparable with that of non-implanted samples (trapping and effective charge density) and in certain aspects – leakage currents and critical electric field – even much better.

Although the plasma implantation does not degrade the properties in plasma oxidized samples (leakage currents, critical electric field, trapping) except for the effective charge density, the observed decrease in EOT seems to eliminate this method from the list of candidates for implementation for dual gate oxide technology in the future. On the basis of the results obtained in this study, it may be concluded that effective plasma implantation reduces the leakage current, especially at medium and high electric field, leading to significant improvement in breakdown properties (E_{BR} reaching 19 MV/cm). This effect may be of great value for future CMOS technologies, which suffer a lot from the leakage and reliability issues.

Acknowledgements

This work has been funded partly by the European Commission under the frame of the Network of Excellence SINANO (Silicon-based nanodevices, IST-506844) and partly by Polish Ministry of Science and Higher Education under the contract no. 3T11B 020 30.

References

[1] International Technology Roadmap for Semiconductor, http://public.itrs.net

[2] T. Chevolleau, A. Szekeres, and S. Alexandrova, "Oxidation of N implanted silicon: optical and structural properties", *Surf. Coat. Technol.*, vol. 151–152, pp. 281–284, 2002.

[3] R. Rajkumer, M. Kumar, P. J. George, S. Mukherjee, and K. S. Chari, "Effects of nitrogen and argon plasma – immersion ion implantation on silicon and its oxidation", *Surf. Coat. Technol.*, vol. 156, no. 1–3, pp. 253–257, 2002.

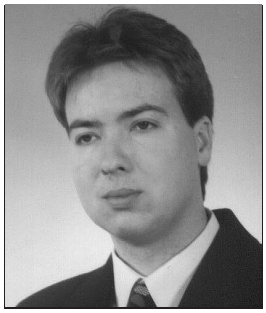
[4] T. Bieniek, R. B. Beck, A. Jakubowski, and A. Kudła, "Formation of ultra-thin oxide layers by low temperature oxidation in r.f. plasma", *Elektronika*, vol. 10, pp. 6–7, 2004.

[5] T. Bieniek, R. B. Beck, A. Jakubowski, and A. Kudła, "Study of extremely shallow nitrogen ions implantation in planar r.f. plasma reactors", *Elektronika*, vol. 2–3, pp. 9–10, 2005.

[6] T. Bieniek, A. Wojtkiewicz, L. Łukasiak, and R. B. Beck, "Silicon dioxide as passivating, ultrathin layer in MOSFET gate stacks", *J. Wide Bandgap Mater.*, vol. 8, no. 3–4, pp. 201–209, 2002.

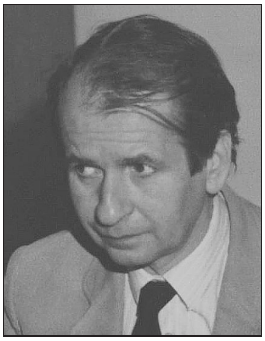
[7] T. Bieniek, R. Beck, A. Jakubowski, P. Hoffmann, D. Schmeisser, P. Konarski, and M. Cwil, "Formation of pedestal oxynitride layer by extremely shallow nitrogen implantation in planar r.f. plasma reactor", *ECS Trans*., vol. 1, no. 5, pp. 407–419, 2006.

[8] B. Majkusiak and A. Jakubowski, "A technical formula for determining the insulator capacitance in a MOS structure", *Solid State Electron.*, vol. 35, no. 2, pp. 223–224, 1992.

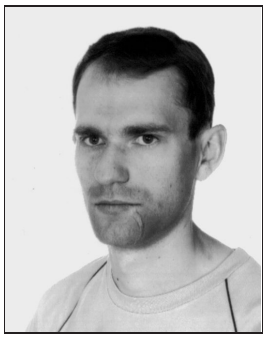


Tomasz Bieniek was born in Warsaw, Poland, in 1977. He received the M.Sc. degree from Warsaw University Technology in 2002 and Ph.D. degree in 2007. His research area concentrates on plasma processes for CMOS-VLSI technology, especially in very thin and ultra-thin dielectric layers. Since 2006 he is working in Institute of Electron Technology.
e-mail: tbieniek@elka.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland
e-mail: tbieniek@ite.waw.pl
Institute of Electron Technology
Lotników av. 32/46
02-669 Warsaw, Poland

Romuald B. Beck received the M.Sc. degree in electronics from the Faculty of Electronics, Warsaw University of Technology, Poland, in 1976. From the same university, he received the Ph.D. and D.Sc. degrees in 1982 and 1996, respectively. Since 2000 he occupies the post of Professor. Since 2005 he has been heading Microelectronic and Nanoelectronic Devices Division. His research activities have been concentrated in the area of modeling, diagnostics and technology of the metal-insulator-semiconductor devices with very thin and ultra-thin oxides, dielectric layers formation methods, their kinetics and the relations between the process kinetics and the electrophysical properties of the devices, their yield and their reliability, dry etching methods and their implementation to modern ICs technology.
e-mail: r.beck@elka.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland

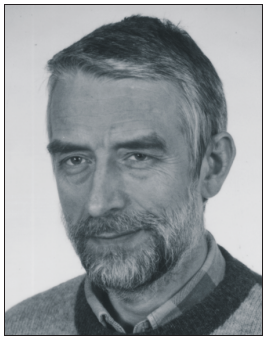


Andrzej Jakubowski received the M.Sc., Ph.D. and D.Sc. degrees in electrical engineering from the Warsaw University of Technology (WUT), Poland. At present Professor Jakubowski is the Head of the Institute of Microelectronics and Optoelectronics (WUT). His main research interests include modeling and characterization of semiconductor devices and integrated circuits. He is author and co-author of more than 300 papers, several books and textbooks.
e-mail: jakubowski@imio.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland



Grzegorz Głuszko was born in Biłgoraj, Poland, in 1976. He received the B.Sc. and M.Sc. degrees in microelectronics from Warsaw University of Technology, Poland, in 2002 and 2004, respectively. Since then he has been working on a Ph.D. thesis concerning characterization of novel MOS devices. His research interests include charge pumping studies of the quality of silicon-silicon dioxide interface, as well as modeling of MOS devices.

ggluszko@elka.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland



Piotr Konarski received the M.Sc. degree from the Chemistry Department of Warsaw University in 1976 and Ph.D. degree from the Institute of Electron Technology, Poland, in 1997. He is the Head of Vacuum Instruments Laboratory at Industrial Institute of Electronics in Warsaw. He performs applied research in the areas relating to: vacuum technology, surface physics, secondary ion mass spectrometry, glow discharge mass spectrometry and depth profile analysis. He is a member of The Polish Fulbright Alumni Association and Polish Vacuum Society.

e-mail: piotr.konarski@pie.edu.pl
Industrial Institute of Electronics
Długa st 44/50
00-241 Warsaw, Poland

Michał Ćwil was born in Warsaw, Poland, in 1979. He received the M.Sc. degree in physics from the Faculty of Physics, Warsaw University of Technology in 2003, where he is currently working on his Ph.D. degree in the field of electrical characterization of CIGS solar cells. He is also a specialist in secondary ion mass spectrometry. Currently he is an Assistant at the Industrial Institute of Electronics in Warsaw.

e-mail: cwil@if.pw.edu.pl
Industrial Institute of Electronics
Długa st 44/50
00-241 Warsaw, Poland

Faculty of Physics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland