Paper

Characterization of SOI MOSFETs by means of charge-pumping

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Abstract—This paper presents the results of charge-pumping measurements of SOI MOSFETs. The aim of these measurements is to provide information on the density of interface traps at the front and back Si-SiO_2 interface. Three-level charge-pumping is used to obtain energy distribution of interface traps at front-interface.

Keywords—charge-pumping, electrical characterization, interface traps, SOI MOSFET.

1. Introduction

Silicon-on-insulator (SOI) technology has several well-known advantages over classical bulk technology, e.g., enhanced current, ideal subthreshold slope, reduced short channel effects and lower junction capacitance [1], as well as superior mobility and decreased power consumption [2]. Moreover, it is immune to latch-up effects, while complete isolation of devices and feasibility of high-resistivity substrate result in reduced substrate-loss for RF applications [3]. The performance of SOI MOSFETs is, however, determined to a large extent by the quality of the top and bottom SiO_2-Si interface. Therefore in this paper the quality of these interfaces is studied by means of charge-pumping (CP) [4].

2. Investigated structures

SOI MOSFETs with body contacts (BC) have been fabricated on SOITEC substrates with an initial top-silicon thickness of $t_{SOI} = 100$ nm and a buried oxide (BOX) thickness of $t_{BOX} = 200$ nm (see schematic Fig. 1a). Top-silicon layers have been doped by boron ion implantation and subsequent annealing to achieve one sample with a nominal channel doping of $N_{ch} = 10^{17}/\text{cm}^3$ and two samples with $N_{ch} = 10^{18}/\text{cm}^3$. Channel regions including source, drain and body contacts have been defined by mesa isolation using inductive coupled plasma reactive ion etching (ICP-RIE) with a two step HBr/O_2 process [5]. After a modified RCA clean, a thermal gate oxide with a thickness of $t_{ox} = 8.5$ nm has been grown at 900°C. Subsequently, polysilicon with a thickness of $t_{poly} = 150$ nm has been deposited by low pressure chemical vapor deposition (LPCVD). Polysilicon has been removed completely except from the gate and BC regions by ICP-RIE, again with a two step HBr/O_2 process [5]. Source and drain have been completed by self aligned arsenic (n^+) ion implantation and rapid thermal annealing (RTA). BCs have been uncovered by ICP-RIE with a two step HBr/O_2 process [5]. The etch mask has then been used in a self aligned manner to dope the BC leads by boron (p^+) ion implantation and RTA.

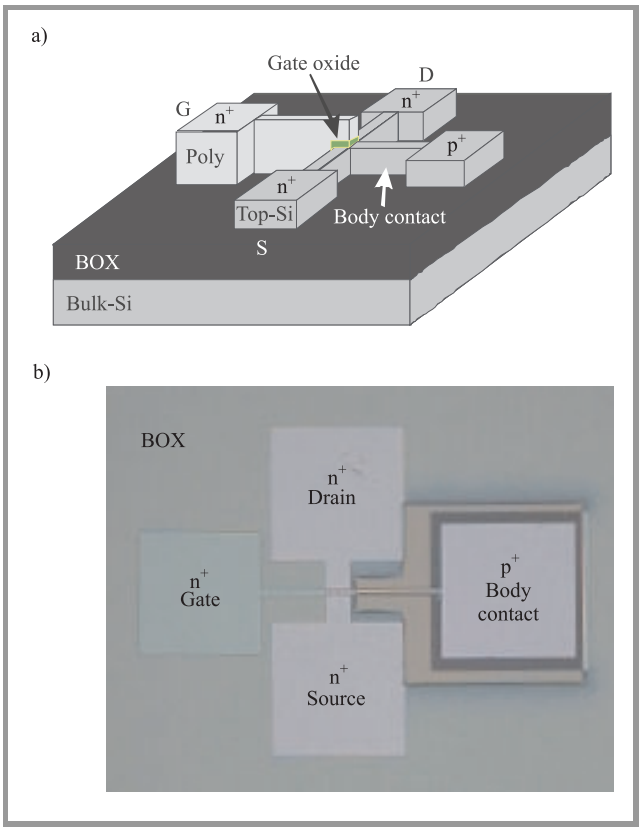

Fig. 1. SOI MOSFET with body contact: (a) schematic; (b) microscope image.

Forming gas annealing in N_2/H_2 for 30 min at 400°C to cure oxide and interface charges has been applied to one sample with $N_{ch} = 10^{18}/\text{cm}^3$. A microscope image of a fabricated device is shown in Fig. 1b. Gate length and gate width are $L_g = 10\,\mu$m and $W = 20\,\mu$m, respectively.

3. Charge-pumping measurements

This section is divided into three parts. The first two are devoted to characterization of front- and back-interface by means of two-level charge-pumping, while the third presents preliminary results of front-interface studies using three-level charge-pumping.

3.1. Two-level charge-pumping – front-interface

Front-interface charge-pumping curves were measured for different values of back-gate bias V_{GB}. Comparison of these curves indicates that no or very weak interface coupling takes place at $V_{GB} = -30$ V, therefore all subsequent measurements of front-interface CP current were carried out at this back-gate bias. The influence of source-body and drain-body junction reverse bias on front-interface CP current is illustrated in Fig. 2. In the case of non-annealed structures significant geometric component is observed for $V_D = V_S < 0.5$ V. This is most probably due to considerable resistance of the body contact. As a result, all subsequent measurements on these structures were made at $V_S = V_D = 0.5$ V.

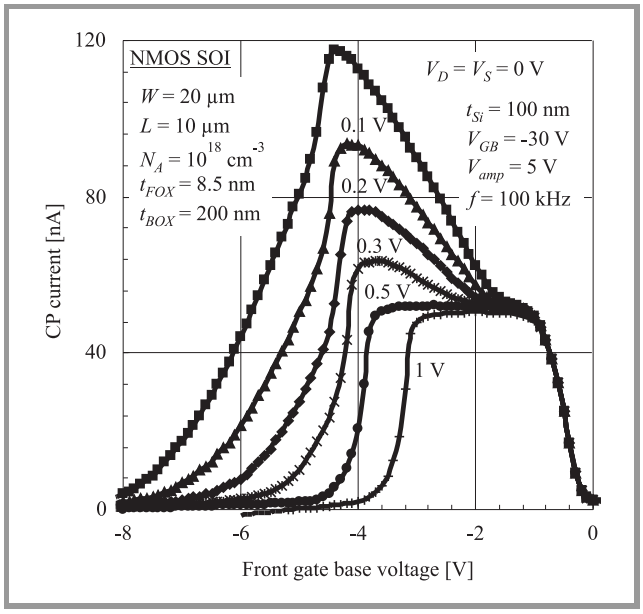

Fig. 2. Front-interface CP current as a function of front-gate base voltage with source-body and drain-body junction bias as a parameter.

An example of CP current measured on structures with body doping of 10^{17} cm^{-3} is shown in Fig. 3a as a function of front-gate base voltage with gate voltage amplitude as a parameter.

The fact that the middle part of each curve is not perfectly flat is probably due to the fact that the resistance of the body contact is considerable due to a relatively low body thickness.

Table 1
Parameters determined from 2-level charge-pumping measurements

Structure type	N_{it} [cm^{-2}]	V_{FB} [V]	V_T [V]
$N_{body} = 10^{17}$ cm^{-3}	$1.7 \cdot 10^{12}$	−0.5	1.1
$N_{body} = 10^{18}$ cm^{-3} (non-annealed)	$2.0 \cdot 10^{12}$	−0.4	1.5
$N_{body} = 10^{18}$ cm^{-3} (annealed)	$8.4 \cdot 10^{10}$	−1.0	0.0

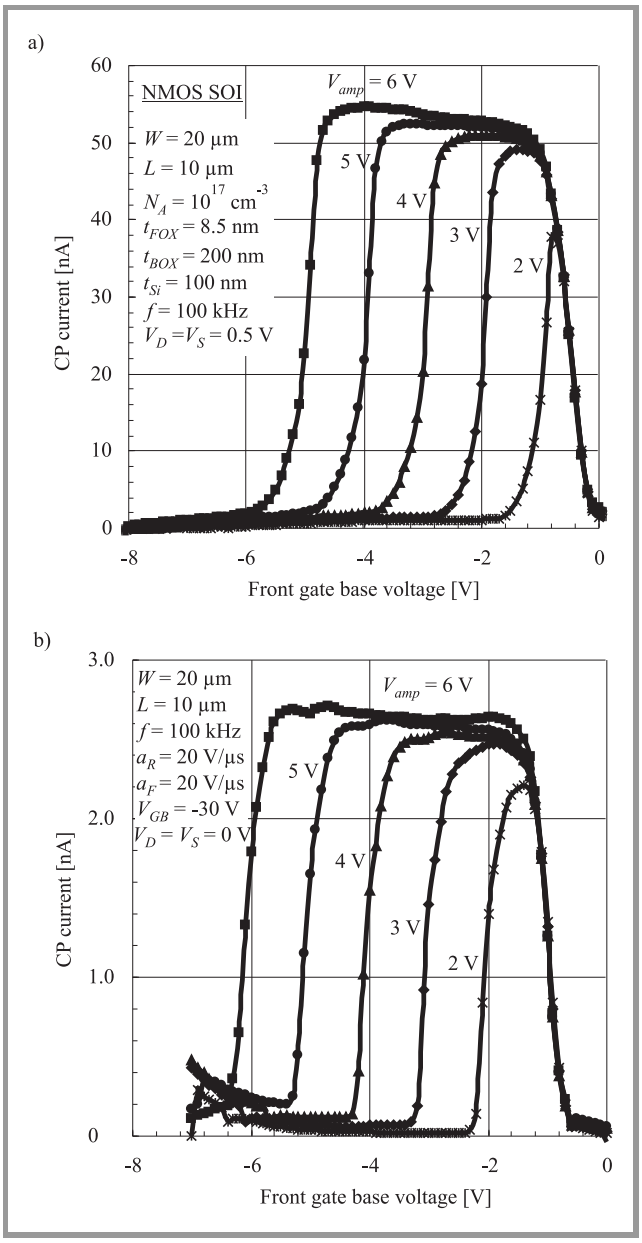

Fig. 3. Front-interface CP current as a function of front-gate base voltage with gate voltage amplitude as a parameter: (a) $N_{body} = 10^{17}$ cm^{-3}; (b) $N_{body} = 10^{18}$ cm^{-3}, annealed.

In the case of annealed structures with body doping of 10^{18} cm^{-3} the CP current is more than an order of magnitude lower, which can be seen in Fig. 3b. Moreover, reverse bias of source and drain junctions is not necessary in this case.

Analysis of the obtained CP curves yields the total density of interface traps N_{it}, flatband voltage V_{FB} and threshold voltage V_T. Similar measurements were performed on both annealed and non-annealed structures with body doping of 10^{18} cm^{-3}. The results are listed in Table 1.

As expected, the lowest density of interface traps is obtained in the case of annealed structures with $N_{body} = 10^{18}$ cm^{-3}. Values of flatband and threshold voltages indicate that CP curves of this structure are shifted to the left

when compared to those of the other two structures. This difference is most probably due to the annealing process. The highest concentration of interface traps was found in non-annealed structures with $N_{body} = 10^{18}$ cm^{-3}. Since this structure type had the worst quality of front-gate interface, it was excluded from further investigations.

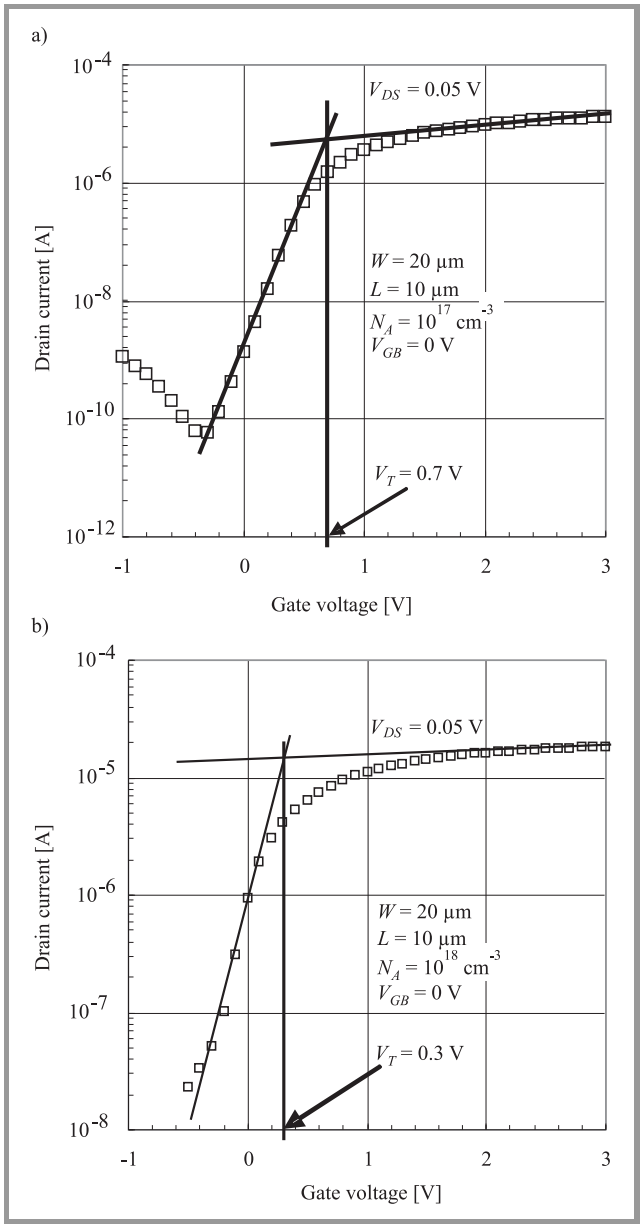

Fig. 4. Drain current as a function of gate voltage: (a) $N_{body} = 10^{17}$ cm^{-3}; (b) $N_{body} = 10^{18}$ cm^{-3}, annealed.

Extraction of flat-band and threshold voltages from CP curves yields only approximate values. For comparison threshold voltage was also determined from transfer characteristics of the drain current shown in Fig. 4 for devices with body doping of 10^{17} cm^{-3} and 10^{18} cm^{-3}, respectively.

It may be seen that values extracted from *I-V* curves are lower by approximately $0.3 - 0.4$ V, which is partly due to the fact that current was measured at $V_{GB} = 0$ V (much more natural operation conditions) instead of -30 V used in CP measurements to eliminate the contribution of the back-interface to CP current. On the other hand, both methods are in qualitative agreement indicating that threshold voltage of transistors with body doping of 10^{17} cm^{-3} is considerably higher than that of annealed devices with $N_{body} = 10^{18}$ cm^{-3}.

3.2. Two-level charge-pumping – back-interface

Similar analysis was performed for back-interface. To avoid interface coupling the front-interface was biased in accumulation ($V_{GF} = -2$ V). Typical CP curves obtained in the case of structures with $N_{body} = 10^{17}$ cm^{-3} and annealed

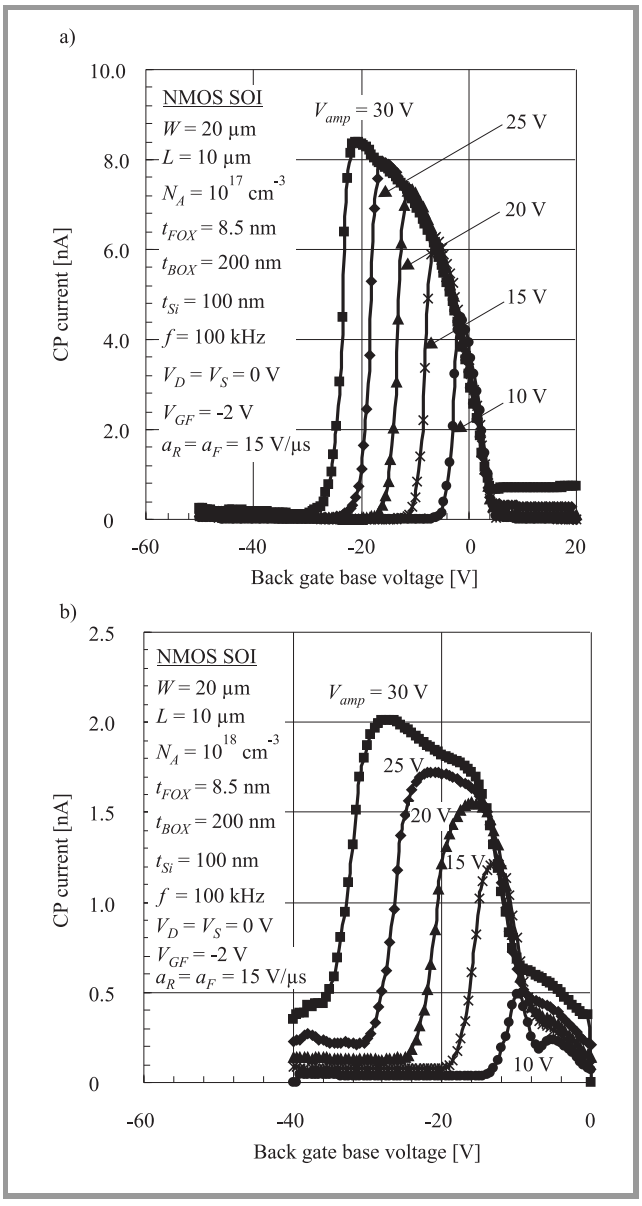

Fig. 5. Back-interface charge-pumping current versus back-gate base voltage with back-gate voltage as a parameter: (a) $N_{body} = 10^{17}$ cm^{-3}; (b) $N_{body} = 10^{18}$ cm^{-3}, annealed.

structures with $N_{body} = 10^{18}$ cm^{-3} are shown in Fig. 5, respectively. It may be seen that the maximum charge-pumping current does not saturate in either case. Using higher back-gate voltage amplitudes leads to a permanent damage to the structure. If N_{it} is determined from the highest CP current obtained, the results are approximately $2.8 \cdot 10^{11}$ cm^{-2} for $N_{body} = 10^{17}$ cm^{-3} and $1.2 \cdot 10^{10}$ cm^{-2} for $N_{body} = 10^{18}$ cm^{-3}. This is either much lower or comparable to the result obtained for front-interface (approximately $1.7 \cdot 10^{12}$ cm^{-2} or $8.4 \cdot 10^{10}$ cm^{-2}, respectively). Normally, back interface has considerably lower quality than the front-interface.

The obtained results could be due to the fact that the structures are damaged before the true maximum back-interface CP current is reached. It is interesting to note that the CP current is again much lower in the case of annealed structures with $N_{body} = 10^{18}$ cm^{-3}. This indicates that the annealing process could have influenced positively the quality of the back-interface, too.

3.3. Three-level charge-pumping – front-interface

Determination of the energy distribution of interface traps from 3-level CP measurements requires the knowledge of front-surface potential as a function of gate voltage. Appropriate simulations were performed using SILVACO/ATLAS software yielding both front and back surface potentials.

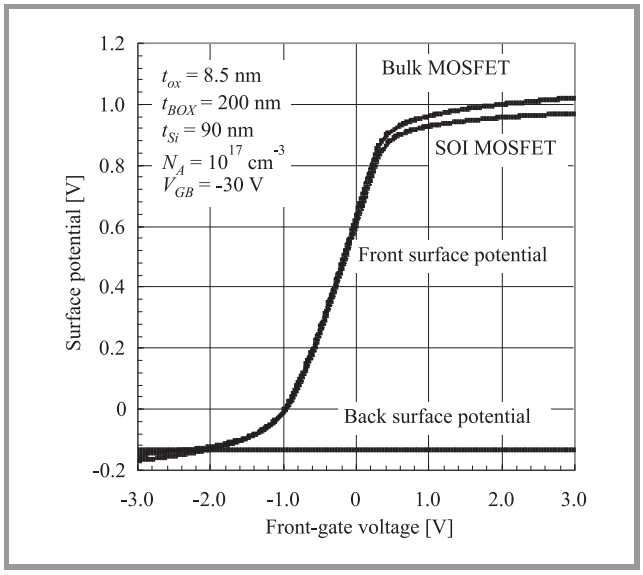

Fig. 6. Front and back surface potential of a SOI structure simulated as a function of front-gate voltage using SILVACO/ATLAS software (simple, numerical simulation of surface potential in a bulk MOSFET added for comparison).

The results are shown in Fig. 6 for body doping of 10^{17} cm^{-3}. For comparison, front-gate surface potential was also calculated in a classical way, that is assuming a bulk MOSFET (with the same gate-oxide thickness and substrate doping) instead of SOI one:

$$V_{GF} - V_{FB} = \frac{\mathrm{k}T}{q} \cdot G \cdot F(\varphi_s) + \varphi_s \,, \tag{1}$$

where: $\mathrm{k}T/q$ – thermal voltage, G – ratio of intrinsic semiconductor capacitance at flatband to gate-oxide capacitance, φ_s – surface potential and $F(\varphi_s)$ – the Kingston function.

It may be seen that the surface potential calculated according to Eq. (1) is in good agreement with that obtained from SILVACO/ATLAS, meaning that there is little coupling between the front and back-interface at $V_{GB} = -30$ V. Moreover, the back surface potential is almost constant in the investigated range of front-gate voltage, therefore

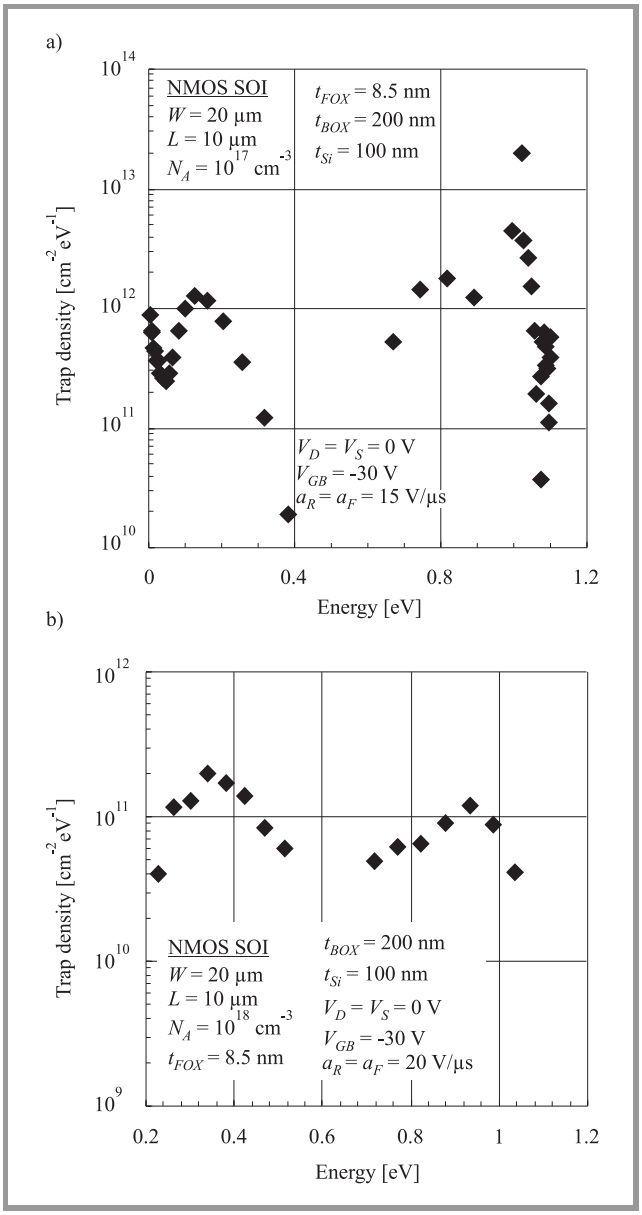

Fig. 7. Energy distribution of interface traps obtained from 3-level CP measurements: (a) $N_{body} = 10^{17}$ cm^{-3}; (b) $N_{body} = 10^{18}$ cm^{-3}, annealed.

back-interface does not contribute to charge-pumping current.

Formula (1) indicates that flatband voltage value is needed to obtain the relation between gate voltage and surface potential. The standard way to determine flat-band voltage from 2-level charge-pumping measurements is to find the front-gate base voltage at which the falling edge of the CP curve reaches half maximum (approximately, -0.5 V in this case). However, if this value is assumed for 3-level charge-pumping, the obtained results have no physical meaning. This is no surprise as the method of establishing V_{FB} value considered here is only a rough guess. Since the Authors of this paper had no other means to find the true value of V_{FB}, the process of determining trap energy levels was carried out for different values of flatband voltage until the region where no meaningful measurement results could be obtained coincided with the vicinity of midgap (trap time constants near midgap are very long, therefore CP current is too small to be measured accurately). This situation occurred at $V_{FB} = -0.98$ V. It may be seen in Fig. 3 that the transition between the flat part and the falling edge of the CP curve takes place at approximately this voltage.

The obtained energy distribution of interface traps is illustrated in Fig. 7. The region between 0.4 and 0.6 eV is too close to midgap to be measured using 3-level CP.

A similar energy distribution of interface traps is shown in Fig. 7a for annealed structures with body doping of 10^{18} cm^{-3}. In this case obtaining meaningful results requires assuming that flat-band voltage is -0.7 V (instead of -1.0 V extracted from 2-level CP measurements). It may be seen in Fig. 3b that -0.7 V is a voltage at which CP current practically falls to zero.

In view of the above energy distribution of interface traps presented in Fig. 7 may only be treated in qualitative terms. Further studies are required to develop an efficient method of V_{FB} extraction suitable for 3-level charge-pumping.

4. Summary

Charge-pumping measurements were performed on SOI MOS transistors with different body doping and subjected to different thermal processing. It was found that in all investigated structures the total density of interface traps at the back-interface was lower than that at the front-interface. This is probably due to the fact that the investigated devices were damaged before saturation of back-interface CP current could be obtained. It was found that annealing in N_2/H_2 at 400°C had a very positive effect on the quality of both front- and back-interface. Values of threshold voltage extracted from CP curves are in qualitative agreement with those obtained from transfer characteristics of drain current. Preliminary results of 3-level charge-pumping were presented, however further studies are needed to develop an appropriate method of flat-band voltage extraction suitable for this characterization technique.

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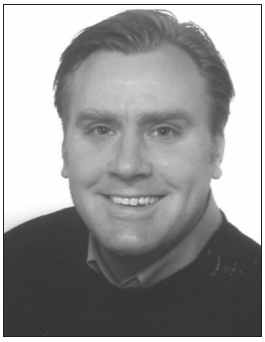

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