Paper

Charge-pumping characterization of FILOX vertical MOSFETs

Grzegorz Głuszko, Lidia Łukasiak, Enrico Gili, and Peter Ashburn

Abstract—This paper presents for the first time the results of charge-pumping (CP) measurements of FILOX vertical transistors. The aim of these measurements is to provide information on the density of interface traps at the Si-SiO_2 interface fabricated in a non-standard process. Flat-band and threshold voltage, as well as density of interface traps are determined. Good agreement between threshold-voltage values obtained from CP and *I-V* measurements is observed.

Keywords—charge-pumping, FILOX, interface traps, MOSFET, vertical MOSFET.

1. Introduction

Vertical transistors (VMOSFETs) offer increased packing density when compared to standard CMOS transistors at a defined technology node (e.g., [1]). So far several papers have appeared discussing the structure of a vertical transistor, fabrication method and performance (e.g., [2–4]). In terms of electrical characterization the analysis of standard *I-V* and *C-V* characteristics has been presented only.

Therefore, the aim of this paper is to address for the first time the issue of interface traps in vertical transistors through charge-pumping studies. While charge pumping measurements of power double-diffused vertical transistors (VDMOSFET) have been reported in, e.g., [5], the devices investigated in that work are totally different from those studied in this paper.

2. Experimental

The devices were fabricated by the University of Southampton using the self-aligned fillet (or spacer) local oxidation (FILOX) that enables a thin second field oxide to be grown in the active area without oxidizing the sidewalls of the pillars. For details of the fabrication process (see [6]).

Process flow and a schematic cross-section of the device with surround gate are shown in Fig. 1a. A photo of the device is presented in Fig. 1b. Vertical transistors with two different values of gate oxide thickness (7 nm and 4 nm) were investigated.

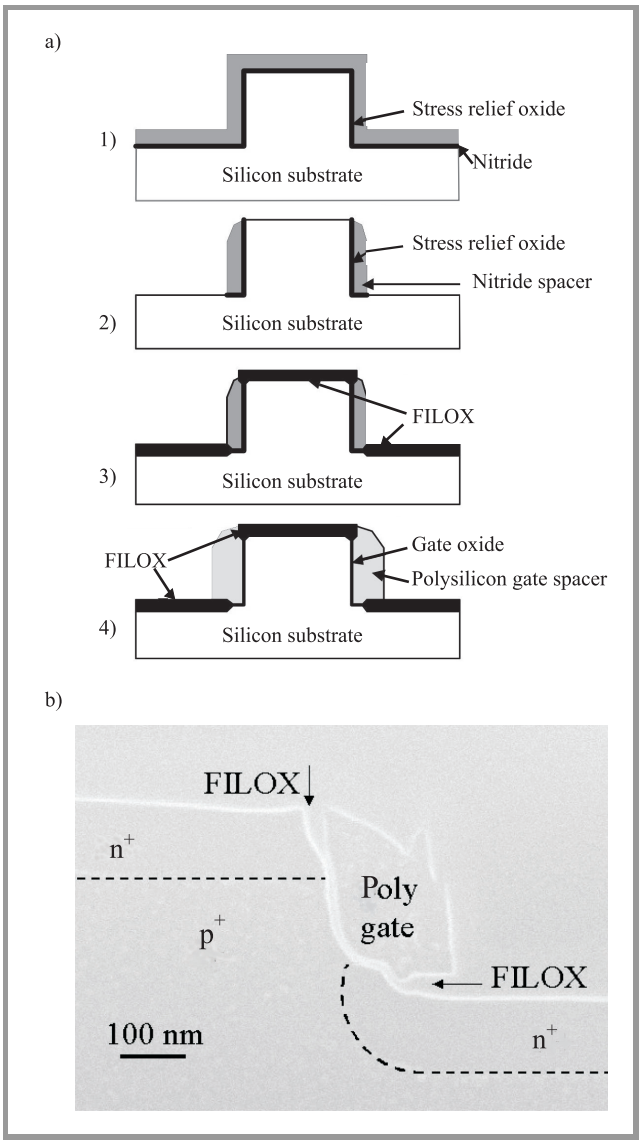

Fig. 1. Vertical MOSFET: (a) process flow and schematic cross-section of a FILOX; (b) photo of the device.

3. Results of electrical characterization

3.1. Analysis of I-V characteristics

A family of output characteristics measured on MOSFETs with the same channel dimensions but gate oxide thickness

of 7 nm and 4 nm is shown in Fig. 2. It may be seen that the saturation drain current of 4-nm VMOSFETs is more than an order of magnitude higher than that of devices with 7-nm oxide at the same gate voltage. While significant

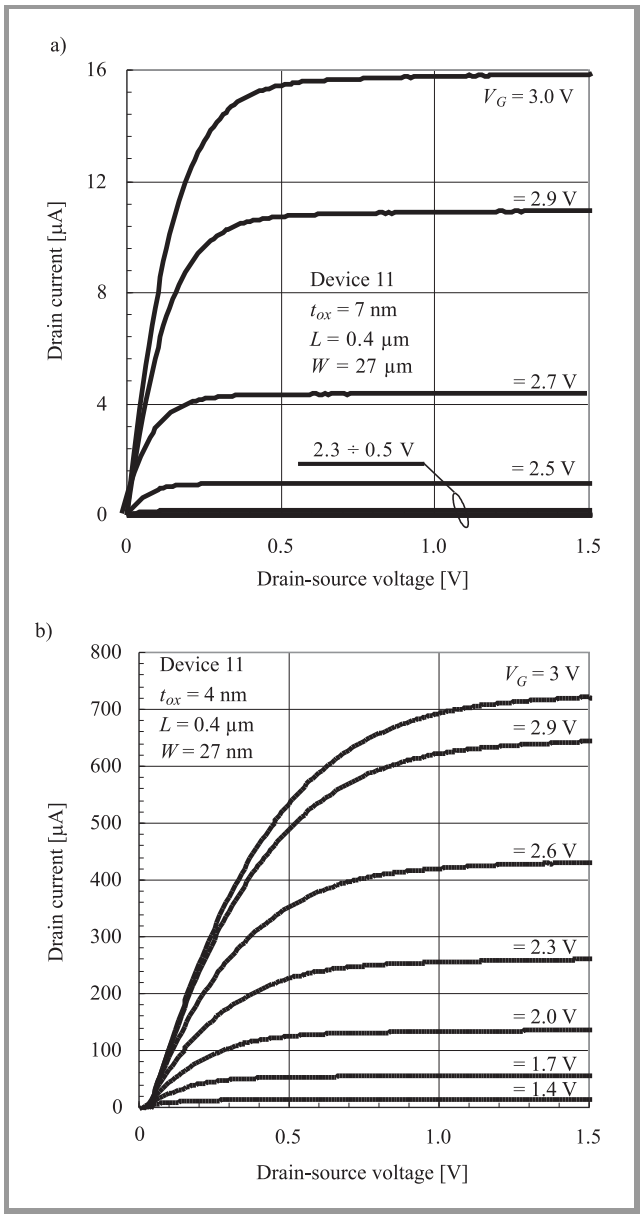

Fig. 2. Output characteristics of a FILOX vertical MOSFET: (a) $t_{ox} = 7$ nm; (b) $t_{ox} = 4$ nm.

enhancement of drain current is a positive consequence of the reduction of gate-oxide thickness, considerable increase of gate current is not. In Fig. 3 transfer characteristics of 7-nm and 4-nm VMOSFETs are shown, respectively, with gate current added for comparison. As seen, gate current is practically negligible in the case of 7-nm VMOSFETs, whereas for 4-nm devices it is comparable to the drain current in the above-threshold region and much higher in the subthreshold region (Fig. 3b). Thus, in terms of leakage current the quality of 4-nm gate oxide is much worse than that of the 7-nm oxide. Threshold voltage determined from

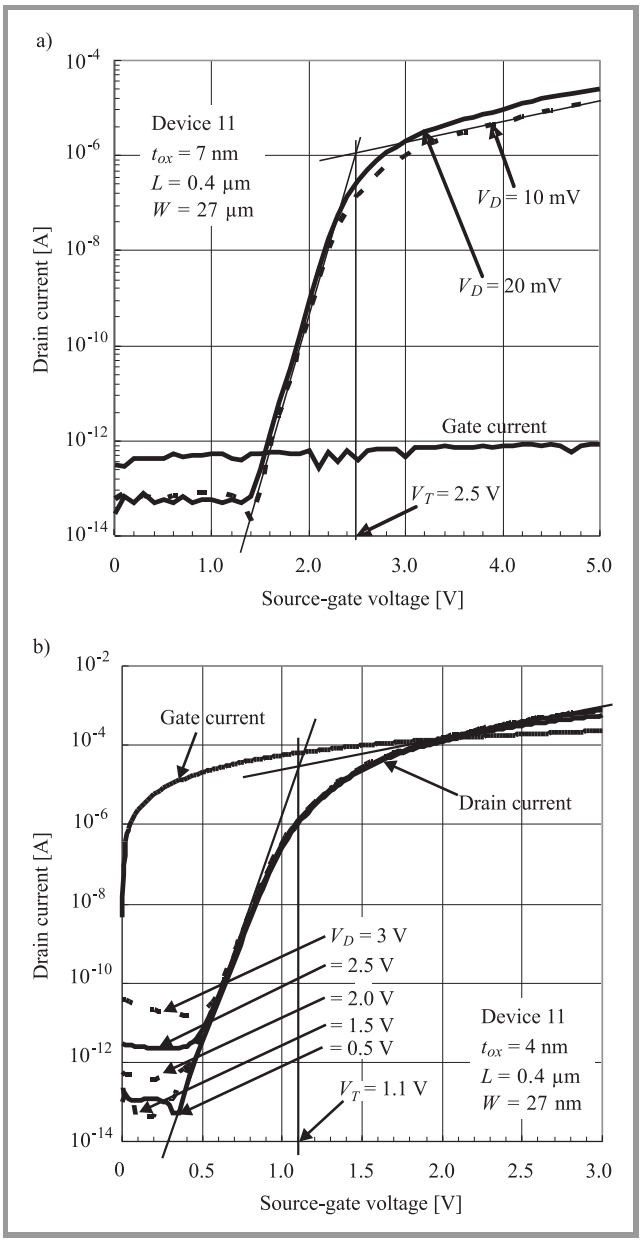

Fig. 3. Transfer characteristics: (a) of a 7-nm FILOX vertical MOSFET; (b) of a 4-nm FILOX vertical MOSFET.

the linear region and from transfer characteristics plotted in logarithmic-linear scale is approximately 2.4 V and 2.5 V for devices with 7-nm oxide and around 1.1 V for 4-nm VMOSFETs.

3.2. Charge-pumping measurements

Charge-pumping (CP), in its numerous forms, yields information on the density, energy levels and other properties of interface traps. Its main advantage is the fact that the device under test is a MOSFET, therefore no special test structures have to be fabricated. The method consists in switching the transistor between accumulation and strong inversion and measuring the DC substrate current that is caused by carrier recombination in interface traps.

The maximum charge-pumping current $I_{cp\max}$ is a measure of interface-trap density according to [7]:

$$I_{cp\max} = A_G q f N_{it}\,, \tag{1}$$

where: A_G – gate area, q – elementary charge, f – gate-signal frequency, N_{it} – total density of interface traps per unit area.

Equation (1) indicates that the maximum charge-pumping current is proportional to gate-signal frequency. Therefore the straight line obtained in Fig. 4 for devices with gate-oxide thickness of 7 nm indicates that the measured current is, indeed, related to charge-pumping. Similar results have been obtained in the case of 4-nm VMOSFETs.

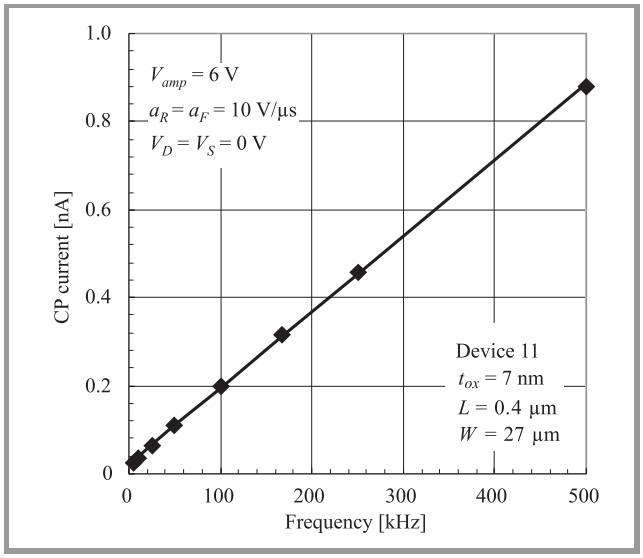

Fig. 4. Maximum charge-pumping current as a function of frequency ($t_{ox} = 7$ nm).

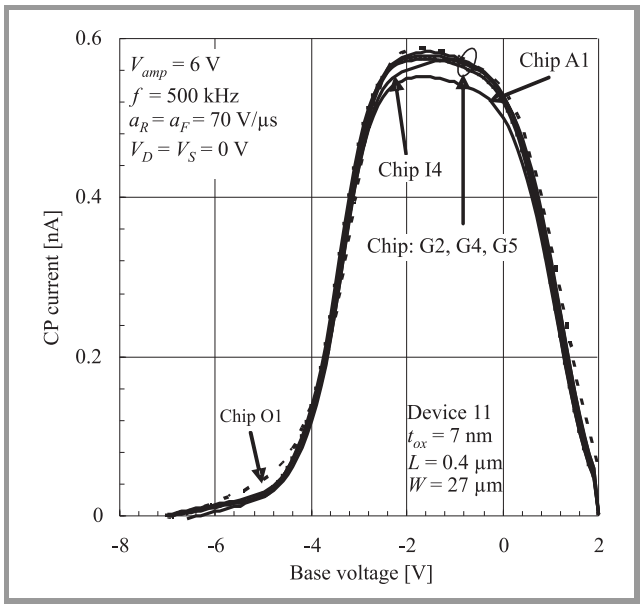

Fig. 5. Charge-pumping current as a function of base voltage for transistors located in several different chips ($t_{ox} = 7$ nm).

Charge-pumping current measured as a function of base voltage on transistors located in different chips (but all with the same gate dimensions) is shown in Fig. 5 for gate-oxide thickness of 7 nm. The results are comparable for all measured devices, which indicates good spatial uniformity of the fabrication process. In the case of 4-nm VMOSFETs the discrepancies between CP curves obtained from devices located at different chips are higher.

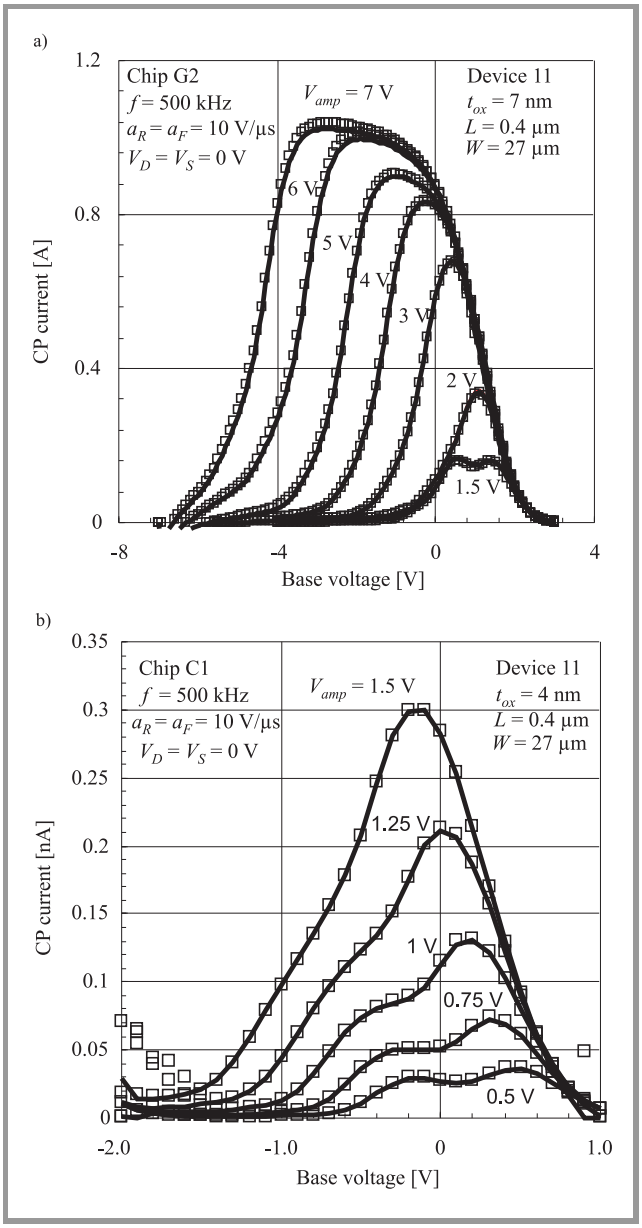

Fig. 6. Charge-pumping current as a function of base voltage with gate-signal amplitude as a parameter (a) $t_{ox} = 7$ nm; (b) $t_{ox} = 4$ nm. The results of repeated measurement are marked as squares.

The results of CP current measurements as a function of base voltage with gate-signal amplitude as a parameter are presented in Fig. 6 for gate-oxide thickness of 7 nm and 4 nm. In the first case the amplitude of the gate signal was successively increased from 1.5 V to 7 V and then

the whole measurement sequence was repeated once. The only difference in the case of $t_{ox} = 4$ nm was that the amplitude varied between 0.5 V and 1.5 V. The results of the first measurement sequence are represented by solid lines, while those of the second sequence by empty squares. Since the difference between the results obtained in either sequence is little, it may be concluded that measurements did not cause visible generation of interface traps. It should be noted that transistors with $t_{ox} = 7$ nm did not break down even at high electric fields in the gate oxide (> 10 MV/cm), while those with $t_{ox} = 4$ nm were damaged at lower electric fields. This indicates again that the quality of the 4-nm oxide is worse than that of the 7-nm one. This is probably the reason for our failure to obtain saturation of the maximum CP current with increasing amplitude for $t_{ox} = 4$ nm.

Comparison of the curves obtained at gate-voltage amplitude of 1.5 V and shown in Fig. 6 for devices with gate-oxide thickness of 7 nm and 4 nm, respectively, indicates that the maximum CP current is lower in the case of $t_{ox} = 7$ nm. The possible reasons for this effect are:

- lower density of interface traps for $t_{ox} = 7$ nm (better quality of the SiO_2-Si interface);
- smaller part of the energy gap is investigated in devices with 7-nm oxide (surface potential is a weaker function of gate voltage than in the case of 4-nm oxide);
- switching the devices with 7-nm oxides between accumulation and strong inversion is more difficult at such low amplitudes because their threshold voltage is higher than that of transistors with 4-nm oxide.

Comparison at higher amplitudes of gate voltage could not be made due to breakdown of the latter devices.

In the case of n-channel devices the location of the rising edge of the CP curve brings information on the value of the threshold voltage V_T (shifted in the direction of lower values by gate-voltage amplitude), whereas the location of the falling edge is a straight indication of the flat-band voltage V_{FB} [8]. The obtained values of the flatband and threshold voltage of a device with gate-oxide thickness of 7 nm are shown in Fig. 7 as a function of gate-signal amplitude. The value of flat-band voltage is approximately 1 V, and a weak dependence on gate-voltage amplitude is observed. If the amplitude is sufficiently high, the values of threshold voltage saturate at the level of 2.6 V, which is in very good agreement with values obtained from *I-V* curves. It should be noted, however, that saturation of the CP curve would be expected in this case at gate-voltage amplitudes of $2-3$ V, while in reality amplitudes of at least $5-6$ V are required. The explanation of this phenomenon is not known at this stage.

In the case of device with $t_{ox} = 4$ nm both flat-band and threshold voltage are strong functions of gate-voltage amplitude. This again is most probably due to the fact that no saturation of the maximum CP current could be obtained for those devices.

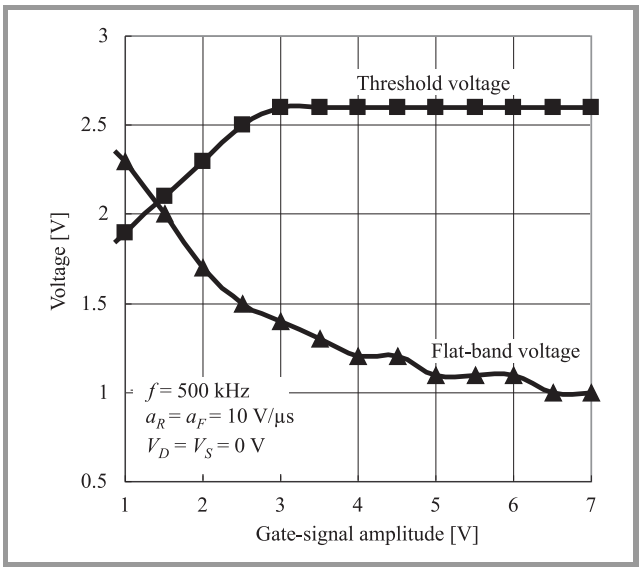

Fig. 7. Flat-band and threshold voltage as a function of gate-signal amplitude ($t_{ox} = 7$ nm).

As it had been mentioned before, the maximum charge-pumping current is used to determine the total density of interface traps N_{it}. Since it was not possible to obtain well-behaved CP curves in the case of $t_{ox} = 4$ nm, only devices with gate-oxide thickness of 7 nm are considered here. Interface trap density N_{it} measured for devices with different channel width varies between $1.3 \cdot 10^{11}$ cm^{-2} to 10^{12} cm^{-2} in a random manner. The reasons for these variations are not known at this stage.

4. Conclusions

Charge-pumping measurements were performed for the first time on FILOX vertical transistors. Well-behaved CP curves were obtained in the case devices with gate oxide thickness of 7 nm, whereas no saturation of CP current was obtained for VMOSFETs with $t_{ox} = 4$ nm, most probably due to high gate leakage current. For devices with $t_{ox} = 7$ nm values of flatband and threshold voltage, as well as total density of interface traps, were determined. Threshold-voltage values were in good agreement with those obtained from *I-V* curves. Further studies are required to explain why considerably higher gate-voltage amplitudes than indicated by V_T and V_{FB} values are needed for the CP current to saturate, and why interface trap density varies for devices with different channel length.

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Enrico Gili was born in Pinerolo, Italy, in 1977. He received the M.Sc. degree in physics engineering from the Institut National Polytechnique, Grenoble, France, in 2001, and the M.Sc. degree in materials engineering from the Politecnico di Torino, Turin, Italy, in 2002. In 2006 he received the Ph.D. degree from the University of Southampton, UK. His Ph.D. dissertation was on fabrication and characterization of CMOS-compatible vertical MOSFETs with reduced parasitics. In October 2006 he joined the Technology Development Department at Atmel North Tyneside in Newcastle Upon Tyne (UK) as a process integration engineer. There he is currently working on a 0.13 m CMOS technology for microcontrollers and flash memory applications.
e-mail: enrico_gili@hotmail.com
School of Electronics and Computer Science
University of Southampton
Highfield SO17 1BJ, UK

Peter Ashburn was born in Rotherham, England in 1950. He received the B.Sc. degree in electrical and electronic engineering in 1971, and the Ph.D. degree in 1974, both from the University of Leeds. His dissertation topic was an experimental and theoretical study of radiation damage in silicon p-n junctions. In 1974, he joined the technical staff of Philips Research Laboratories and worked initially on ion implanted integrated circuit bipolar transistors, and then on electron lithography for sub-micron integrated circuits. In 1978 he joined the academic staff of the Department of Electronics and Computer Science of the University of Southampton as a lecturer, and currently is the holder of a Personal Chair in Microelectronics. Since taking up a post at University of Southampton, Professor Ashburn has worked on polysilicon emitter bipolar transistors, high-speed bipolar and BiCMOS technologies, gate delay expressions for bipolar circuits and the effects of fluorine in bipolar transistors. His current research interests include SiGe HBTs on SOI, SiGeC devices and ultimate DMOS devices. He has authored and co-authored 170 papers in technical literature, given invited papers on polysilicon emitters and SiGe heterojunction bipolar transistors and has authored two books on bipolar transitors and SiGe heterojunction bipolar transistors.
e-mail: pa@ecs.soton.ac.uk
Department of Electronics and Computer Science
University of Southampton
Highfield SO17 1BJ, UK

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Lidia Łukasiak – for biography see this issue, p. 65.