Invited paper

Low frequency noise in advanced Si bulk and SOI MOSFETs

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Abstract—A review of recent results concerning the low frequency noise in modern CMOS devices is given. The approaches such as the carrier number and the Hooge mobility fluctuations used for the analysis of the noise sources are presented and illustrated through experimental data obtained on advanced CMOS SOI and Si bulk generations. Furthermore, the impact on the electrical noise of the shrinking of CMOS devices in the deep submicron range is also shown. The main physical characteristics of random telegraph signals (RTS) observed in small area MOS transistors are reviewed. Experimental results obtained on 0.35–0.12 μm CMOS technologies are used to predict the trends for the noise in future CMOS technologies, e.g., 0.1 μm and beyond. For SOI MOSFETS, the main types of layout will be considered, that is floating body, DTMOS, and body-contact. Particular attention will be paid to the floating body effect that induces a kink-related excess noise, which superimposes a Lorentzian spectrum on the flicker noise.

Keywords—CMOS, SOI, low frequency noise, fluctuations, kink-related excess noise, DTMOS.

1. Introduction

The low frequency (LF) noise and fluctuations in metal-oxide-semiconductor (MOS) devices have been the subject of intensive research during the past years. The LF noise is becoming a major concern for scaled-down devices, since the $1/f$ noise increases as the reciprocal of the device area [1–38]. Excessive low frequency noise and fluctuations could lead to serious limitation of the functionality of the analog and digital circuits. The $1/f$ noise is also of paramount importance in RF circuit applications where it gives rise to phase noise in oscillators or multiplexers [33]. The development of submicron CMOS technologies has led to the onset of new type of noise, i.e., random telegraph signals (RTS's) [8–10, 15], yielding large current fluctuations, which can jeopardize the circuit functionality. In addition, thanks to their structure, the SOI technologies present several intrinsic properties for analog and RF applications. For instance, as it is well established now, these interesting devices allow the reduction of the power consumption at a given operating frequency.

Moreover, the high insulating properties of SOI substrates, in particular with the use of high resistivity material, leads to high performance mixed-signal circuits [34–36]. However, in order to use this kind of devices in such applications, low frequency noise, which can directly impact RF or analog integrated circuits, needs to be thoroughly evaluated. Following the specifications of the ITRS roadmap, the $1/f$ noise amplitude is predicted to decrease in modern technologies. But, the maximum signal is also lowered with decreasing operation voltage leading to a deterioration of the signal to noise ratio. Therefore, accurate characterization of the noise behavior has to be established.

The aim of this paper is first to present recent issues about the low frequency and RTS noise in CMOS devices. The approaches such as the carrier number and the Hooge mobility fluctuations used for the analysis of noise sources will be presented and illustrated through experimental data obtained on advanced CMOS SOI and Si bulk generations. The application of low frequency noise measurements as a characterization tool for large area MOS devices will also be discussed. Besides, the main physical parameters characterizing the RTS's in small area MOS transistors will be briefly reviewed. Experimental data obtained on 0.35–0.12 μm CMOS technologies will be used to predict the trends for the noise in the future CMOS technologies, e.g., 0.1 μm and beyond.

2. Low frequency noise in large area devices

2.1. Carrier number fluctuations and correlated mobility fluctuations

In the classical carrier number fluctuation approach, the fluctuations in the drain current stem from the fluctuations of the inversion charge nearby the Si-SiO_2 interface, arising from the variations of the interfacial oxide charge after dynamic trapping/detrapping of free carriers into slow oxide border traps. These interface charge fluctuations δQ_{it} can be equivalently equated to a flat band voltage variation $\delta V_{fb} = -\delta Q_{it}/(WLC_{ox})$. Moreover, in a more detailed analysis one should also take into account the supplementary mobility change $\delta\mu_{eff}$ due to the modulation of the scattering rate induced by the interface charge fluctuations. The drain current fluctuations therefore read [16, 22]:

$$\delta I_d = -g_m \delta V_{fb} - \alpha I_d \mu_{eff} \delta Q_{it}, \qquad (1)$$

where g_m is the transconductance, μ_{eff} is the effective mobility, α is the Coulomb scattering coefficient ($\approx 10^4$ Vs/C for electrons and 10^5 Vs/C for holes).

This leads to a normalized drain current and input gate voltage noise $S_{Vg} = S_{I_d}/g_m^2$ for strong inversion:

$$S_{I_d}/I_d^2 = (1+\alpha\,\mu_{eff}\,C_{ox}\,I_d/g_m)^2\left(\frac{g_m}{I_d}\right)^2 S_{V_{fb}} \qquad (2a)$$

and

$$S_{V_g} = S_{V_{fb}}\left[1+\alpha\,\mu_0\,C_{ox}(V_g-V_t)\right]^2, \qquad (2b)$$

where μ_0 is the low field mobility, C_{ox} is the gate oxide capacitance, V_t is the threshold voltage, $S_{V_{fb}} = S_{Q_{it}}/(WLC_{ox}^2)$ with $S_{Q_{it}}$ (C^2/Hz/cm^2) being the interface charge spectral density per unit area, W the device width and L the device length.

The spectral density of the oxide interface charge depends essentially on the physical trapping mechanisms into the oxide. For a tunneling process, the trapping probability decreases exponentially with oxide depth x, so that the flat band voltage spectral density takes the form [2, 3]:

$$S_{V_{fb}} = \frac{q^2 \mathrm{k}T\,\lambda\,N_t}{WLC_{ox}^2 f^\gamma}, \qquad (3)$$

where f is the frequency, γ is a characteristic exponent close to 1, λ is the tunnel attenuation distance (≈ 0.1 nm), kT is the thermal energy and N_t is the volumetric oxide trap density (eV^{-1} cm^{-3}).

For a thermally activated trapping process [7], the trapping probability decreases exponentially with the cross section activation energy E_a, so that the flat band voltage spectral density reads [11]:

$$S_{V_{fb}} = \frac{q^2 \mathrm{k}^2 T^2 N_{it}}{WLC_{ox}^2 f^\gamma \Delta E_a}, \qquad (4)$$

where ΔE_a is the amplitude of the activation energy dispersion and N_{it} is the oxide trap surface state density (eV^{-1} cm^{-2}). In both trapping mechanisms, the $1/f$ nature of the spectrum stems from the uniform distribution in log scale of the involved time constants [5].

It should be mentioned that Eqs. (2a,b) also applies to the nonlinear regime of MOSFET operation [23]. Indeed, the drain voltage dependence of S_{I_d}/I_d^2 is naturally accounted for by that of the transconductance to drain current ratio squared $(g_m/I_d)^2$. This can been checked experimentally by comparing the respective variations of S_{I_d}/I_d^2 and $(g_m/I_d)^2$ with drain voltage V_d.

2.2. Hooge mobility fluctuations

In the Hooge model [4], the drain current noise results from the fluctuations of the carrier mobility through the variations in the scattering cross section entering the collision probability likely due to phonon number fluctuations [6]. This leads to a flicker noise with the amplitude inversely proportional to the total number of carriers in the device. The normalized drain current noise and input gate voltage noise in ohmic operation can then be written in the form [17, 22]:

$$\frac{S_{I_d}}{I_d^2} = \frac{q\alpha_h}{WLQ_i f} \qquad (5)$$

and

$$S_{V_g} = \frac{q\alpha_h}{WLfC_{ox}}(V_g-V_t)\left[1+\theta(V_g-V_t)\right]^2, \qquad (6)$$

where Q_i is the inversion charge, α_h is the Hooge parameter ($\approx 10^{-4}-10^{-6}$), and θ is the mobility attenuation coefficient.

Similarly, in the case of the nonlinear region of MOSFET operation, the inversion layer is no longer uniform along the channel and the normalized drain current can be expressed as [17]:

$$\frac{S_{I_d}}{I_d^2} = \frac{q\alpha_h}{fWL^2}\int_0^L \frac{\mathrm{d}y}{Q_i(y)} = \frac{q\alpha_h}{fWL^2}\int_0^{V_d}\frac{W\mu_{eff}}{I_d}\mathrm{d}\phi_c$$
$$= \frac{q\alpha_h < \mu_{eff} > V_d}{fL^2 I_d}, \qquad (7)$$

where $< \mu_{eff} >$ is the average mobility along the channel. Indeed, in the ohmic region, Eq. (7) reduces to Eq. (5). Therefore, in all the cases (ohmic and nonlinear regions), the normalized drain current noise due to Hooge mobility fluctuations varies as the reciprocal drain current.

2.3. Impact of series resistance

The impact of series resistance on the low frequency noise can simply be obtained by adding to the channel current noise the contribution of the excess noise arising from the access region. For instance, in the linear region, the total drain current noise becomes [26]:

$$\frac{S_{I_d}}{I_d^2} = \left(\frac{S_{I_d}}{I_d^2}\right)_{channel} + \left(\frac{I_d}{V_d}\right)^2 S_{R_{sd}}, \qquad (8)$$

where $S_{R_{sd}}$ is the spectral density of source-drain series resistance.

For the carrier number fluctuations, one gets:

$$\frac{S_{I_d}}{I_d^2} = \left(1+\alpha\,\mu_{eff}\,C_{ox}\,I_d/g_m\right)^2\left(\frac{g_m}{I_d}\right)^2 S_{V_{fb}} + \left(\frac{I_d}{V_d}\right)^2 S_{R_{sd}}. \qquad (9)$$

2.4. Diagnosis of the low frequency noise sources

2.4.1. Measurements in the linear regime

A generic procedure for the diagnosis of the excess LF noise sources in a MOS transistor can be drawn from the above analyses [22]. The normalized drain current noise versus drain current characteristics in a log-log scale can first be inspected for comparison with Eqs. (2) and (7). If the normalized drain current spectral density varies with the drain current as the transconductance to drain current

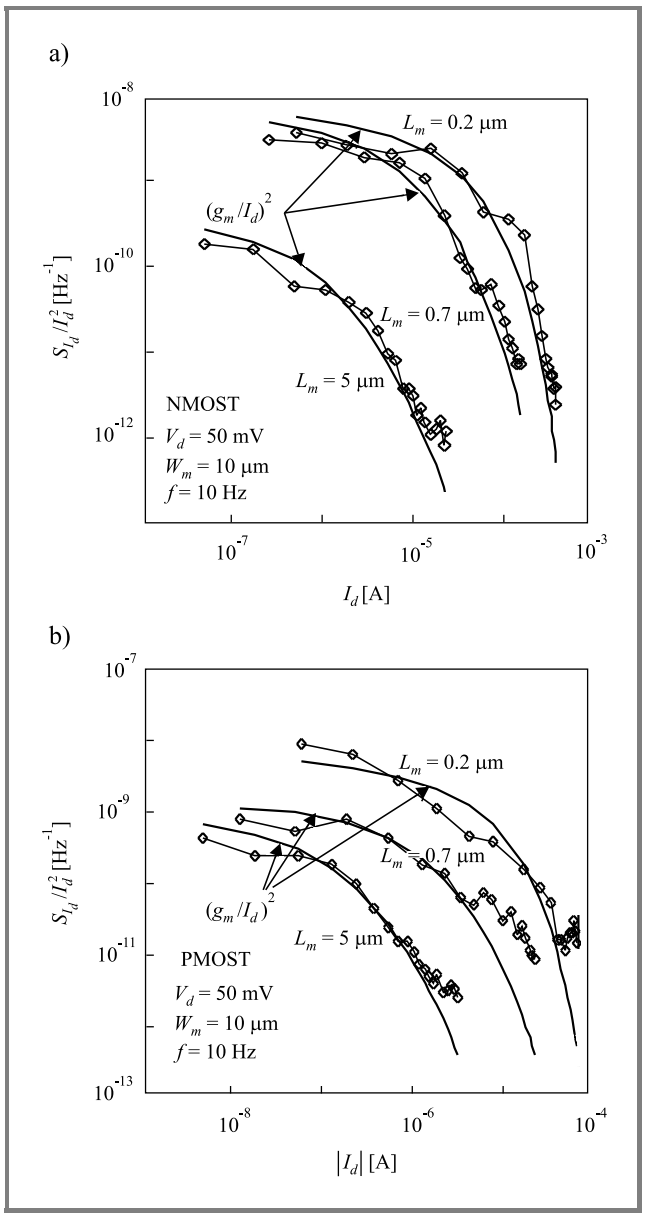

Fig. 1. Variation of the normalized drain-current noise versus drain current for (a) n-channel and (b) p-channel 0.18 μm CMOS devices.

ratio squared, one can likely conclude that carrier number fluctuations dominate. Furthermore, if the associated input gate voltage noise shows a parabolic dependence on the gate voltage at strong inversion, the correlated mobility fluctuations might be involved ($\alpha \gg 1$ in Eq. (2)).

Hooge mobility fluctuations can also be diagnosed using the $S_{I_d}/I_d^2(I_d)$ plot in a log-log scale. If the normalized current noise varies as the reciprocal of the drain current from weak to strong inversion, it can be concluded that Hooge mobility fluctuations dominate.

Moreover, if the normalized drain current noise increases at high drain current, this is indicative of an enhanced LF noise contribution of the access resistance (see Eq. (8)).

Figure 1 gives typical examples of $S_{I_d}/I_d^2(I_d)$ characteristics for 0.18 μm CMOS Si bulk devices. They illustrate

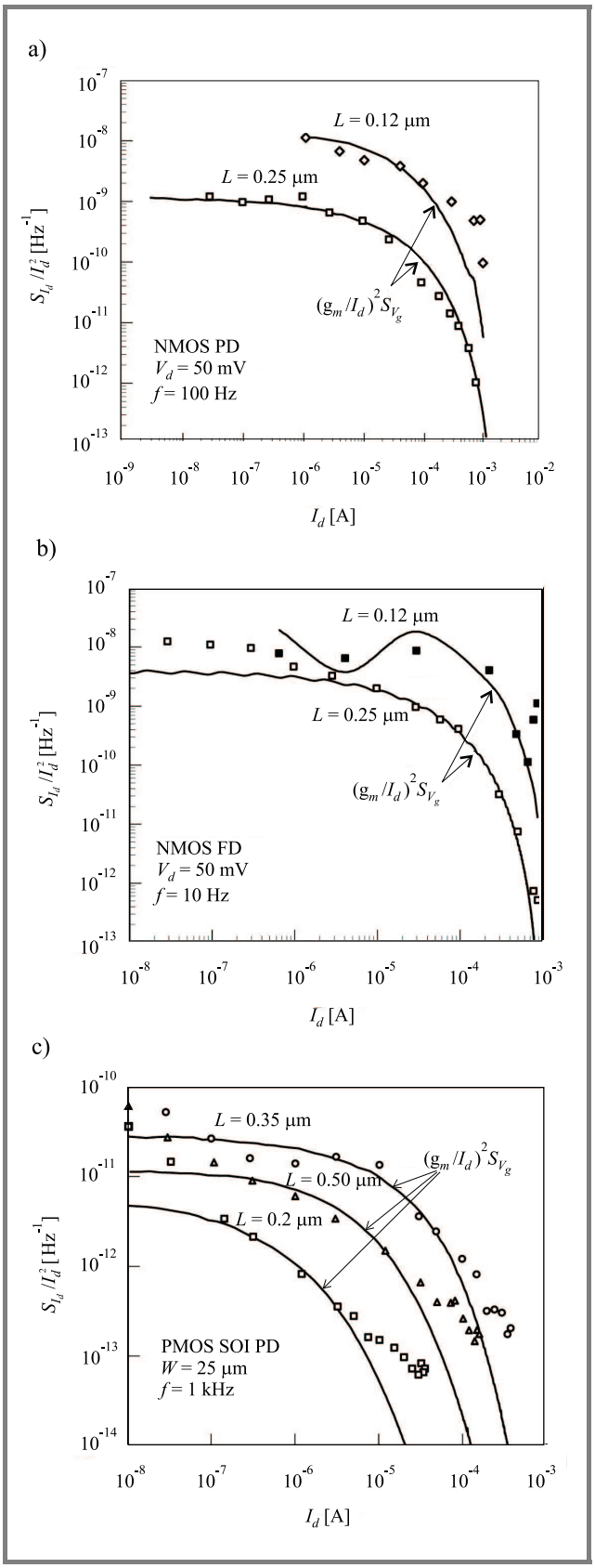

Fig. 2. Normalized drain-current power spectral density S_{I_d}/I_d^2 at $V_d = 50$ mV as a function of drain current at different channel lengths for (a) NMOS FB partially-depleted; (b) NMOS fully depleted and (c) PMOS FB partially-depleted SOI devices. Full lines: $S_{V_g} * (g_m/I_d)^2$.

a very good correlation between the normalized drain current noise and the transconductance to drain current ratio squared from weak to strong inversion. Therefore, in this case, it can be inferred that carrier number fluctuations are the main LF noise source. This behavior is representative of modern n- and p-channel devices ($L < 0.35$ μm), where both device types operate in surface mode due to the dual poly gate material. In contrast, for 0.35 μm technology, it was found that p-type transistors obey Hooge mobility model due to the buried architecture of the channel with n^+ Si poly gate [29]. Therefore, in general, for surface mode operated MOSFETs, the LF noise is found to result from carrier number fluctuations whereas, for volume mode operated devices, Hooge mobility fluctuations should contribute more.

Figure 2 shows the normalized drain current power spectral density S_{I_d}/I_d^2 in the ohmic regime ($V_d = 50$ mV), plotted as a function of the drain current for n-channel partially-depleted (PD) SOI MOSFETs (Fig. 2a) and for n-channel fully-depleted (FD) SOI MOSFETs (Fig. 2b) for two channel lengths: $L = 0.25$ and 0.12 μm. In this plot, the straight line represents the front gate power spectral density S_{V_g} multiplied by the ratio $(g_m/I_d)^2$, where g_m stands for the gate transconductance. A good correlation is obtained between these two quantities, confirming the results predicted by the McWhorter model, which associates the $1/f$ noise with the carrier number fluctuations. Moreover, some difference in strong inversion can be observed (p-channel, Fig. 2c), which is attributed to the correlated mobility fluctuations.

2.4.2. Measurements in the saturation mode

Low frequency noise characterization of SOI devices also needs to be carried out in the saturation mode, where bias conditions give birth to the kink-related excess noise observed in SOI devices. The drain current spectral density S_{I_d}, normalized to the width, is plotted (Fig. 3) versus the applied drain voltage V_d for 0.12 μm floating body (FB) PD SOI and for $L = 0.25$ μm with FB-PD and body-contacted (BC) technologies.

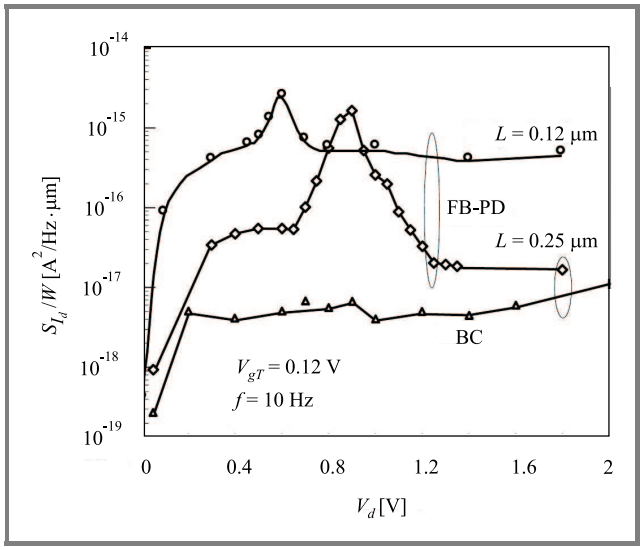

Fig. 3. Drain-current power spectral density, normalized to the width W as a function of drain voltage, at $f = 10$ Hz for FB-PD devices with two channel lengths ($L = 0.25$ and 0.12 μm) and for BC devices with $L = 0.25$ μm.

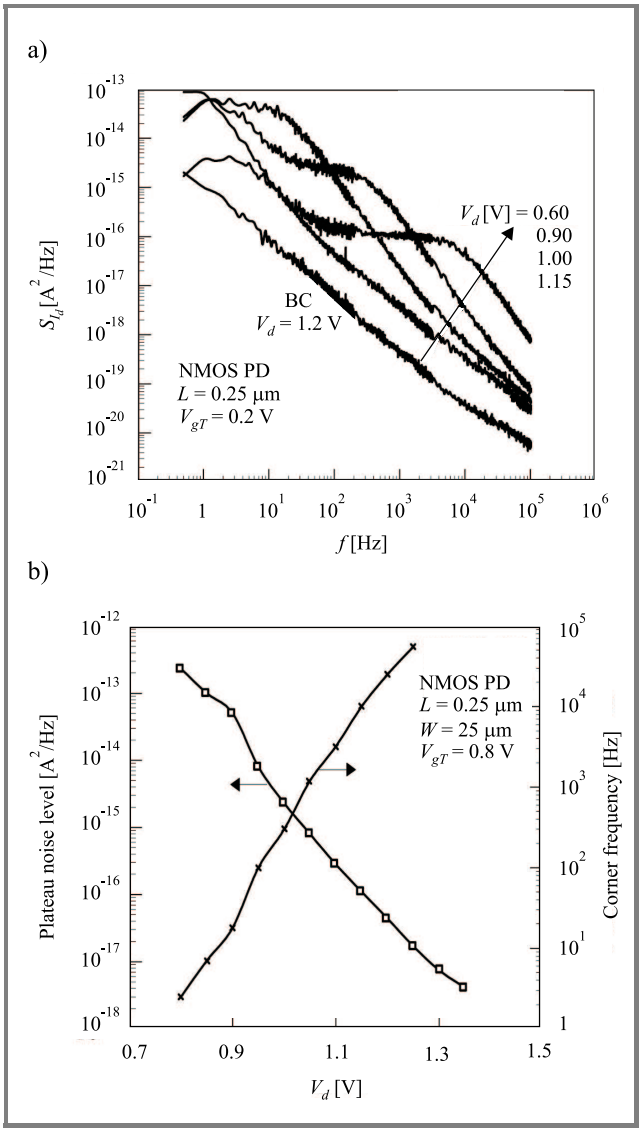

Fig. 4. (a) Drain current power spectral density versus frequency for 0.25 μm FB and BC partially-depleted devices, at different drain voltages and (b) drain bias dependence of the plateau noise level and the corner frequency for 0.25 μm PD device with a floating body.

A substantial kink effect is clearly observed in the case of FB-PD devices, and a low frequency excess noise occurs for a drain bias corresponding to the kink effect in static measurements. This noise peak shifts with the frequency, towards higher V_d. However, the kink effect disappears when the SOI film is connected to the ground. The floating body effect induces a kink-related excess noise, which superimposes a Lorentzian spectrum on the flicker noise,

characterized by a corner frequency, f_c, and a plateau noise level, S_{I_d} (0).

Several mechanisms have been proposed to explain this excess noise, such as trap-assisted generation-recombination noise [37] or shot noise amplified by floating body effect [38]. This behavior is clearly shown in Fig. 4a for a 0.25 μm PD device at different values of V_d. It is important to note that the corner frequency and the plateau noise level of the Lorentzian spectrum depend both on the drain bias (Fig. 4b).

For PD devices, f_c increases and the noise level of the plateau of the Lorentzian spectrum decreases continuously as the drain bias is enhanced. This is due to a close correlation between the substrate current, I_B, and the kink phenomenon. The noise plateau level is reversely proportional to I_B and the corner frequency is proportional to the substrate current. Moreover, a relevant point here is the difference between the kink noise overshoot for 0.25 and 0.12 μm PD technologies. The magnitude for $L = 0.12$ μm is only one decade high, contrary to the 0.25 μm SOI CMOS technology for which two orders of magnitude were obtained.

3. Random telegraph signals in small area MOS devices

The observation of RTS's in small area MOS transistors is commonly attributed to individual carrier trapping at the silicon-oxide interface [8–10, 14, 15, 18]. The drain current RTS fluctuations can be interpreted as conductance modulation originating from carrier number and/or subsequent mobility fluctuations.

Figure 5 displays a typical time domain waveform of the drain current illustrating the three main RTS parameters. As the transition times from low to high level (and *vice versa*) are Poisson distributed random variables, the RTS parameters have to be measured using statistical analysis [12, 21]. The histogram of the drain current amplitudes, which is no longer Gaussian, provides the average drain current RTS amplitude ΔI_d. The average values of the high and low level time constants represent, for an acceptor like trap, the capture time τ_c and the emission time τ_e, respectively.

The drain current spectrum of a random telegraph signal has a Lorentzian shape [1]:

$$S_{I_d} = 4A\Delta I_d^2 \frac{\tau}{1+\omega^2\tau^2}, \tag{10}$$

where $\tau = (1/\tau_c + 1/\tau_e)^{-1}$ is the effective time constant, $A = \tau/(\tau_c+\tau_e) = f_t(1-f_t)$ is the space mark ratio $\omega = 2\pi f$ is the angular frequency and f_t is the trap occupancy factor, $f_t = 1/\left\{1+\exp\left[(E_t-E_f)/\mathrm{k}T\right]\right\}$ with E_t being the trap energy and E_f the Fermi level position.

The drain current RTS amplitude can be calculated assuming that the trapping of an elementary charge q in the channel changes the local conductivity [12, 23–25]. It is easy to show that, to a first order approximation, the relative drain current RTS amplitude is given by [25, 27]:

$$\frac{\Delta I_d}{I_d} = \frac{g_m}{I_d}\frac{q}{WLC_{ox}}\left(1-\frac{x_t}{t_{ox}}\right), \tag{11}$$

where x_t is the distance of the trap to the Si-SiO_2 interface and t_{ox} is the gate oxide thickness.

This expression, which applies to the ohmic and nonlinear regions, shows that the RTS amplitude should vary with drain and gate voltages as the transconductance to drain current ratio. It is also worth noticing that it represents the amplitude version of Eq. (2a) for $\alpha = 0$.

Figure 6 displays typical variations of the relative drain current RTS amplitude with gate and drain voltages as obtained on NMOSFETs, which illustrate the validity of Eq. (11). This relation is rather well appropriate for the strong inversion region. However, it does not explain quantitatively the huge sample-to-sample variations of the RTS amplitude observed in weak inversion [27]. It has been proposed that a proportionality factor depending on the trap area could be introduced in Eq. (11) in order to extend its range of application [27].

The capture and emission times are in general governed by the Shockley-Read-Hall statistics [12]:

$$\tau_c = \frac{1}{\sigma n_s v_{\mathrm{th}}} \quad \text{and} \quad \tau_e = \frac{1}{\sigma n_1 v_{\mathrm{th}}}, \tag{12}$$

where v_{th} is the thermal velocity, n_s is the surface carrier concentration, n_1 is the surface carrier concentration when

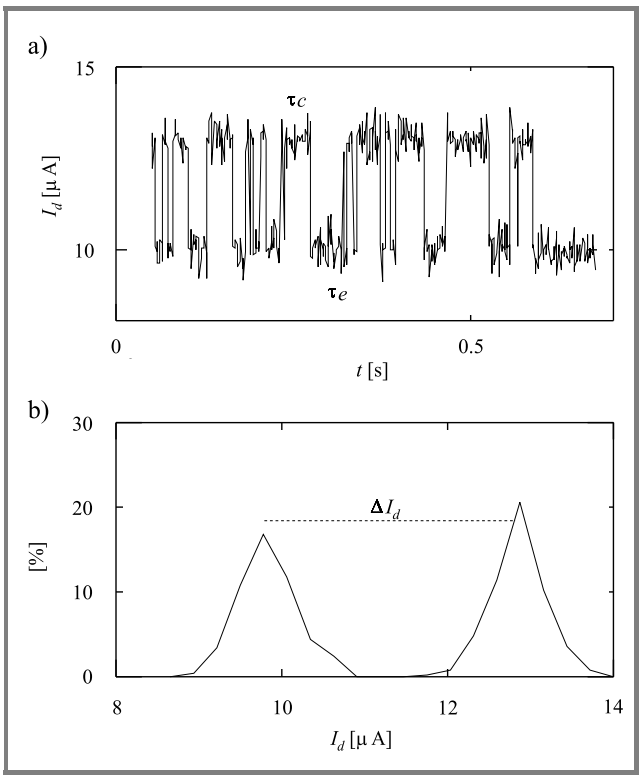

Fig. 5. Typical time-domain plot of the drain current for RTS noise (a) and corresponding amplitude histogram (b).

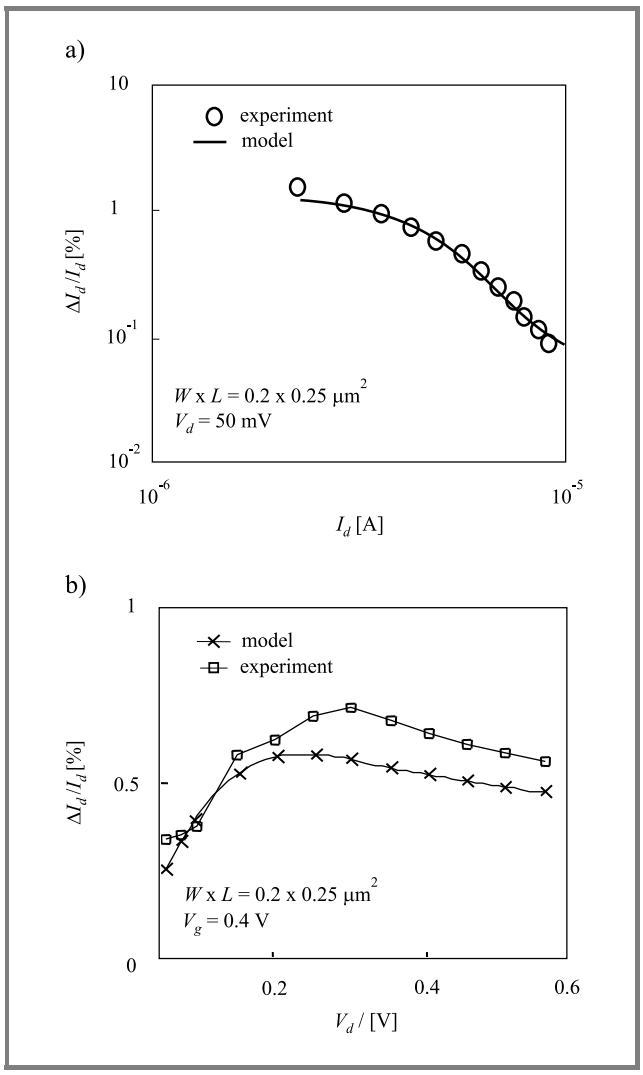

Fig. 6. Typical variations of the capture and emission times with gate (a) and drain (b) voltages. The lines show the results from the SRH model with appropriate parameters.

the Fermi level E_f equals the trap energy E_t, and σ is the trap cross section including tunneling effect and activated process [12, 20].

4. Low frequency noise in DTMOS

In this section, low frequency noise (LFN) in n- and p-channel dynamic-threshold MOSFET's on unibond substrate (SOI) is investigated. Two different types of transistors have been used: with and without current limiter. The LFN in DTMOS is analyzed in ohmic and saturation regimes. The impact of the use of a current limiter (clamping transistor) is shown. An explanation based on floating body effect inducing excess noise is proposed.

Due to a high-leakage current when the body is strongly forward biased, a small size current limiter is added between the gate and body in a DTMOS structure. Figure 7 shows the two device types. Note that the clamping transistor complicates the design but prevents the body potential (V_{BS}) from exceeding 0.65 V and allows the operation at 1 V gate bias without high gate current. Figure 8 shows drain and gate static currents versus gate voltage for 0.25 μm N-DTMOS with and without a clamping transistor. We can note the gate current limitation thanks to the clamping transistor.

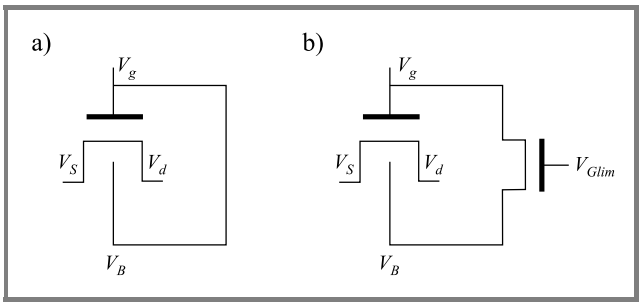

Fig. 7. Schematics of the two transistor types. DTMOS (a) without a clamping transistor and (b) with a clamping transistor.

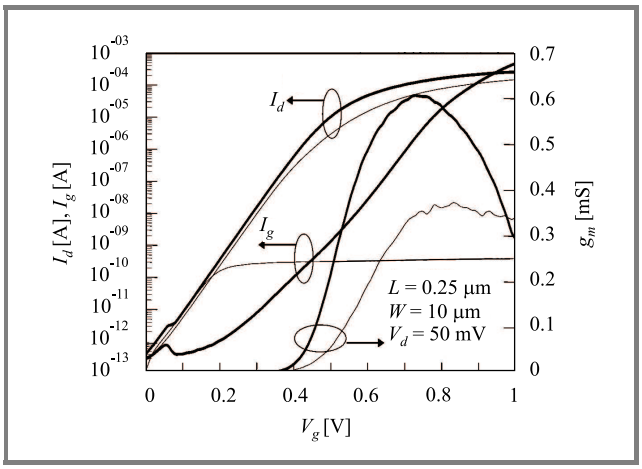

Fig. 8. Drain and gate currents, and gate transconductance versus gate voltage at $V_d = 50$ mV for 0.25 μm DTMOS with and without current limiter.

In Fig. 9a the drain current power spectral density (S_{I_d}) in the ohmic region ($V_d = 50$ mV) is plotted as a function of frequency at various levels of drain current, for 0.25 μm n-channel DTMOS without a clamping transistor. $1/f$ spectra are obtained for all drain-current levels. Similar results have also been obtained in PMOS transistors.

If a clamping transistor is used with a DTMOS, however, $S_{I_d}(f)$ shows Lorentzian spectra (Fig. 9b). These spectra are strongly dependent on the gate voltage of the current limiter (V_{Glim}). The plateau level of the Lorentzian spectrum decreases and the corner frequency increases when V_{Glim} increases (Fig. 9b). This behavior is quite similar to the noise overshoot (at high V_d) induced by the kink effect in partially depleted SOI, which is due to the impact ionization mechanism. In our case, V_d is too weak to induce the impact-ionization current, however, the clamping transistor current flows through the body inducing an excess noise

following Lorentzian spectra. When V_{Glim} is between zero and 1 V, the body potential is fixed by the clamping transistor current and, consequently, this current increases the body potential inducing a direct biasing of the source-body junction and a kink-excess-like noise is obtained, even at low drain voltage. At $V_{Glim} = 1$ V, the clamping transistor is on, therefore, the body is directly connected to the gate. In this case, a quasi $1/f$ behavior is obtained (Fig. 9b).

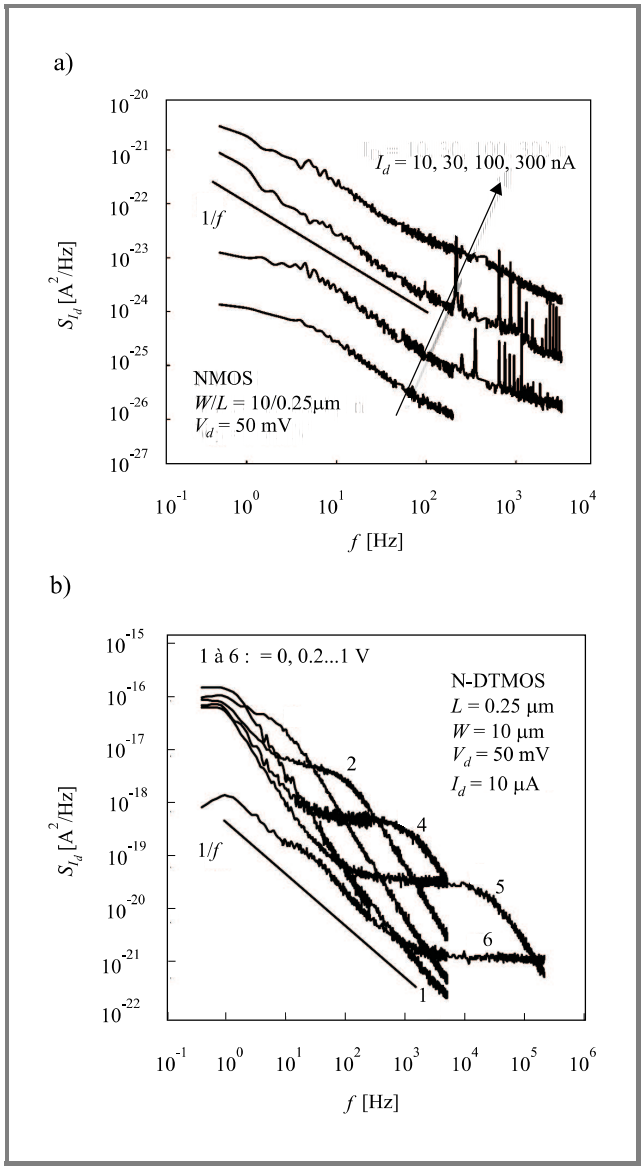

Fig. 9. Drain current power spectral density versus frequency in ohmic region for 0.25 μm n-channel DTMOS without (a) and with (b) current limiter.

Figure 10 shows the normalized drain current noise versus drain current for N- and PMOS transistors in BC and DTMOS modes. A good correlation with $(g_m/I_d)^2$ for n- and p-channel is obtained. It confirms, therefore, that the noise source in these devices is due to the carrier number fluctuations. Moreover, for all devices, the same drain-current noise is obtained, at least in weak inversion.

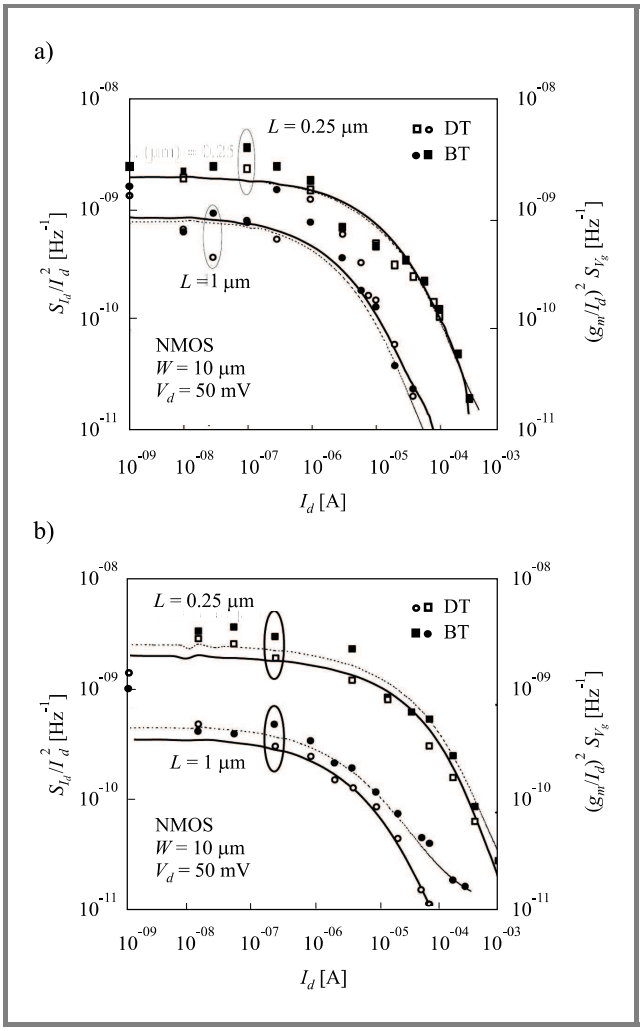

Fig. 10. Normalized drain current power spectral density $S_{I_d}/{I_d}^2$ at $V_d = 50$ mV and two channel lengths for (a) NMOS and (b) PMOS SOI devices. Full symbols for body-contacted and open symbols for DTMOS.

Some difference in strong inversion can be observed (1 μm p-channel BTMOSFET), which is attributed to the correlated mobility fluctuations.

5. Gate induced floating body effects

Low frequency excess noise associated to gate induced floating body effect is reported in partially depleted SOI MOSFETs with ultra-thin gate oxide. This is investigated with respect to floating body devices biased in linear regime. Due to a body charging from the gate, a Lorentzian-like noise component is superimposed on the conventional $1/f$ noise spectrum. This excess noise exhibits the same behaviour as the kink-related excess noise previously observed in partially depleted devices in the saturation regime.
Indeed, scaling metal-oxide-semiconductor devices to very-deep submicron dimensions has resulted in an aggressive shrinking of the gate oxide thickness. In this ultra-thin

gate oxide range, direct tunneling from the gate clearly appears, and increases exponentially with decreasing oxide thickness. Taking into consideration the case of floating body PD SOI MOSFETs with a 2 nm front gate oxide, the gate-to-body tunneling component becomes large enough to charge the body of the devices, resulting in gate induced floating body effects (GIFBE) observed even in the linear regime.

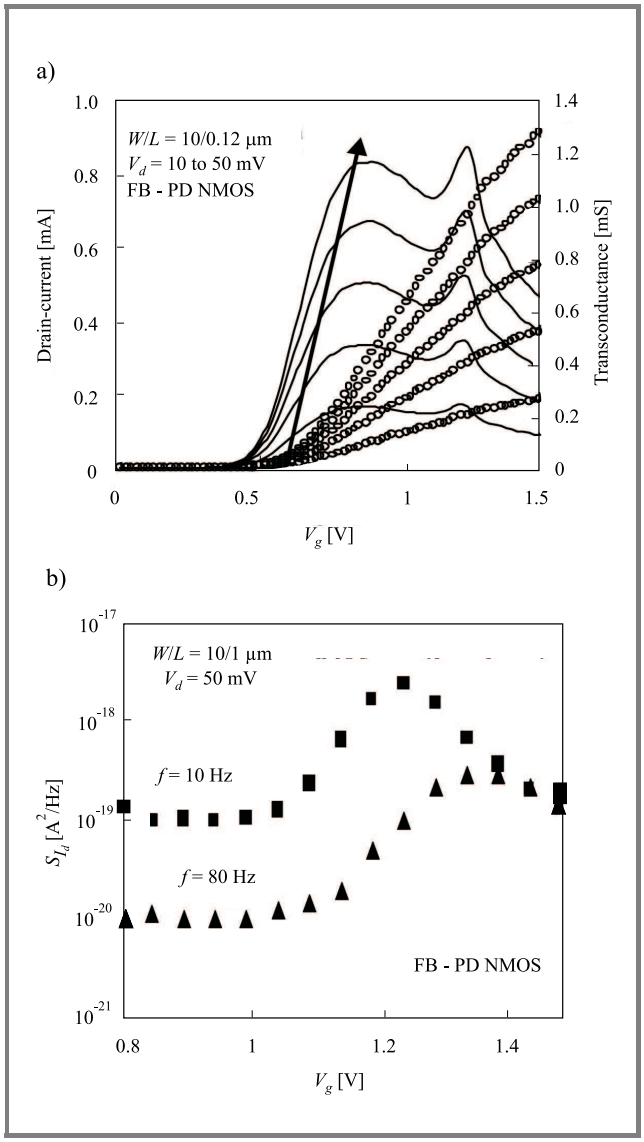

Fig. 11. (a) I_d and g_m transfer characteristics of a $W/L = 10/0.12$ μm PD NMOSFET at low drain voltage ($V_d = 10$ to 50 mV), and (b) drain current power spectral density of a $W/L = 10/1$ μm PD NMOSFET with $V_d = 50$ mV. The two different frequencies are 10 Hz and 80 Hz.

Figure 11a illustrates the drain current and transconductance measured in the linear regime for $V_d = 10$ up to 50 mV for a $W/L = 10/0.12$ μm PD NMOSFET. A sudden increase of the drain current is noticeable close to $V_g = 1.1 - 1.2$ V regardless of the drain bias. This results in an unforeseen second hump in the transconductance characteristics, the value of which exceeds that of the normal peak. The same feature is observed in PMOSFETs. Then, we considered the drain current power spectral density versus the applied front-gate bias for two different frequencies ($f = 10$ and 80 Hz). The results are plotted in Fig. 11b for a $W/L = 10/1$ μm FB-PD SOI MOSFET biased with a drain voltage $V_d = 50$ mV. The level of noise overshoot attributed to the GIFBE is almost two decades for this device. The shift of the noise peak towards higher gate biases with increasing measurement frequency is clearly shown in Fig. 10b.

6. Summary and conclusion

A brief review of recent results concerning the low frequency noise in modern CMOS devices has been given. The approaches such as the carrier number and the Hooge mobility fluctuations used for the analysis of the noise sources have be presented and illustrated through experimental data taken on advanced CMOS generations. The use of low frequency noise measurements as a characterization tool for large area MOS devices has also be discussed. Moreover, the main physical parameters characterizing the RTS's in small-area MOS transistors have been reviewed. An overview of the low frequency noise in both partially and fully depleted SOI CMOS technologies has been given. An enhancement of the overall noise level is noticeable when reducing the channel length. As regards partially depleted devices, the kink-related excess noise magnitude is reduced with the channel length, especially in terms of Lorentzian-like spectra and corner frequency evolution. The LFN in DTMOS was studied in ohmic and saturation regimes and the impact of the use of a current limiter was thoroughly analyzed. Finally, the impact of the oxide thickness thinning on the noise was also shown.

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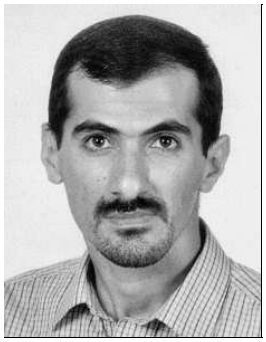

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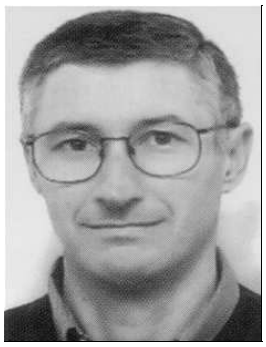

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