Invited paper

An accurate prediction of high-frequency circuit behaviour

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Abstract—An accurate way to predict the behaviour of an RF analogue circuit is presented. A lot of effort is required to eliminate the inaccuracies that may generate the deviation between simulation and measurement. Efficient use of computer-aided design and incorporation of as many physical effects as possible overcomes this problem. Improvement of transistor modelling is essential, but there are many other unsolved problems affecting the accuracy of RF analogue circuit modelling. In this paper, the way of selection of accurate transistor model and the extraction of parasitic elements from the physical layout, as well as implementation to the circuit simulation will be presented using two CMOS circuit examples: an amplifier and a voltage controlled oscillator (VCO). New simulation technique, electro-magnetic (EM)-co-simulation is introduced.

Keywords—electro-magnetic simulation, SPICE, circuit test structure, RF CMOS, EKV2.6-MOS model, spiral inductor, CMOS VCO.

1. Introduction

The goal of RF analogue circuit design with ultimate accuracy has been sought by both modelling and circuit engineers for a long time. The necessity to consider the electro-magnetic (EM) effects has been recognized because the electro-magnetic behaviour of the signal line and the passive elements can have considerable effect on the circuit performance.

The following phenomena become prominent: the self-inductance, skin effect and mutual electrical coupling between signal lines and the electro-magnetic loss of silicon substrate. These factors are as important for the design as for the accuracy of the transistor SPICE model. Moreover, the issue becomes even more critical as the operating frequency of RF circuits is increased.

Introduction of the above phenomena into the model is not easy because of their dependence on the type of the layout, location, size of the device, the number and the structural configuration of the transistor, etc. Thus, for the circuit design of chips intended for mass production, the electro-magnetic behaviour has still not been introduced until today.

In this paper, ways to overcome this problem for the semiconductor industry have been proposed. This is a new simulation technique, EM-co-simulation [1].

The main idea is to share the results of EM simulation with the circuit simulation. Each step, as well as the results of the verification will be explained in this paper.

All the test structures presented in this paper have been fabricated in TOSHIBA's 3.3 V, 0.40 μm rule SiGe BiCMOS technology. The maximum values of f_T and $f_{\max}$ of n-p-n transistors are 30 GHz and 50 GHz, respectively, and the maximum f_T of NMOS is about 20 GHz. Three metal layers have been implemented with the uppermost layer of 3 μm thickness dedicated for the fabrication of inductors.

This report consists of the following parts:

- selection of CMOS SPICE model,
- investigation of the applicability of EM simulation,
- verification of the circuit performance by using EM-co-simulation technique.

2. Selection of CMOS SPICE model

An accurate transistor model is the most essential matter for the real circuit design. Lately, surface potential (SP) based MOS models, such as EKV [3–5], HiSIM [6] and SP [7] have become well recognized.

Among these three models, only EKV Version 2.6 (EKV2.6) has already been implemented into several commercial-based simulators, therefore, a comparison in terms of DC and small signal output characteristics between EKV 2.6 and BSIM3 Version 3.2 (BSIM3V3.2) [8, 9] was made.

2.1. Device measurement and stability test

Before starting the discussion on the accuracy of the above two models, one should rather clear the measurement stability issue first to make the discussion trustworthy. Its solution is to analyze the robustness of the measurement data by using statistical approach. The detailed procedure will be explained in the following section.

The measurement of MOS transistors with three geometries: large ($L_g = 10$ μm, $W_g = 10$ μm), short ($L_g = 0.4$ μm, $W_g = 10$ μm), and narrow ($L_g = 10$ μm, $W_g = 0.6$ μm), has been performed by two persons for 4 chips belonging to one wafer. This 8 (= 4 times 2) sets of measurements have been repeated three times. A total of 24 measurement data for each size have been collected. Agilent's HP4156 with cascade probe station has been used as a measurement tool.

To evaluate the model's accuracy two quantities Dev_g_{ms} and Dev_n_{fact} have been introduced defined by the following formulae:

$$\text{Dev_}g_{ms} = \sum_{large,short,narrow} \sum_{\frac{I_D}{I_{spec}}=0.1}^{\frac{I_D}{I_{spec}}=10} \frac{|\text{meas}(g_{ms}) - \text{sim}(g_{ms})|}{\text{sim}(g_{ms})}, \tag{1}$$

$$\text{Dev_}n_{fact} = \sum_{large,short,narrow} \sum_{\frac{I_D}{I_{spec}}=0.1}^{\frac{I_D}{I_{spec}}=10} \frac{|\text{meas}(n) - \text{sim}(n)|}{\text{sim}(n)}. \tag{2}$$

The measurement and calculation of g_{ms} (normalized gate-to-source conductance) and n (slope factor) have been done using formulae (3)–(9), where I_D is the drain current, U_T is the thermal voltage (= kT/q), q is the electron charge, ε_{si} is the silicon permittivity, N_{sub} is the doping concentration in silicon, and V_{TO} is the threshold voltage.

Using (4), the universal function G_s expressed by (3) [5] can be obtained from the g_{ms}, that can easily be obtained from the simulation and measurement data. In this sense, G_s is a useful figure, because both simulated and measured behaviour of a MOSFET should follow this function:

$$G_S = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{I_D}{I_{spec}}}}, \tag{3}$$

$$g_{ms} \equiv -\left.\frac{\partial I_D}{\partial V_S}\right|_{V_G, V_D} = \frac{G_S \cdot I_D}{U_T}, \tag{4}$$

where:

$$I_{spec} = 2 \cdot n \cdot U_T^2 \cdot \mu \cdot C_{ox} \cdot \frac{W}{L}, \tag{5}$$

$$n \equiv \left[\frac{\partial V_P}{\partial V_G}\right]^{-1} = 1 + \frac{\text{GAMMA}}{2\sqrt{\Psi_o + V_P}}, \tag{6}$$

where:

$$V_P \cong \frac{V_G - V_{TO}}{n}, \tag{7}$$

$$\text{GAMMA} = \sqrt{2q\varepsilon_{\text{si}} N_{sub}}/C'_{ox}, \tag{8}$$

$$\Psi_0 = 2 \cdot U_T \cdot \ln\left(N_{sub}/n_i\right). \tag{9}$$

The Dev_g_{ms} and Dev_n_{fact} have been calculated and statistical analysis has been performed with Minitab [10] software using the obtained data. Figures 1 and 2 show the statistical distribution of Dev_g_{ms} and Dev_n_{fact} and

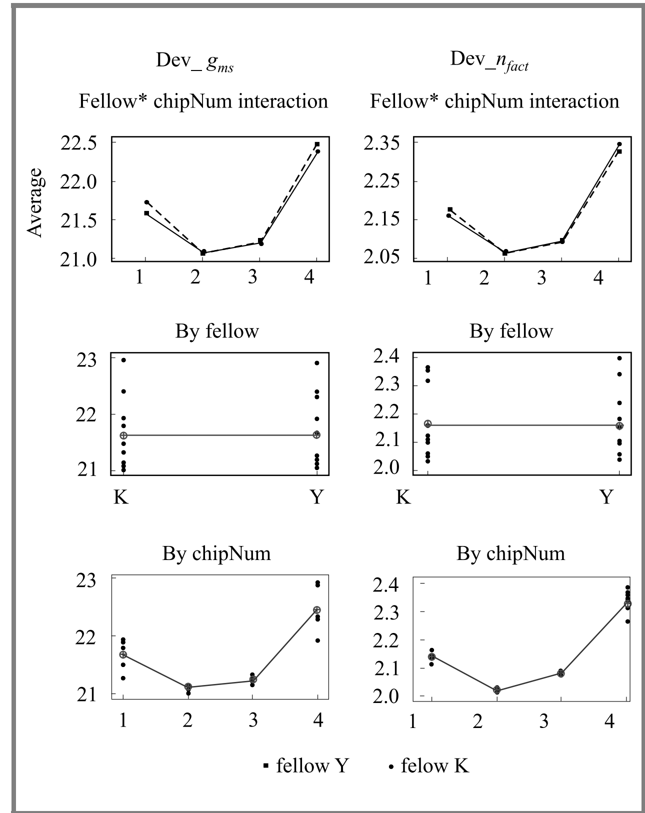

Fig. 1. Run chart of Dev_g_{ms} and Dev_n_{fact} in the case of EKV2.6 model.

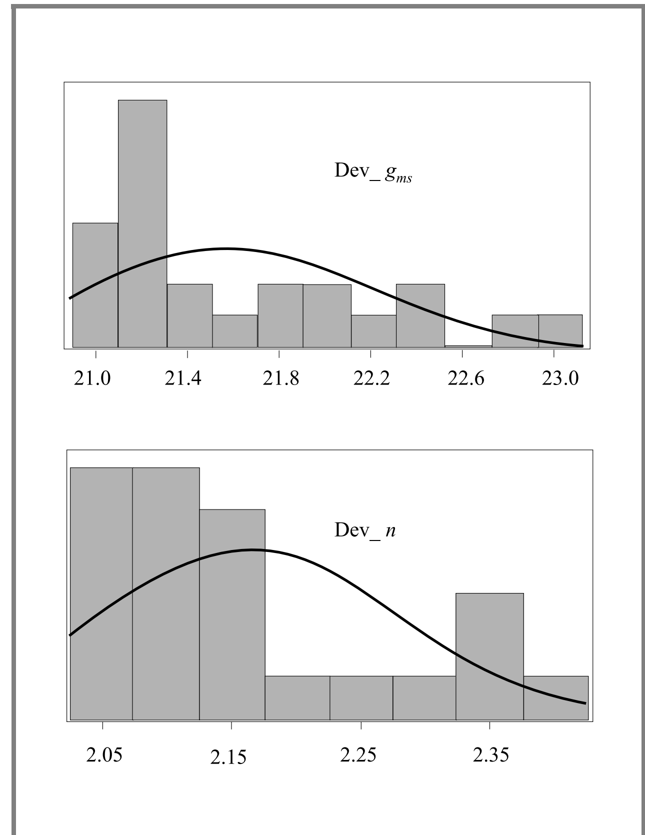

Fig. 2. Statistical distribution of Dev_g_{ms} and Dev_n_{fact} values in the case of EKV2.6 model.

Table 1 summarizes the analytical result. Gauge R&R in Table 1 is the measure of the stability of the measurement system, which is the total sum of % contribution of three factors: (1) repeatability, (2) reproductivity and (3) measurement operator. The theory requires that Gauge R&R should be less than 20% [10].

Table 1
Summary of the stability test of Dev_g_{ms} and Dev_n_{fact} in case of EKV2.6 model

Factor for robustness	Contribution [%]	
	Dev_g_{ms}	Dev_n_{fact}
Total Gauge R&R	5.49	13.12
– repeatability	5.49	13.12
– reproductivity	0	0
– fellow	0	0
Part-to-part	94.51	86.88
Total variation	100	100

The resultant Dev_n_{fact} and Dev_g_{ms} value in Table 1 was 5.49% and 13.2% respectively, which is less than 20%. It has been concluded that the way of measurement used in this study is stable and independent of the measurement operator so that the obtained measurement data is trustworthy.

2.2. Results and discussion of the benchmark test

The SPICE parameter extraction for EKV2.6 and BSIM3V3.2 models was done. The number of model parameters was 26 in the case of extraction based on EKV2.6 (including 22 original parameters and 4 parameters for extrinsic elements) and 81 in the case of BSIM3V3.2 (all 81 original parameters). Simulation data has been generated by Synopsys's HSPICE2002.2. Agilent's ICCAP has been used for verification and parameter extraction.

It should be noted that the parameters of both models include the temperature effects in the range from $-40°$C to 150°C. The number of the variations of geometrical test patterns used for the extraction is 19 (gate length ranges from 0.35 μm to 10 μm, and gate width from 0.6 μm to 10 μm).

After parameter extraction, simulation data was generated to calculate Dev_g_{ms} and Dev_n_{fact}, and the median value of 24 samples for each model was obtained using the Minitab software. Discussion on the modelling accuracy has been done based on this median value.

Figure 3 shows the comparison of G_s between EKV2.6 and BSIM3V3.2 for short and large devices. One should focus

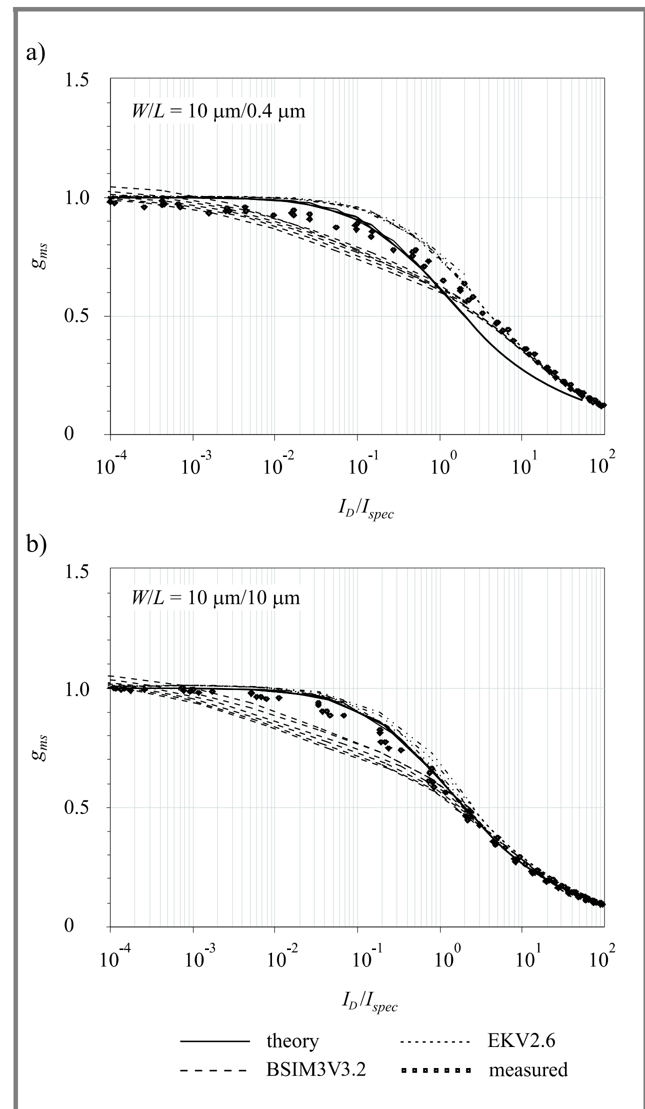

Fig. 3. The benchmark result of $G_s(= g_{ms}U_T/I_D)$ according to EKV2.6 and BSIM3V3.2 for: (a) short device ($I_{spec} = 3.0$ μA); (b) large device ($I_{spec} = 280$ nA).

on the G_s value in the range $0.1 < I_D/I_{spec} < 10$, which corresponds to the operation region of MOSFET between moderate and strong inversion, which is typically used for analogue circuits. This figure shows that both theoretical and measured G_s values match well. This means that the formula (3) is a valid expression for MOSFETs output characteristics.

As for the simulated results between two models, the EKV2.6 model is a better fit with G_s than BSIM3V3.2 in the whole range of I_D/I_{spec}. This fact indicates that EKV2.6 can describe the real behaviour of MOSFETs much better than BSIM3V3.2.

Comparison of the slope factor n has been performed and the results are given in Fig. 4. Strange behaviour has been observed in the case of BSIM3V3.2 results. The BSIM3V3.2 curve started decreasing for voltages below $V_{GB} = 0.7$ V and then increasing sharply for V_{GB} more

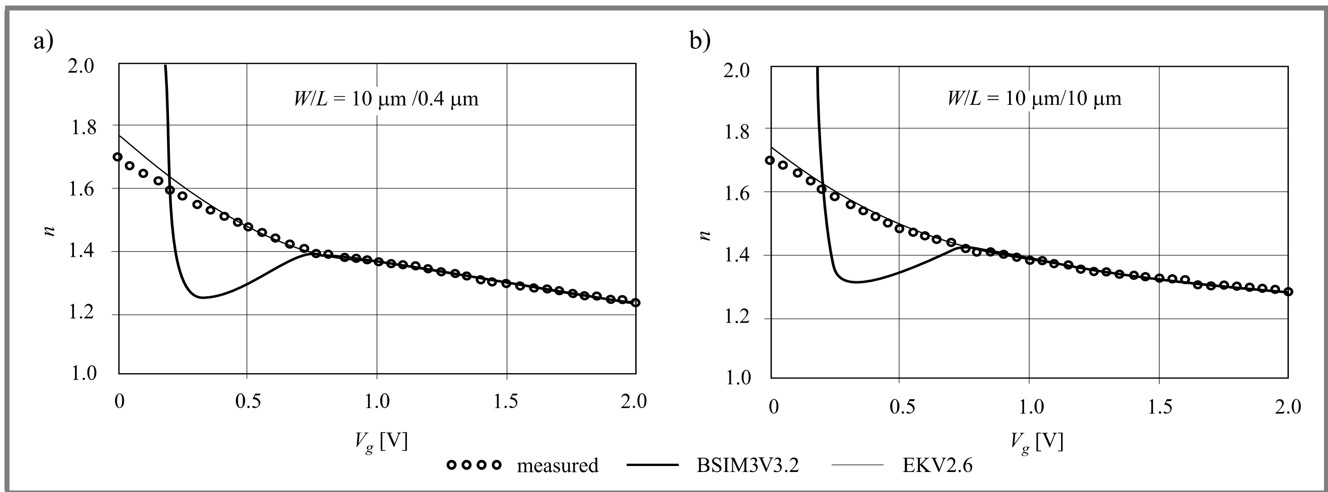

Fig. 4. The benchmark result of n factor according to EKV2.6 and BSIM3V3.2 for: (a) short device; (b) large device.

Fig. 5. Fitting result of EKV2.6 model of short (a, b, c) and large (d, e, f) device for three ambient temperatures.

closer to 0, while the EKV2.6 curve is in good agreement with the measured data.

The results are summarized in Table 2. Dev_g_{ms} for EKV2.6 was 21.0, which is approximately 1/5 of that of BSIM3V3.2 (99.0). The same holds for Dev_n_{fact} which was only 2.10 for EKV2.6, while it rose to 28.3 for BSIM3V3.2, which is 13.5 times higher. This confirms that EKV2.6 is better to use than BSIM3V3.2. These results coincide completely with those presented by Dr. Matthias Bucher [5].

Table 2
Comparison of Dev_g_{ms} and Dev_n_{fact} values calculated according to EKV2.6 and BSIM3V3.2

Contents	EKV2.6	BSIM3V3.2
Dev_g_{ms}	21.0	99.0
Dev_n_{fact}	2.10	28.3

Figure 5 shows the results of the verification of EKV2.6 models over three ambient temperatures (−40°C, 27°C and 80°C). It is amazing that this superb fit could be obtained using only 26 model parameters.

As a result of the above investigation, EKV2.6 was chosen for the entire study in this research.

2.3. Modification of the MOSFET SPICE model for RF application

In the previous section, the modelling accuracy of the intrinsic part of MOSFET has been discussed. However, the following extrinsic elements should be taken in account in the case of high frequency circuit operation:

1. Ohmic resistance of the gate material.
2. Resistance between source or drain and the substrate.
3. Coupling capacitances between gate, drain and source, respectively.

Figure 6 shows the EKV2.6 model modified for RF application [11–14]. Two added resistors R_G and R_B describe the gate and substrate resistance, respectively. Two capacitances (C_{GDFI} and C_{GSFI}) placed between the gate and drain, and gate and source are the sum of the overlap capacitances for the intrinsic part (C_{GD} and C_{GS}) and the extrinsic part describing the coupling between gate and drain, and gate and source electrodes (C_{GD_FI} and C_{GS_FI}) .

These values have been related to the physical layout by the following formulae [13, 14]. In the following section, extraction procedure of these values will be explained later.

- - - Device configuration - - -

L_g	[m]	: gate length
W_f	[m]	: finger length
Multi		: numbers of parallel devices
R_{PSH}	[Ω/square]	: sheet resistance of gate material
R_{GCT}	[Ω]	: gate contact resistance

- - - Gate resistance reduction factor - - -

$$FRG = \frac{1}{3} \quad \text{(one sided)} \tag{10}$$

$$FRG = \frac{1}{12} \quad \text{(double sided)} \tag{11}$$

- - - Formula for the extraction of R_G - - -

$$R_{GSH} = R_{PSH} \cdot FRG \tag{12}$$

$$R_G = \frac{R_{GCT} + R_{GSH} \cdot W_f / L_g}{\text{Multi}} \tag{13}$$

- - - Formula for the extraction of R_B- - -

R_{bref} : R_B value used for best fit

W_{fref} : finger length used to fit R_B

$$R_B = \frac{R_{bref} W_{fref}}{W_f \,\text{Multi}} \tag{14}$$

- - - G-D coupling capacitance - - -

$$C_{GDFI} = (C_{GD} + C_{GD_FI})\, W_f \,\text{Multi} \tag{15}$$

- - - G-S coupling capacitance - - -

$$C_{GSFI} = (C_{GS} + C_{GS_FI})\, W_f \,\text{Multi} \tag{16}$$

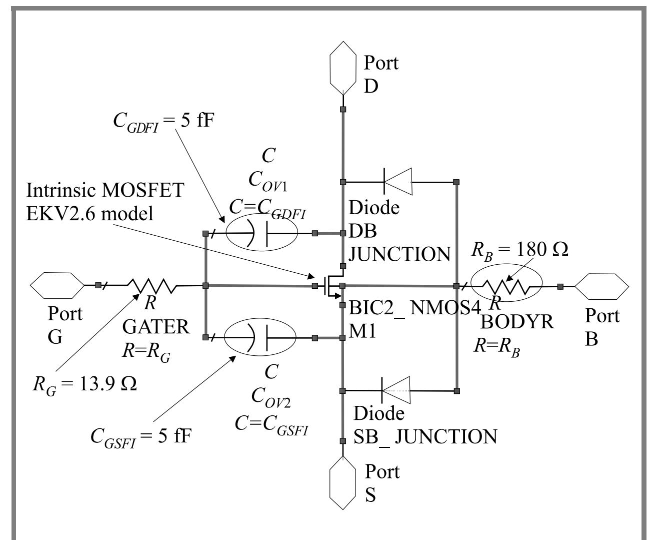

Fig. 6. Subcircuit-based EKV2.6 model with W_f (finger length) = 20 μm, L_g (gate length) = 0.4 μm, and Multi (numbers of fingers) = 5.

3. Investigation of the applicability of EM simulation

In this section, the results of the investigation of the applicability of electro-magnetic simulation will be explained using pad and inductor structures. Agilent's Momentum [1] has been used as a simulation tool.

3.1. Verification using pad structure

Figure 7 is the layout view of the pad structure used as the first case of the investigation. This is 1 port ground (G)-signal (S)-ground (G) configuration with 150 μm pitch. Two G pads are connected to the silicon substrate through guard ring. Figure 8 illustrates the cross sectional information on the BiCMOS process used for the Momentum simulation. A thin conductive layer with variable thickness (d), which has the same resistivity as the bulk sub-

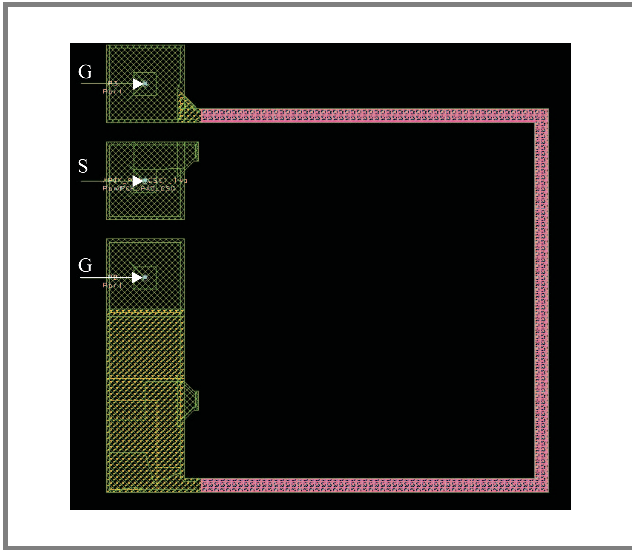

Fig. 7. Layout of the pad structure used for the verification of Momentum.

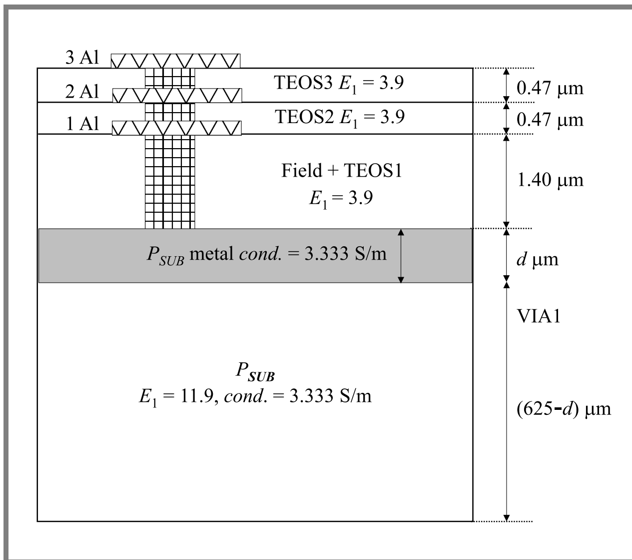

Fig. 8. Cross sectional information on TOSHIBA's 0.4 μm BiCMOS technology used for Momentum simulation.

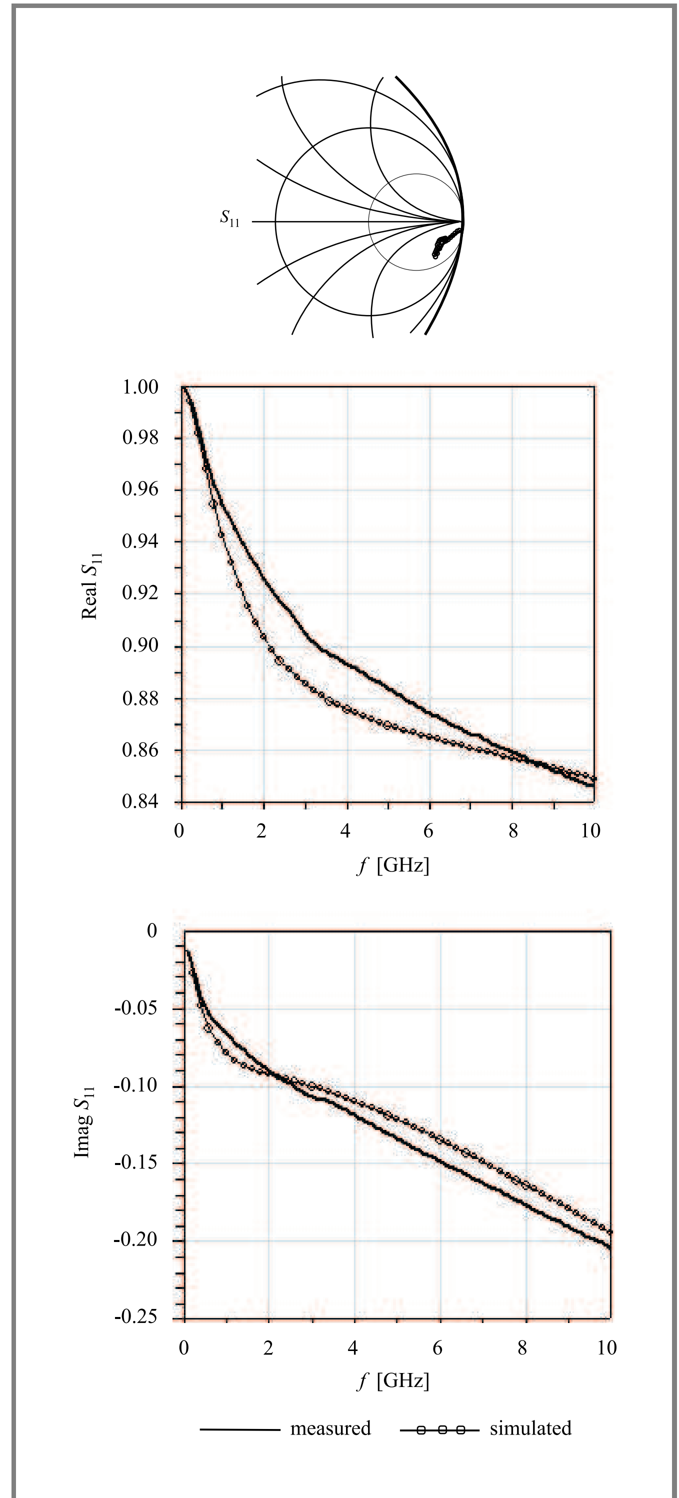

Fig. 9. Comparison of the S_{11}-parameter data obtained from Momentum simulation with measurement data of the structure shown in Fig. 8. Covered frequency range: from 100 MHz to 10 GHz.

strate, is placed on top of the substrate. Its role is to modify the amount of eddy current induced in the substrate. Because the actual value of d is unknown and typically process dependent, optimization has been used to find the best match with the measurement data.

The optimum d was obtained by fitting with S_{11} measurement data (frequency range: 0.1 GHz to 10 GHz) of the structure presented in Fig. 7. Figure 9 shows the results of S_{11} fitting with the case of $d = 60$ μm. The simulation RMS error stayed below 12.2% for the real part and 2.5% for the imaginary part, respectively.

3.2. Verification using inductor structure

The d value of 60 μm obtained previously has been verified using inductor shown in Fig. 10. The pad configuration is the same as in the previous case, and the distance between the inductor and guard-ring was 20 μm.

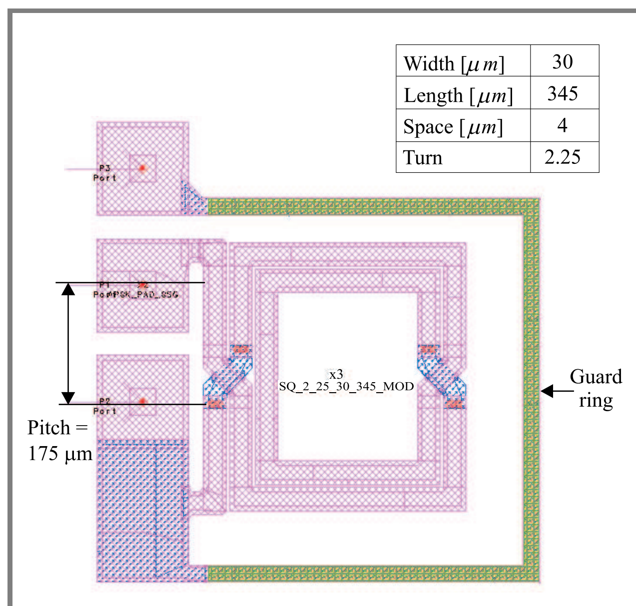

Fig. 10. Layout of the 2.25 turns of inductor used for the verification of Momentum.

Figure 11 shows a comparison of S_{11} and quality factor Q between simulation and measurement. Very good match has been obtained in this case, too. The S_{11} simulation RMS error was kept below 2.0% for the real part and 2.2% for the imaginary part, respectively.

The applicability of EM simulation has been verified using two structures, and good match between measurement and simulation has been obtained. It was achieved by adding the conductive layer with 60 μm thickness on top of the bulk silicon substrate. It is believed that the same approach may be applied to other silicon technologies as well.

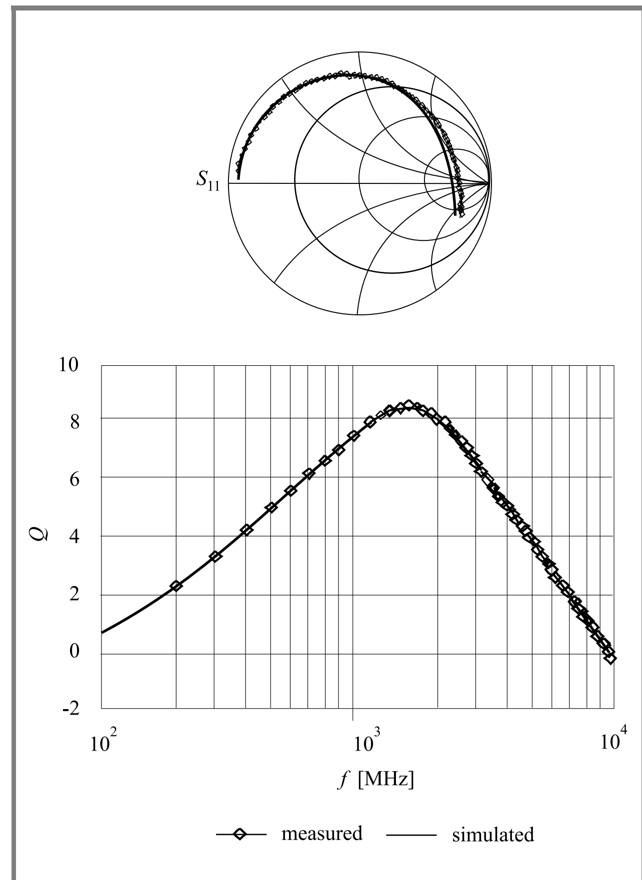

Fig. 11. Comparison of the S_{11}-parameter data obtained from Momentum simulation with measurement data of the structure shown in Fig. 8. Covered frequency range: from 100 MHz to 10 GHz.

4. Verification of the circuit performance using EM-co-simulation technique adapted for two design examples

The extended EM simulation technique applied for circuit design will be explained in this section. This is called electro-magnetic co-simulation. This technique has been applied to two cases, 1) CMOS differential amplifier and 2) 1.9 GHz CMOS VCO, and the results will be explained.

4.1. Case 1: CMOS differential amplifier

4.1.1. Description of the circuit

The layout and schematic of the CMOS differential amplifier used in this study are shown in Figs. 12 and 13, respectively. This is a single-ended configuration. Five pads,

located on the upper side of the circuit are for the DC power supply, and two sets of G-S-G pads on both sides are provided for the input/output. This circuit, which is fully dedicated for the verification of model parameters, has the following features.

1. **Unified device configuration to suppress the process fluctuation effect.**

   All transistors in the circuit are NMOSFETs with the following geometry and configuration of R_G:

$$L_g \text{ (gate length)} = 0.4\ \mu\text{m}, \tag{17}$$

$$W_f \text{ (finger length)} = 20\ \mu\text{m}, \tag{18}$$

$$\text{Multi (numbers of parallel devices)} = 5, \tag{19}$$

$$FRG = \tfrac{1}{3} \text{ (single-sided gate contact)}, \tag{20}$$

$$R_{PSH} \text{ (sheet resistance of gate material)} = 3.5\ \Omega\text{/square}, \tag{21}$$

$$R_{GCT} \text{ (gate contact resistance)} = 3\ \Omega, \tag{22}$$

$$R_{GSH} = R_{PSH} \cdot FRG = 1.67\ \Omega\text{/square}, \tag{23}$$

$$R_G = \frac{R_{GCT} + R_{GSH} \cdot W_f / L_g}{\text{Multi}} = 12.3\ \Omega. \tag{24}$$

   All resistors are used with a series or parallel connection of the 300 Ω resistor having 4 μm width. This is aimed at reducing the effect of process fluctuations, which strongly depends on the resistor width.

2. **Only 1st and 2nd metal layers have been used**.

   This is for practical reasons. A shorter turn-around time was expected.

3. **Special pattern has been fabricated to calibrate out the parasitic impedances of the pads**.

   Open calibration pattern was prepared to detect the intrinsic behaviour of the circuit.

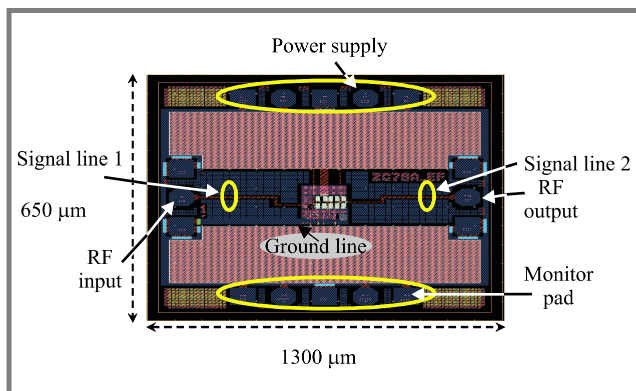

Fig. 12. Layout of CMOS differential amplifier.

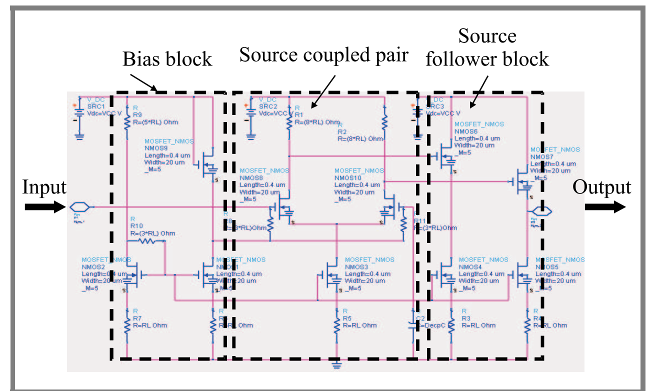

Fig. 13. Schematics of CMOS differential amplifier shown in Fig. 12.

4.1.2. Conditions of the measurement and simulation

The two port S-parameter measurement was done in the following conditions:

– frequency range: 0.1 GHz to 6 GHz with 0.1 GHz step,

– supply voltage: 2.8 V to 3.4 V with 0.2 V step,

– instrument: Agilent's HP8510B network analyzer and HP4142 DC supply.

4.1.3. Characterization of signal lines using Momentum

To predict the high frequency behaviour more accurately, the effect of series parasitic impedances of the following lines should be taken into account, because such effects cannot be removed by open de-embedding procedure only:

1) signal line between RF input pad and the core circuit,

2) signal line between RF output pad and the core circuit,

3) ground line between ground and the core circuit.

Momentum simulation has been used to characterize these three lines. The layout data of the above signal lines were picked up and used for Momentum simulation. The resulting S-parameters have been converted into the equivalent circuit as shown in Fig. 14 and the parameters of the circuit equivalent model were calculated by the formulae listed in Table 3.

In Fig. 14 L_s and R_s is the series inductance and resistance. $C_{ox1(2)}$ is the coupling capacitance between metal lines and silicon substrate, which is usually estimated by the insulator capacitance. The parallel network of $R_{sub1(2)}$ and $C_{sub(2)}$ denote the signal loss regarding eddy current generated

in the substrate. The formulae in Table 4 exhibit the case for symmetrical topology. Nevertheless, this can be expanded to the asymmetrical case by introducing y_{22} instead of y_{11}. The advantage of this methodology is that all the model parameters can be extracted directly from the measurement data without any use of optimization.

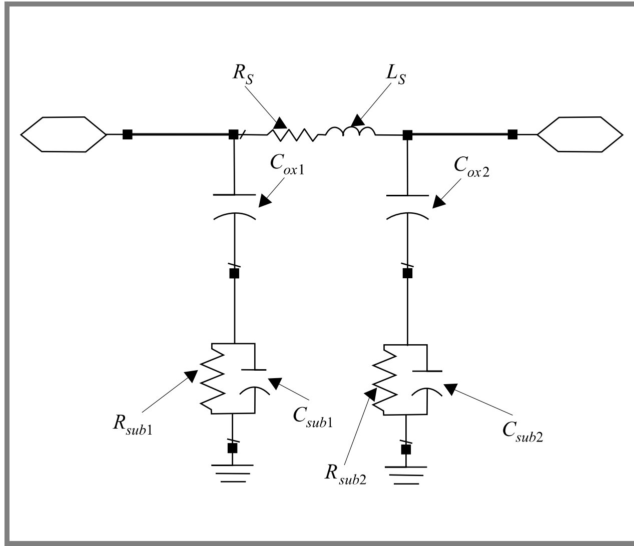

Fig. 14. Schematic description of the equivalent circuit of the signal line 1, signal line 2 and ground line shown in Fig. 12.

Table 3
Formulae for the extraction of the equivalent circuit of Fig. 14

Element	Extraction formula
L_s	$\dfrac{\mathrm{Im}\left(\frac{1}{y_{21}}\right)}{2\pi f}$
R_s	$\mathrm{Re}\left(\frac{1}{y_{21}}\right)$
$Z_{sub1(2)}$	$\dfrac{1}{y_{11(22)}+y_{21}} - \dfrac{1}{\mathrm{j}2\pi C_{ox}}$
$C_{ox1(2)}$	$\dfrac{-1}{2\pi f\,\mathrm{Im}\left[\frac{1}{y_{11(22)}+y_{21}}\right]}$ at low frequency end
$C_{sub1(2)}$	$\dfrac{\mathrm{Im}\left[\frac{1}{Z_{sub1(2)}}\right]}{2\pi f}$
$R_{sub1(2)}$	$\dfrac{1}{\mathrm{Re}\left[\frac{1}{Z_{sub1(2)}}\right]}$

The calculation methodology in Table 4 starts from the generation of π-structured network consisting of Y_1, Y_2 and Y_3.

Table 4
Equivalent-circuit elements of the three lines shown in Fig. 12 with the symmetrical topology assumed

Line element	L_s [nH]	R_s [Ω]	$C_{ox1(2)}$ [fF]	$C_{sub1(2)}$ [fF]	$R_{sub1(2)}$ [Ω]
Input	0.51	2.68	31.9	13.4	892
Output	0.51	2.79	54.2	13.2	1541
Ground	0.39	0.60	150.2	23.7	720

They are calculated based on the two-port y-parameters (y_{11}, y_{12}, y_{21}, y_{22}) according to the following relationship:

$$Y_1 = y_{11}+y_{12} \quad \text{or} \quad y_{11}+y_{21}, \tag{25}$$

$$Y_2 = y_{22}+y_{12} \quad \text{or} \quad y_{22}+y_{21}, \tag{26}$$

$$Y_3 = -y_{12} = -y_{21}. \tag{27}$$

Complete expressions for Y_1 and Y_2 can be written as the series impedance connection for $C_{ox1(2)}$ and $Z_{sub1(2)}$. Nevertheless, one assumption makes the extraction of $C_{ox1(2)}$, $C_{sub1(2)}$ and $R_{sub1(2)}$ simple. At the low frequency end, where the effect of eddy current is negligible, $Z_{sub1(2)}$ can be simplified to be a solo connection of $R_{sub1(2)}$. In this case, both Y_1 and Y_2 can be approximated in the following way:

$$Y_{1(2)} = \frac{1}{\mathrm{j}\omega C_{ox1(2)}} + \frac{1}{\frac{1}{R_{sub1(2)}}+\mathrm{j}\omega C_{sub1(2)}}$$

$$\cong \frac{1}{\mathrm{j}\omega C_{ox1(2)}} + \frac{1}{\frac{1}{R_{sub1(2)}}} = \frac{1}{\mathrm{j}\omega C_{ox1(2)}} + R_{sub1(2)} \tag{28}$$

Thus, $C_{ox1(2)}$ can be calculated from the imaginary part of Eq. (28). Care should be taken to obtain $C_{ox1(2)}$ value. It should be picked up from the data taken at a frequency as low as possible, where the introduced assumption is valid.
Then, $Z_{sub1(2)}$ can be defined by the remainder after subtracting the impedance of $C_{ox1(2)}$ from $Y_{1(2)}$:

$$Z_{sub1(2)} = \frac{1}{\frac{1}{R_{sub1(2)}}+\mathrm{j}\omega C_{sub1(2)}}$$

$$= Y_{1(2)} - \frac{1}{\mathrm{j}\omega C_{ox1(2)}}. \tag{29}$$

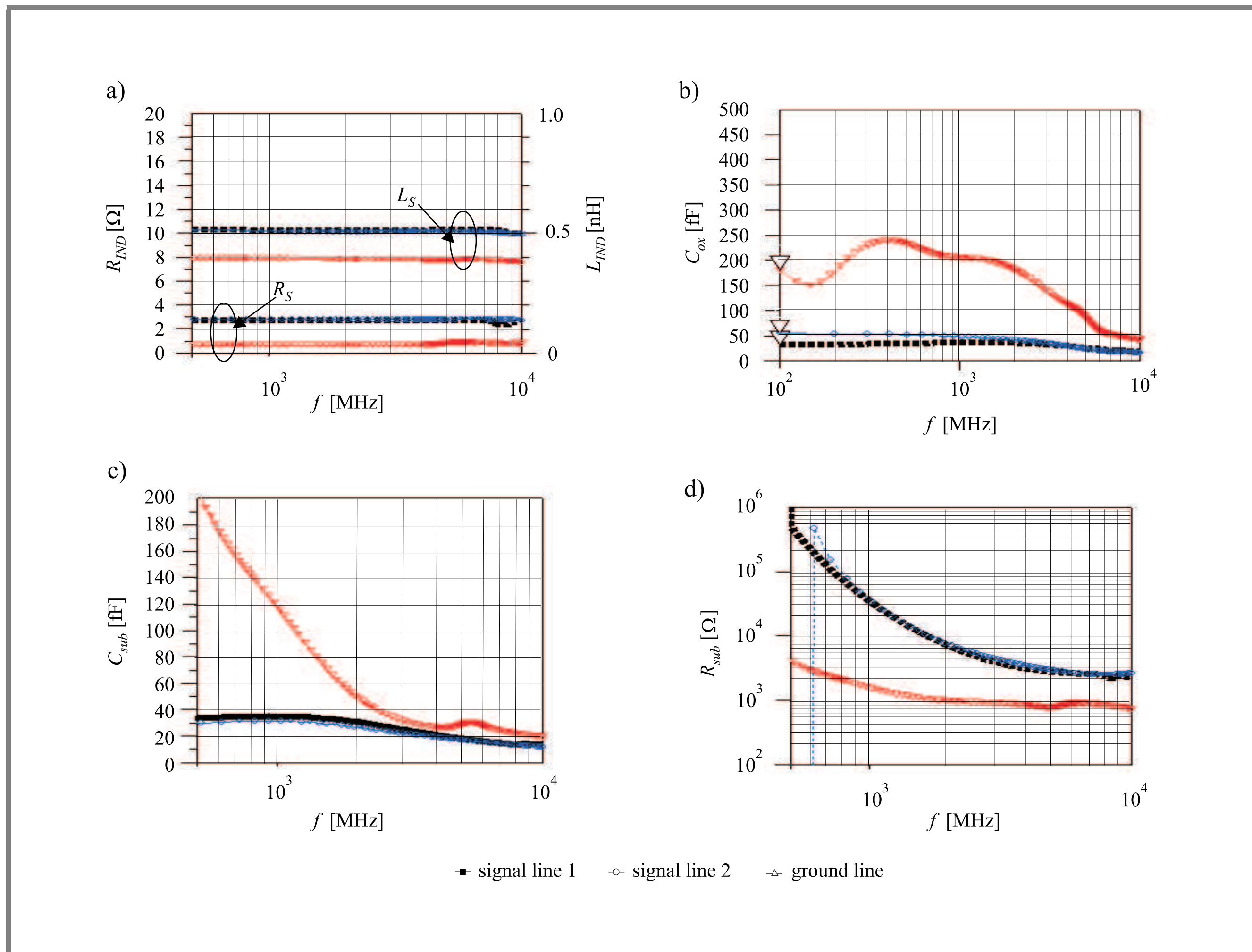

Fig. 15. Simulated frequency behaviour of L_S and R_S (a), C_{ox} (b), C_{sub} (c) and R_{sub} (d) of the three signal lines. Covered frequency range: from 100 MHz to 10 GHz.

Both $R_{sub1(2)}$ and $C_{sub1(2)}$ can be defined by the real and imaginary part of $Z_{sub1(2)}$, respectively. Figure 15 displays model parameters of the three signal lines, calculated by the formulae given in Table 3 (symmetrical topology ($Y_1 = Y_2$) is applied). Table 4 lists the obtained values.

4.1.4. Implementation of Momentum for the extrinsic parameter extraction of MOSFET models

The estimation of R_G, R_B, C_{GD_FI}, and C_{GS_FI} shown in Fig. 6 is very complex because they can hardly be recognized by the measurement data of the real device. Nevertheless, their accurate values should be extracted because they have strong influence on the high frequency characteristics.

The R_G value was extracted by the Momentum simulation using MOSFET layout data (configured by 5 fingers of 20 μm length with single-sided contact) of the gate electrode material as shown in Fig. 16. The two port y-parameters have been calculated between input port and 5 opposite ends. The R_G has been extracted by the real part of the resultant y_{21}:

$$R_G = \mathrm{Re}\left(-\frac{1}{y_{21}}\right). \tag{30}$$

Frequency dependency of R_G is plotted in Fig. 17. Extracted R_G value is approximately 13 Ω and is almost frequency independent. By comparing the estimated value as calculated in Eq. (24), it can be concluded that Eq. (13), used to calculate the initial value, can predict the R_G value with acceptable accuracy.

The determination of both C_{GD_FI} and C_{GS_FI} has been done in the same manner. The layout data shown in Fig. 18 was used for Momentum simulation. Both C_{GD_FI} and C_{GS_FI} have been calculated using the imaginary part of resultant y_{21} value:

$$C_{GS_FI}, C_{GD_FI} = \frac{1}{2\pi f \,\mathrm{Im}\left(\frac{1}{y_{21}}\right)}. \tag{31}$$

The result is shown in Fig. 19. Both capacitances are almost independent of the frequency and amounted to about 5 fF each.

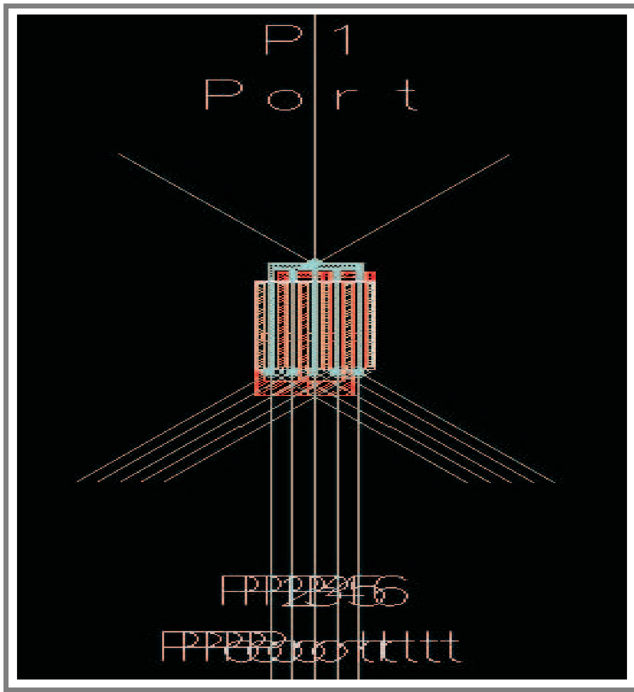

Fig. 16. Momentum setup for the extraction of R_G. Simulation target is the gate electrode material with 5 fingers of 20 μm length.

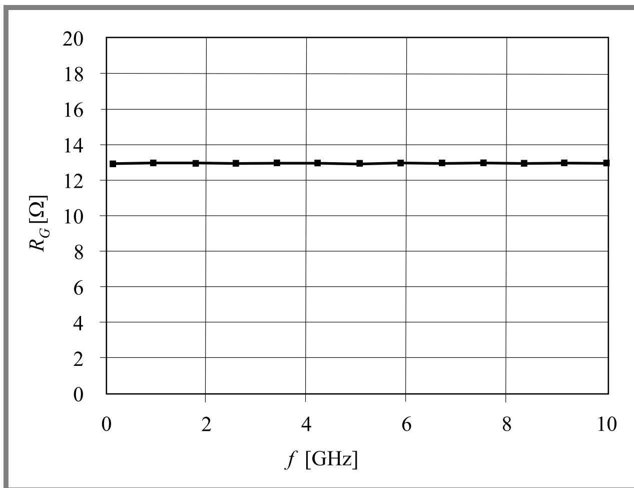

Fig. 17. Resultant R_G obtained using the setup shown in Fig. 16. Covered frequency range: from 100 MHz to 10 GHz.

The extraction of R_B was done as the last step. R_B has a strong effect on the S_{22} value of the circuit. This is because the output impedance of MOSFET, which forms the source-follower network, has a strong influence on the circuit's S_{22}. Mathematical optimization has been used to extract R_B. The effect of R_B on the circuit's S-parameters is displayed in Fig. 20. At R_B value of 180 Ω, best fit with the measurement was obtained. All parameters extracted in this section are summarized in Fig. 6.

With the lumped model of the signal lines and modified EKV2.6 model, the final simulation was performed.

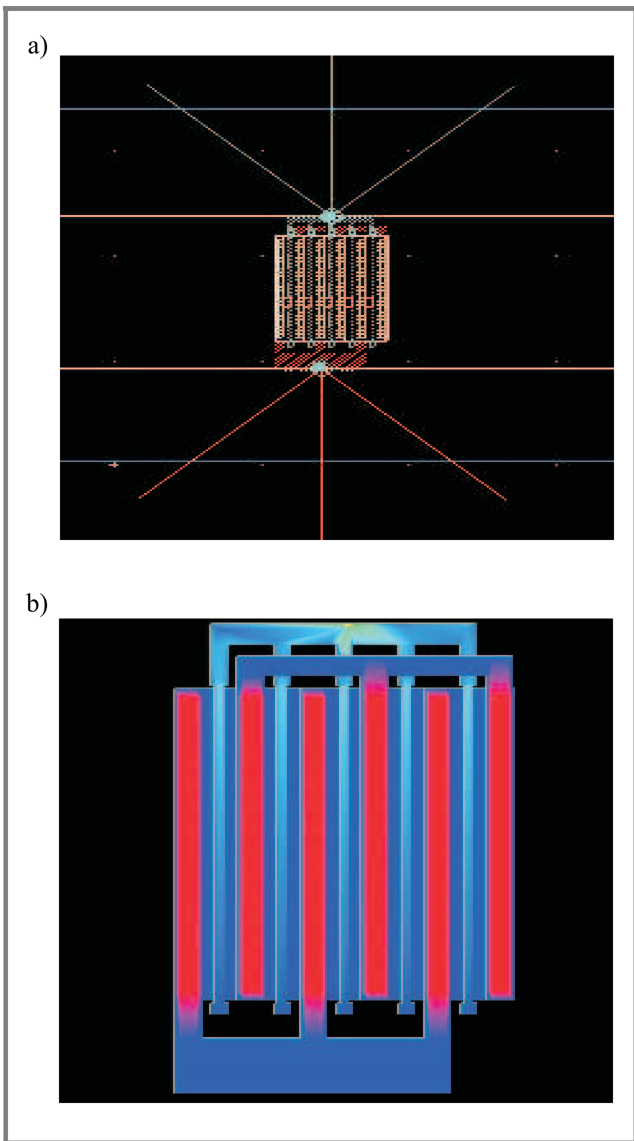

Fig. 18. (a) Setup for the extraction of C_{GS_FI} and C_{GD_FI}; (b) resultant current flow obtained from Momentum simulation. Simulation target is the gate material with the configuration as shown in Fig. 6.

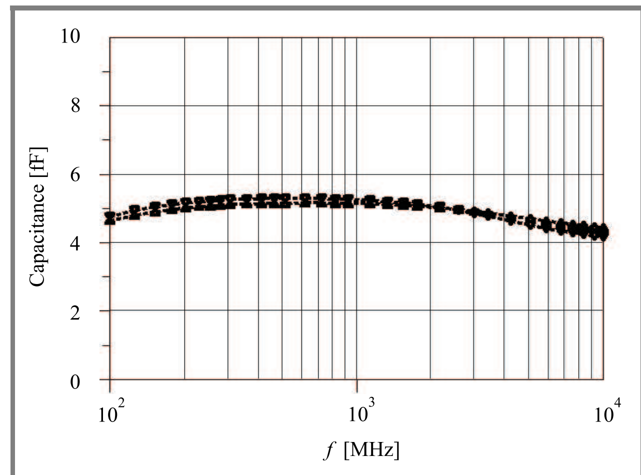

Fig. 19. Extracted C_{GD_FI} and C_{GS_FI}. Covered frequency range: from 100 MHz to 10 GHz.

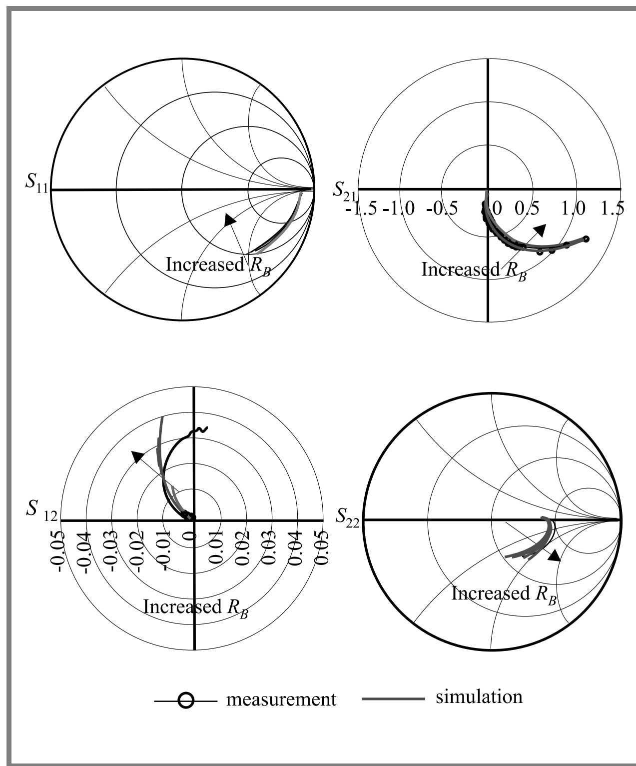

Fig. 20. Effect of R_B as shown in Fig. 6 on the *S*-parameters of the differential amplifier. Covered frequency range: from 100 MHz to 6 GHz.

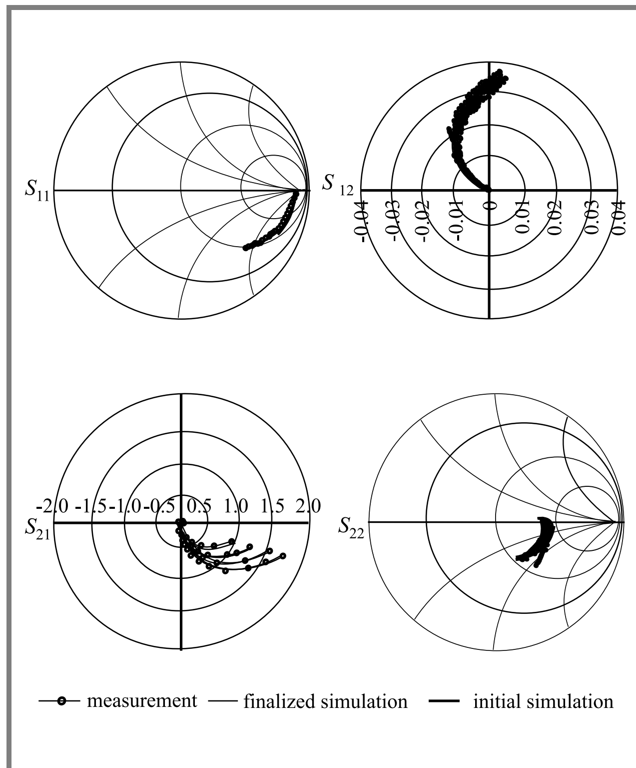

Fig. 21. Final simulation results with subcircuit-based RF-MOSFET (as shown in Fig. 6) and lumped signal line models (as shown in Fig. 13). Covered frequency range: from 100 MHz to 6 GHz.

The results are shown in Fig. 21. As seen, the simulated and measured *S*-parameter values are in very good agreement. Thus, the simulation accuracy of an RF circuit can be enhanced by the use of a proper device model and EM simulation.

4.1.5. Verification of amplifier behaviour using EM-co-simulation technique

As an extended example, EM-co-simulation technique will be presented in this section. The flow chart to execute EM-co-simulation is illustrated in Fig. 22. A layout-component, that is a symbolized layout block, can be used together with SPICE compact models as shown in Fig. 23. Agilent's ADS-2003C with Verilog-A code of EKV2.6 model was used for this simulation.

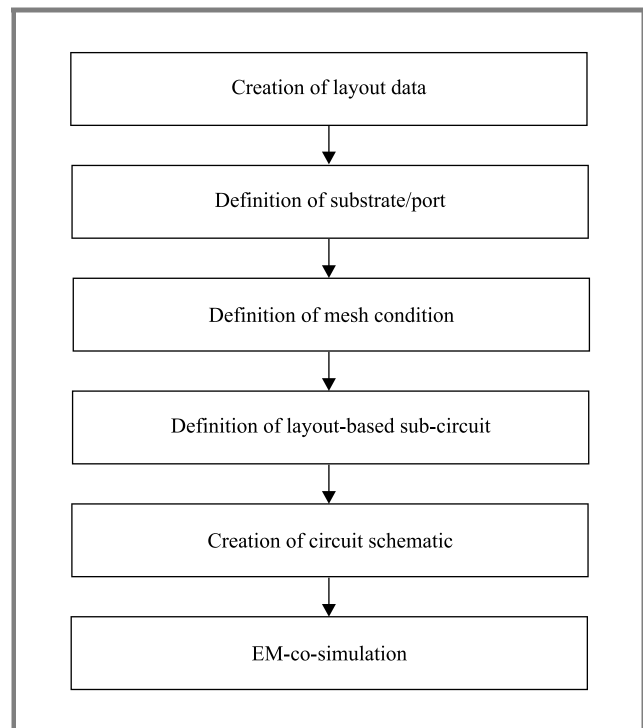

Fig. 22. Simulation flow of electro-magnetic co-simulation.

Figure 23 illustrates the view of the simulation schematic. The core part of the circuit is composed of spice components (transistors, resistors and capacitors), and other external components such as signal lines, pads are contained inside the layout-components.

At the first step of the simulation, EM simulation is invoked to analyze the *S*-parameters of the layout-component. After its completion, circuit simulation is followed by the use of the resultant *S*-parameters and compact model. Now that both accurate transistor model and EM simulation methodology is available, simulation results shows good agreement with the measurement data as shown in Fig. 24.

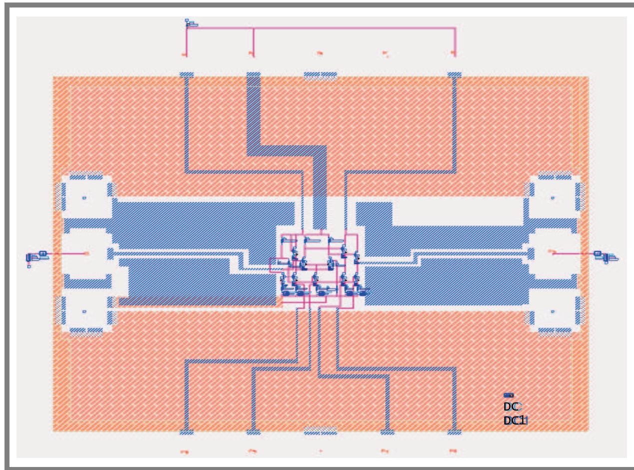

Fig. 23. The EM-co-simulation setup for the CMOS differential amplifier. Its schematic is shown in Fig. 13.

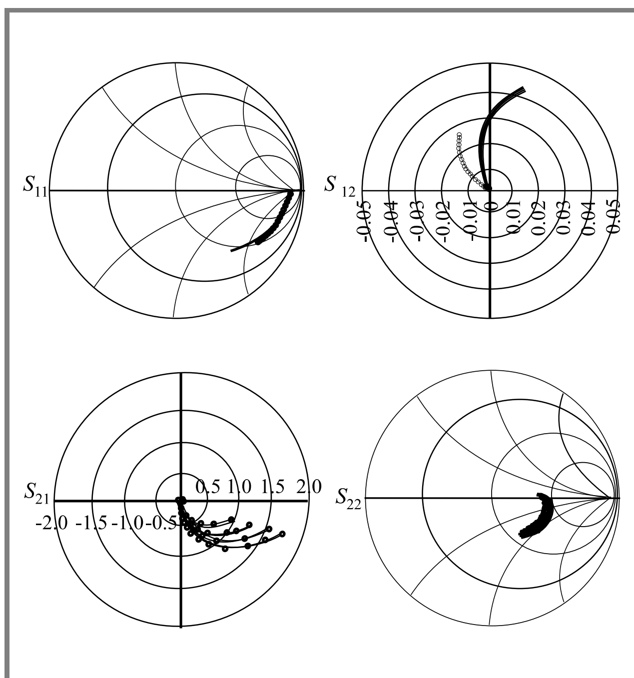

Fig. 24. Comparison between EM-co-simulation and measurement data of CMOS amplifier with the schematic shown in Fig. 13. Covered frequency range: from 100 MHz to 6 GHz.

The duration of the simulation of this example was 30 minutes on Solaris2.6 based EWS. The S-parameter values obtained from the Momentum simulation can be reused so that the duration of the second simulation did not take more than 30 seconds.

4.2. Case 2: 1.9 GHz CMOS VCO

4.2.1. Description of the circuit

The second adaptation example of the EM-co-simulation technique is the 1.9 GHz CMOS VCO design. Designing VCO is very difficult because many factors, such as the device model accuracy, parasitic elements and electromagnetic effect should be taken into account carefully in the course of the circuit design. The most difficult and critical issue is the characterization of tank circuit.

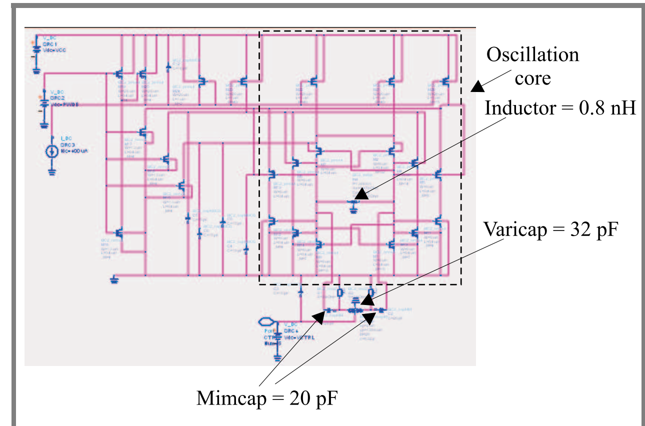

Fig. 25. Schematic of CMOS VCO for DCS1800 application.

The circuit schematic is displayed in Fig. 25. Six pairs of CMOS transistors with different numbers of fingers (unit size of 8 μm/0.4 μm) and a tank circuit (consisting of an inductor, a capacitor and a variable capacitor) constitute the main oscillator block.

The 2.75 turns of inductor used in the tank circuit have line and spacing of 40 μm/4 μm, and self inductance estimated from the Greenhouse formula [15] is 0.8 nH.

4.2.2. VCO measurement and simulation conditions

The frequency tuning characteristics and oscillation frequency have been measured with the supply voltage of 2.9 V and the control voltage (v_{ctrl}) swept from 0 V to 2.5 V with the step of 0.5 V.

4.2.3. Verification of VCO tuning behaviour using EM-co-simulation technique

The following two circuit simulations have been done for comparison:

1) circuit simulation using the schematic of Fig. 25 with the initial estimation (0.8 nH) of the inductance,

2) EM-co-simulation.

The schematic of (2) is displayed in Fig. 26. Simulation was using 7 tones' harmonic-balance simulation and Momentum simulation. The layout-component consisting of the tank circuit (inductor, leading line of varicap) and other signal lines between transistors and guard-ring was analyzed by the Momentum simulation.

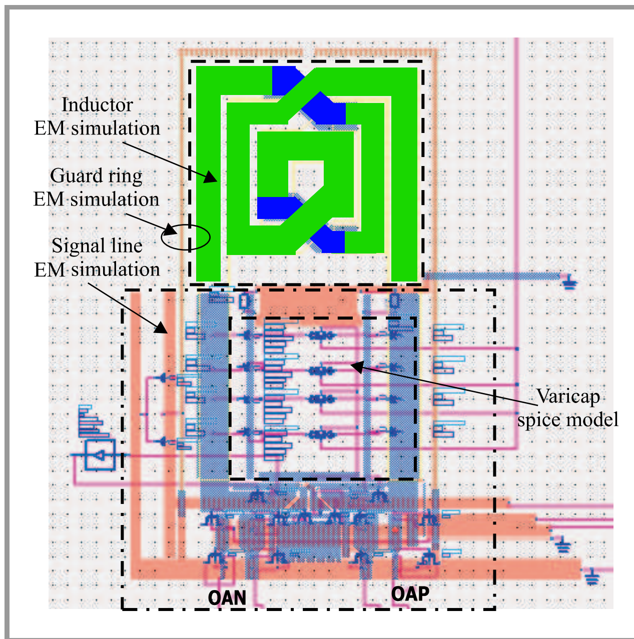

Fig. 26. Simulation setup of EM-co-simulation for CMOS VCO tuning characteristics.

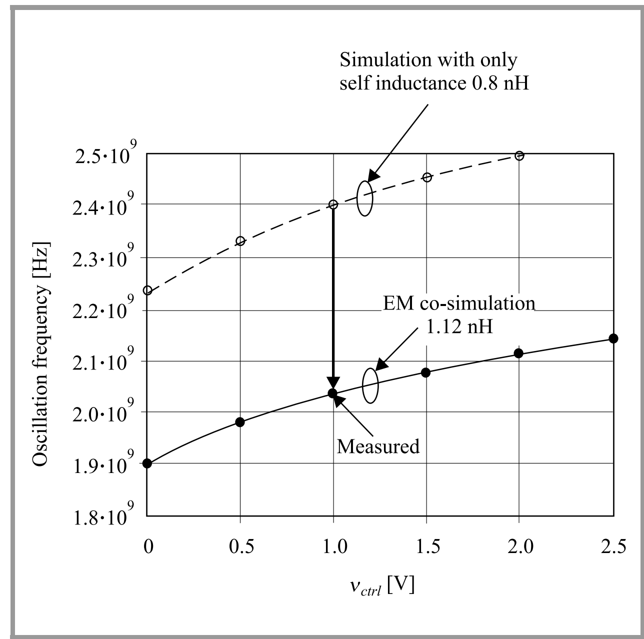

Fig. 27. Comparison of simulation results between EM-co-simulation and measurement of tuning characteristics of CMOS VCO.

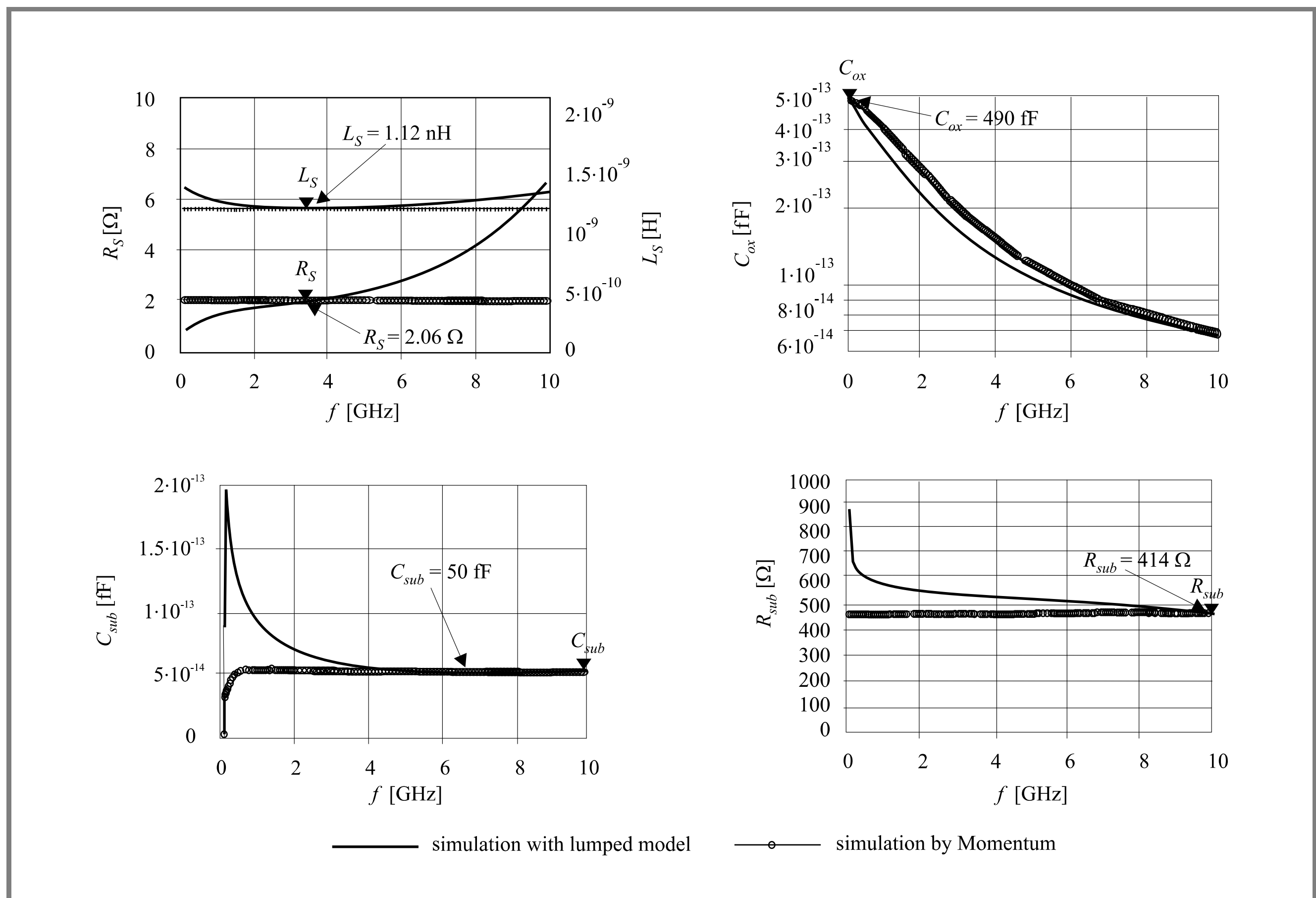

Fig. 28. Comparison of simulation characteristics of the inductor in the tank circuit between lumped model and Momentum. Model parameter values are displayed in the figure.

Simulation results for the two cases are compared in Fig. 27. The frequency deviation in the case (1) ranged between 330 MHz and 400 MHz from $v_{ctrl} = 0$ V to $v_{ctrl} = 2.0$ V, which approximately amounted to the frequency error of 16%–18%. In the case (2), the deviation has been drastically decreased to only 3 MHz difference from the measurement in the whole v_{ctrl} range. Thus, it can be concluded that EM-co-simulation is accurate and effective for the design of VCO circuits.

4.2.4. Detailed analysis of the tank circuit

The reason for the obtained accuracy in the case (2) seems to be the increase of the inductance in the tank circuit. This is confirmed by the Momentum analysis of the tank circuit layout. The values of the equivalent circuit as shown in Fig. 14 are $L_s = 1.12$ nH, $R_s = 2.06\ \Omega$, $C_{ox1(2)} = 490$ fF, $C_{sub1(2)} = 50$ fF and $R_{sub1(2)} = 414\ \Omega$. Figure 28 shows the comparison of simulation data of equivalent circuit with Momentum output.

The resultant L_s was 1.12 nH (a visible increase from the initial estimation of 0.8 nH), which means that the oscillation frequency was decreased by 15%. This increased inductance is ascribed to the parasitic inductances of the inductor's extension part, mutual coupling with the surrounding guard ring, and other electrical coupling.

Based on the above results, it can be concluded that the EM-co-simulation can incorporate the parasitic effects that cannot easily be estimated from the layout, and provides the circuit designer with the accurate prediction of high frequency circuit behaviour.

5. Conclusions

In this study, it has been proved that the proper use of good CMOS SPICE model (EKV2.6) and electro-magnetic simulation can yield a good match between measured and simulated data. Through the investigation of the applicability of EM simulation, using several test structures, it has been concluded that EM simulation is very useful for the estimation of inductor characteristics, layout parasitic components in the circuit and the extrinsic part of the transistor. EM-co-simulation is introduced as a new simulation technique. This can be used as a "post-layout tool" because of its acceptable accuracy.

To summarize, it can be concluded again that the use of both: accurate transistor model and electro-magnetic simulation is the shortest route to predict the behaviour of RF circuits in the most accurate way.

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