Invited paper

Trends in assembling of advanced IC packages

Ryszard Kisiel and Zbigniew Szczepański

Abstract—In the paper, an overview of the current trends in the development of advanced IC packages will be presented. It will be shown how switching from peripheral packages (DIP, QFP) to array packages (BGA, CSP) and multichip packages (SiP, MCM) affects the assembly processes of IC and performance of electronic systems. The progress in bonding technologies for semiconductor packages will be presented too. The idea of wire bonding, flip chip and TAB assembly will be shown together with the boundaries imposed by materials and technology. The construction of SiP packages will be explained in more detail. The paper addresses also the latest solutions in MCM packages.

Keywords— IC packages, SiP, wire bonding, TAB, flip chip.

1. Introduction

The development of the electronics industry is dominated by communication products, which are characterised by rapid market introduction and fast mass-manufacturing capabilities. The main drivers of this development are miniaturisation and styling or eco design and production. The industry has made great strides in reducing the package size from the dual in line package (DIP) and quad flat pack (QFP) to ball grid array (BGA) and chip scale package (CSP). Table 1 illustrates the current trends in IC packaging. Standard leadframe packages still have the largest market share. Packages like BGA and CSP have gained increasing importance and popularity. CSPs are used more often than BGAs, in packaging, e.g., of memory products, controllers and digital signal processors, due to their smaller size.

Table 1
Trends in IC packages, 2001–2006 [1]

Package type	Standard (QFP)	BGA	CSP
Max body size [mm]	30 → 32	40 → 50	27 → 20
Max number of I/Os	300 → 320	900 → 3500	400 → 650
Min lead/ball pitch [mm]	0.4 → 0.3	0.75 → 0.5	0.5 → 0.3
Max package thickness [mm]	1.4 → 1.0	2.0 → 1.0	1.2 → 0.7
Market share [%]	88 → 78	4 → 7	4 → 15
US$ ct/I/O	0.8 → 0.4	0.9 → 0.6	0.9 → 0.4

Table 2 compares the main features of QFP, BGA and CSP at a comparable I/O number in the range of 200–300. It is obvious that switching to CSP packages reduces the physical area occupancy on the PCB, about three times compared to QFP for this I/O range. Shorter connections offered by CSP reduce parasitic inductance and capacitance.

Table 2
Comparison of key features of various packages [2]

Feature	QFP	BGA	CSP
I/O	208	225	313
Pitch [mm]	0.5	1.27	0.5
Footprint [mm^2]	785	670	252
Height [mm]	3.37	2.3	0.8
Package to die ratio	8	7	1
Inductance [nH]	6.7	1.3 – 5.5	0.5 – 2.1
Capacitance [pF]	0.5 – 1	0.4 – 2.4	0.05 – 0.2

Compared to leaded packages such as QFPs, BGA and CSP packages are expensive. The cost is about twice as high, but when cost per I/O is taken into account the prices become almost the same. In addition, the substrates on which chips have to be used are generally more expensive because more layers and possibly microvias are needed.

2. Packaging technology requirements

System integration is a key element for manufacturing future products. The idea behind system integration is to combine individual components and subsystems into a functional electronic system. Assembly and packaging of the semiconductor products are an essential part of this process. The most difficult challenges facing the assembly and packaging industry, according to the ITRS roadmap, are as follows [1, 3]:

- Improved organic substrates. The substrates must be compatible with Pb-free solder processing. Improved impedance control and lower dielectric losses are needed to support higher frequency applications. The substrates must be characterised by low moisture absorption, improved planarity and low wrapage at higher process temperatures as well as low-cost embedded passives.
- Improved underfillers for flip chip on organic substrates. Underfiller must have improved flow, fast dispense/cure properties, better interface adhesion, and lower moisture absorption, as well as higher operating temperature range for automotive applications and Pb-free soldering in liquid dispense underfiller.

- Impact of Cu/low κ on packaging. Direct wire-bond and bump to Cu must be possible. Mechanical strength of dielectrics must be improved and bump as well as underfill technology must assure low κ dielectric integrity. New tests to measure the critical properties need to be developed.
- New system level technologies must be capable to integrate chips, passives and substrates. Embeded passives may be integrated into the "bumps" as well as the substrates. Bumpless area array technologies must be developed, for example for face-to-face connection.
- Pb, Sb and Br free packaging materials. New materials and processes must meet new requirements, including higher reflow temperature and reliability under thermal cycling.

To fulfil these requirements special attention must be paid to [8]:

– area array packaging (flip chip, CSP, SiP),
– cost efficient and flexible substrate materials,
– thin semiconductor chips,
– cost efficient bumping process,
– fine pitch and multilayer technology,
– integration of passive components into the substrate,
– integration of optical and electrical signal transmission,
– material characterization (model and measurement),
– environmentally compatible choice of materials and processes.

Such requirements are more prominent in cost-performance applications, such as notebooks, personal computers and telecommunication equipment [3, 4]. The key single-chip-package technology requirements are shown in Table 3. Economic aspects are especially important here. Assembly and packaging costs are expected to decrease over time on a cost-per-pin basis, but the chip and package pin-count is increasing more rapidly than the cost-per-pin is decreasing.

Table 3
Development of selected packaging parameters in the next decade [3, 4]

Parameter	Year		
	2002	2006	2010
Chip size [mm^2]	178	206	268
Cost [cents/pin]	0.75–1.44	0.56–1.03	0.48–0.98
Core voltage [V]	1.5	0.9	0.6
Package pincount	480–1320	550–1936	780–2700
Package thickness [mm]	1.0–1.2	0.8–1.2	0.65–0.80
Performance on chip [MHz]	2320	5630	12000
Performance: peripheral buses [MHz]	200/660	300/966/1062	300/1415
Junction temp. max [°C]	85	85	85
Chip interconnect pitch [μm]	35	20	20
Flip chip pitch [μm]	160	130	90

3. Bonding technology for chip packaging level

There are three chip-level interconnection technologies currently in use:

– wire bonding (WB),
– flip chip (FC),
– tape automated bonding (TAB).

Wire bonding is a well established bonding technology. This technique is used for over 90% of all interconnections. Flip chip is another technique that has been a steadly gain in importance, particularly in new applications where system performance and miniaturisation is important. It also offers special advantages in terms of high accuracy in chip placement by self-adjustment when solder bumps are on the die. This is of special interest for the integration of optical interfaces in electro-optical devices.
A concept of TAB process was initiated in the 1960s by General Electric. In the mid-90s TAB process was widely used in high volume products, such as Pentium laptops and high resolution printers [7]. Now it is not use so often. The comparison of the three bonding techniques, mentioned above, in aspect of signal propagation delay is shown in Table 4.

Table 4
Typical values for lead capacitance and inductance [7]

Bonding technique	Capacitance [pF]	Inductance min [nH]
Wire bond	0.5	6
TAB	0.6	2
Flip chip	0.1	0.2

Propagation time is directly proportional to the length of interconnection, the longer the lead the greater the propagation delay and the slower the off-the-chip system speed.

3.1. Wire bonding assembly

In "standard" packaging , the interconnection between the die and the carrier is made using the wire. Different types of wires are used for the wire bond process: gold, aluminium and copper. The die is attached to the carrier face up, then a wire is bonded first to the die, then looped and bonded to the carrier (Fig. 1) [9]. Wires are

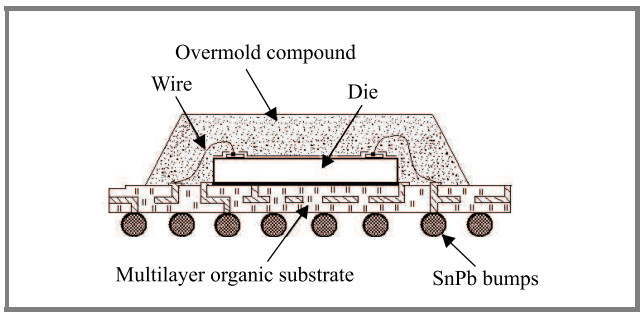

Fig. 1. Wire bonding technology applied in BGA package.

typically 1–5 mm in length and 25–35 μm in diameter. The process used most often to realize these interconnections is thermosonic bonding with gold wire.

3.2. Flip chip assembly

The term flip chip describes a method of establishing electrical connectors between the die and the package carrier. The interconnection between the die and the carrier in flip chip packaging is made through a conductive "bump" placed directly on the die surface. The bumped die is then "flipped over" and placed face down, with bumps connecting directly to carrier (Fig. 2). A bump is typically 70–100 μm high and 100–125 μm in diameter.

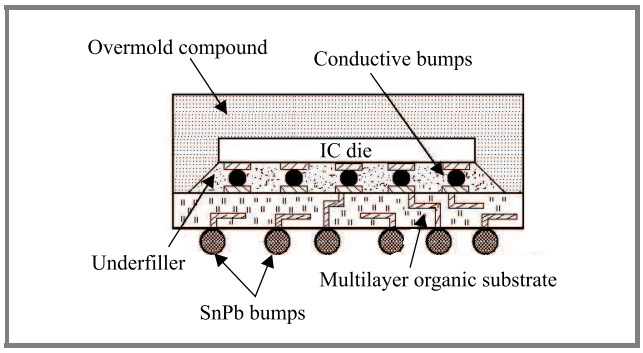

Fig. 2. Flip chip technology for inner assembly in BGA package.

The flip chip connection is generally formed in one of two ways: using solder or a conductive adhesive. The most common packaging interconnect is the eutectic SnPb solder. The solder bumped die is attached to a substrate by means of a solder reflow process. After the die is soldered, the underfiller is added between the die and the substrate. Underfiller is designed to control the stresses in the solder joints caused by the difference in thermal expansion between the silicon die and the carrier. Once cured, the underfiller adsorbs the stresses, reducing the strain in the solder bumps, greatly increasing the life of the finished package and reliability of solder joints.
The other method of establishing the flip chip connection is adhesive bonding. Various methods of joining can be used: connecting with isotropically or anisotropically conductive adhesives and using non-conducting materials. The bump material is predominantly gold. Without the danger of solder-bridge formation, smaller pitches can be implemented with adhesive techniques. Furthermore, substrates can be used which cannot withstand the melting temperature of the eutectic lead/tin solder or lead-free alloys. Adhesive flip chip bonding, based mainly on the anisotropically conductive adhesive, is the dominant technology for LC-displays assembly.
The main benefits and features that flip chip can offer are:

- High package density without the need for lead frame.
- Enhanced electrical performance as a result of short distance between chip and substrate, including minimal propagation delay, minimal transmission losses at high frequency, and low parasitic capacitance as well as inductance values.
- Low thermal resistance solder bonds serve primarily as heat-dissipating paths, thus suitable for high-speed electronic devices.
- Power can be spread directly from the core of the die to laminate (substrate). This greatly decreases the noise of the core power and improves performance of the silicon.
- Better suited to making small electronic modules, due to the low profile, reduced weight and space requirements.
- The entire surface of the die can be used for interconnecting. So, it can support vastly larger numbers of interconnects on the same die size. Flip chip technique is mainly used for assembling ball grid arrays. Such packages use PCB with, pitch above 500 μm and require large substrate areas. In the case of smaller pitch the CSP packages are used.

3.3. Tape automated bonding interconnection technology

The TAB process involves bonding Si chips to patterned metal on polymer tape, e.g., copper on polyimide, using thermocompression or solder bonding. Subsequent processing is carried out in strip form through operations such as testing, encapsulation, and burn-in, followed by excising of the individual packages from the tape and attachment to the substrate or board by outer lead bonding.
The copper leads on a thin polyimide film are made using subtractive photo-chemical process. Finally the leads have to be plated to retain solderability. Gang bonding of the bumped chip to copper tin plated leads on polyimide tape is performed using thermode heater. After chip protection TAB device is excised from polyimide tape, see Fig. 3 and next attached to the board surface bonding pads. Attachment technique includes pulse heated hot bar. This hot bar or thermode heater mechanically presses the leads onto bonding pads, which eliminates any coplanarity errors arising from lead forming. The main disadvantage of hot

bar soldering is the fact that a thermode has to be mechanically rigid, to exert the force on the component leads. Unfortunately, this force can be high enough to damage the substrate. To solve this problem, spring loaded thermode or thermode which can be held on a spherically mounted suspension unit are used. The last one allows the blades of thermode to be planarised with respect to the surface of the substrate. This yields uniform forces across all leads around the bonding site. Placement accuracy for TAB devices is tighter than for conventional SMD components, since the lead pitch is smaller in comparison to SMD. So, the machine positioning system must include reliable machined hardware, precision encoders and stable base.

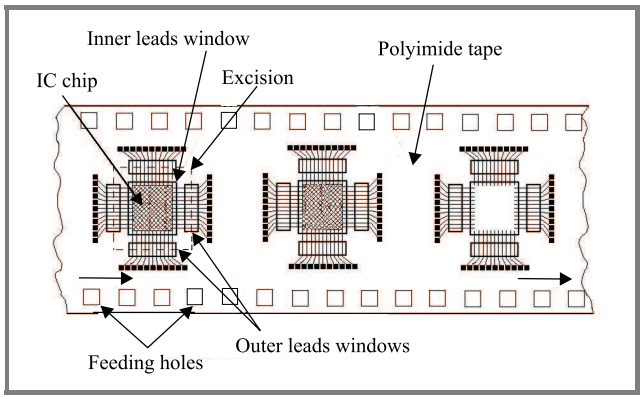

Fig. 3. The idea of TAB connection.

The width and spacing of the inner lead bonding pads of the TAB process used currently is 50 μm. The corresponding dimensions of the outer lead bonding pads are 100 μm if the substrate technology allows it. TAB offers advantages in the area of improved electrical and thermal performance. TAB process is also a very good choice for building reliable MCMs.

4. Wafer level packaging

The wafer level CSP is a packaging technology where the majority of the packaging process steps are carried out at the wafer level [3, 8]. It is the most interesting technology from the point of view of miniaturisation. These packages are made before the wafer is sawed, therefore their size cannot be larger than that of the die. Most packages of this type are made by re-routing the bond pads on the wafer, followed by bumping.

The limitation on wafer level packaging (WLP) is how many I/O can be placed under the chip. Typical application market for WLP is projected for ICs with total I/O below 100 and adequate silicon area. A key enabling technology to take full advantage of WLP is the development of wafer level test and burn-in. Most WLPs with I/O pitch equal or greater than 0.5 mm do not require the use of underfiller and can be directly implemented into a standard surface mount technology (SMT) process flow.

The reliability of WLP that use bond pad redistribution is a problem, especially when they are to be mounted on FR-4 boards. Due to different thermal expansion coefficients of silicon and printed board, the maximum die size is limited. So, the use of wafer level packages focuses on ICs with relatively low pin count (small size). Many portable equipment manufactures use underfilling. It improves resistance to solder fatigue and improves the resistance to mechanical stress, such as, shock, board wrapage and vibration. The reliability of WLP can also be improved when the stand-off between the component and the printed board is enlarged [11].

WLP technology is ideal for portable communications and related applications that require a low cost packaging solution with small form factor and improved signal propagation characteristic.

A disadvantage of WLP and flip chip is that their size is not standardized. The package has the same dimensions as the die, which can have any dimension. To avoid the need for customised test sockets, trays, reels, etc., it is best to perform as many operations as possible at the wafer level.

5. Types of IC array packages

5.1. BGA packages

The BGA package is based on a PCB substrate. The standard core thickness of substrate is typically from 0.2 to 0.4 mm with 18 μm copper on each side. The silicon chip is die bonded to the top side of the substrate using die attach adhesive. The chip is then gold wire-bonded to wire bond pads on the substrate. Traces from the wire bond pads take the signal to vias which carry them to the bottom side of the substrate and then to circular solder pads. The bottom side solder pads are laid out on square or rectangular grid with either a constant 1.5 mm, 1.27 or 1.0 mm pitch. An overmold is then performed to completely cover the chip, wires and substrate wire bond pads. Majority of BGAs will utilize a wire bond interconnection on the periphery of the IC (Fig. 1). Area array flip chip connections to BGAs are needed for high I/O counts or high power chips (Fig. 2). Laminate-based array packages will require the use of underfillers to reduce the shear stress load on the flip chip interconnections for large die, due to the large difference in the CTE between the silicon IC and the substrate. BGA packages will provide good solutions for the pincount range above 200.

5.2. CSP technology

Defined by a criterion of size, CSP are no smaller than 80% of the chips they house. For CSP, the pitch drops below 0.8 mm. CSPs normally contain an interposer on which the die is attached by either wire-bonding or flip chip interconnect [8]. A rewiring of the I/O pads is done on a flex interposer or directly on the wafer/die surface. The area distributed I/O contacts (solder ball height smaller

than 250 μm) for board assembly are satisfied by the PCB land pitches in size 250 μm to 500 μm. In case of wafer level redistribution the packaging cost can be reduced tremendously. CSP package with flexible interposer is shown in the Fig. 4. The relatively expensive underfilling process after assembling can be avoided because a stress compensation can be implemented into the "package".

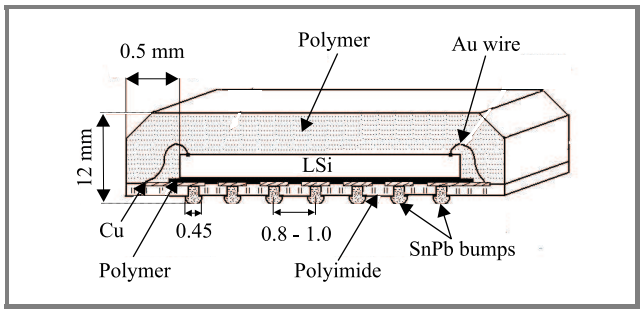

Fig. 4. Cross-section of CSP package.

The comparison of these two type of package is shown in Table 5. CSP packages will provide good solutions for the pincount range above 400. In CSP package the silicon-to-package area ratio is increased up to 100% in most versions. Having reduced the package body to equal the die size the next available step is the integration in the z-direction by stacking more dies in the same package [10].

Table 5
Development of BGA and CSP packages parameters in the next decade [3, 4]

Package/parameter	Year		
	2002	2006	2010
BGA – solder pitch [mm]	1.00	0.65	0.50
BGA – body size [mm]	23	18	17
– possible pincount	484	729	1089
CSP – area array pitch [mm]	0.40	0.30	0.30
CSP – body size 10 mm			
– possible pincount	320	540	540
CSP – body size 21 mm			
– possible pincount	572	1280	1280

The CSP packages provide a potential solution where low weight and small size are the requirements. These packages are only slightly larger than the chip itself, and are available in a variety of configurations and materials combinations. The size may range from 4 to 21 mm. Significant size reduction can only be realized by using CSP, which has pitches ranging from 0.4 mm to 0.3 mm. Four type of CSPs can be distinguished [8]:

– CSPs with rigid interposer (organic or ceramic),
– CSPs with a flexible interposer (usually polyimide),
– CSPs with a leadframe,
– wafer level CSPs.

The next level of wafer level packaging is reached by integration of passive (R, L) and active devices (Si, GaAs ICs). Such system are known as multi-chip modules (MCM).

5.3. MCM technology

The simplest definition of an MCM is that of a single package containing more than one IC. More precisely, in the MCM there are multiple bare dies mounted along with signal conditioning or support circuitry such as capacitors, resistors and other parts on a laminate or ceramic base material. MCMs introduce a packaging level between the application-specific IC (ASIC) and board level. Digital and analog functions can be mixed without serious limitations, and an ASIC can be composed easily with standard processors, devices and memories in one package. The next generation of MCMs could even have optical I/Os as an option. In such solution, high-speed components can be placed closer to each other, the load on the IC output buffers is lower and signal transmission properties are better. The new version of MCM is called system-in-package (SiP) where dies are mounted one on the other.
Multi-chip module technology has been previously used for high performance applications like mainframe CPU's. MCMs of this type are typically very complex and expensive. MCM-C applied in the IBM 4300 computer used a glass-ceramic substrate with more than 40 layers and containing more than 25 ICs [2].

5.4. SiP packages (multi-stacked LSI)

The term system-in-package is used to describe multi-chip IC, such as stacked die CSP or MCM-PBGAs. SiP is a functional block or module, which incorporates ICs, passive components, antennas, etc. Curent SiPs assemble 2–5 dies in a single package combining wire bond with peripheral or center pads, die-to-die- bonding, flip chip and SMT [12, 13]. SiP is used as a standard component in board level manufacturing (Fig. 5). It is based on a merger of mainstream, high volume and low cost IC assembly technology and surface mount technology. The IC assembly technology is used to interconnect the IC chips to the SiP substrate while the SMT technology is used to interconnect the IC chips to the SiP substrate while the SMT technology is used to connect passive components and other

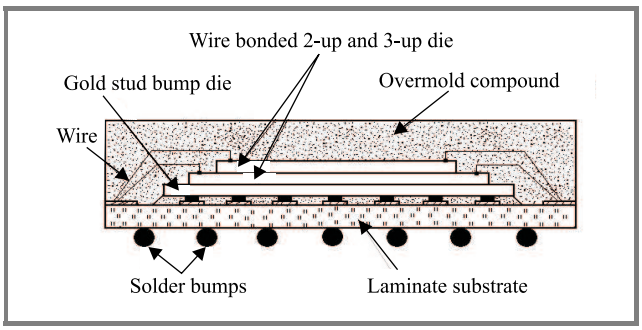

Fig. 5. Cross-section of SiP package.

SMT-compatible components (e.g., connectors) to the SiP substrate.
Current SiP solution is based on low cost IC assembly technology and surface mount technology. The SiP can be manufactured using ceramic, leadframe, organic laminate or even tape-based substrates. The following attributes are used to define SiPs:

- Includes chip-level interconnect technology. In other words, flip chip, wire bond, TAB or other interconnect directly to an IC chip.
- Quite often includes passive components. The passives may be either surface mounted discrete components or they may be embedded into or manufactured on the substrate material, as buried components.
- Typically includes more than one IC chip, so integration of various die technologies (e.g., Si, GaAs, SiGe, SOI, MEMS and optical) in the same package is possible.
- May include other components necessary to bring the SiP to more complete functional system or subsystem level – such as housings, lids, RF shields, connectors, antennas, batteries, etc.

The SiP thickness started at 1.4 mm for a 2-stack but has now been reduced to 1.2 mm for the 3-stack and already there is a demand for a 4-stack in the 1.4 mm package. The end applications continuously require thinner packages. Reduction in package thickness requires thinner substrate, thinner die and smaller solder balls with a shrinking pitch. The majority of common 2-L laminate substrates have been reduced to 0.21 mm and the copper/polyimide tape substrates today use 0.05 mm polyimide and ultimately will migrate to 0.025 mm. The thinnest die in high volume production today is 0.14 mm, but this will soon be reduced to 0.10 mm and ultimately to 0.05 mm.
The primary driver behind SiP is maximum functionality in the minimum footprint. Assembling multiple die side-by-side in one package reduces interconnect length and can increase electrical performance. Lower cost is the driver for most packaging. SiP cost is only fractionally higher than the single-die package cost because it utilizes only one substrate, the backend operations are the same and are assembled using the same infrastructure.
The need to mix ASIC or digital signal processor (DSP) chips with memory has pushed the development of a three-stack SiP with sequentially smaller die stack. Same-die-stack technologies all using the 1.4 mm thickness CSP family. Technically these options can be grouped into three SiP families.

- **SiP I**. Wire bonded die-up SiP assembles die with peripheral bond pads in 2-up or 3-up configurations in one or two stacks. Through the use of a thin flex tape-based interposer and thin backgrind wafer technology, the triple-chip stacked SiP still meets the 1.4 mm maximum thickness ceiling required for advanced handsets.
- **SiP II**. Wire bonded die-up and die-down SiP with peripheral and centre pads at the bottom. The most common application is with DRAM with center pads at the bottom. The wire bonding to the die is done through a slot in the substrate that is subsequently encapsulated before the remaining dice are assembled.
- **SiP III**. Flip chip and wire bond SiP with die-up configuration are shown in Fig. 5. The flip chip connection is the gold stud bump formed directly on the aluminium die pads using wire bond technology.

Though the majority of CSPs today use the 0.8 mm pitch with 0.48 mm ball diameter, higher pincount applications with smaller footprints are migrating to 0.5 mm pitch with 0.30 mm diameter ball.
SiP offers the flexibility of mixing analog and digital designs, each optimised separately for performance and cost, and also integrates technologies like CMOS and SiGe or GaAs that cannot be mixed in one die to produce a system-on-chip (SoC).
Integrating many ICs in a SiP format and using a high-density substrate can result in significant cost saving by reducing routing complexity and layer count in the motherboard. Also, SiP solution can save a significant amount of space on the motherboard, which will enable more functionality to be integrated in a system board. The SiP equates to be functional block of the system that can be standarized across a product family and dropped into a new system board design with minimal effort. The SiP solution usually results in system cost savings by reducing motherboard cost, reducing system size and simplifying system assembly and rework process.
Communication system uses SiP technology for RF and wireless devices, networking and computing, image sensors and memory applications such as flash cards. In today's systems, the ASIC and memory are packaged separately and mounted to the system board. Considerable cost, size and performance benefits can be realized by integrating the ASIC and memory devices into a system in package configuration. The ASIC device is mounted in a flip chip configuration along with memory devices mounted on the same substrate beside the ASIC. Decoupling capacitors and other passives can also be mounted to the substrate. Memory devices are packaged and tested in individual CSP packages before they are mounted to the substrate using a conventional SMT process. This eliminates the yield loss issues associated with traditional MCM designs. Since all routing between the ASIC and memory is done on the first or second layer of the substrate, signal integrity is optimised.

6. Conclusion

Packaging technology plays an important role in the realisation of a new generation of products. This requires

the development of new packaging technologies and materials. The estimation of packaging technologies can be done by an indicator the so called packaging efficiency. It is defined by the ratio of the silicon chip to the area of the package. The best level of efficiency for pheripheral packages, like QFP, can reach 50%; for area array package like BGA/CSP does not exceed 90% and for wafer scale or bare chip solutions can achieve 100% silicon efficiency. Through SiP technologies, 200% efficiency can be approached without having to tackle the more complex second level interconnect and reliability challenges associated with 0.5 mm and finer ball pitch.
Stacked chip interconnection in combination with ball grid array and chip scale package technology platforms are merging to create a new wave of 3D package integration.

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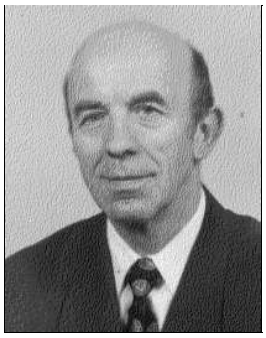

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