Paper

# DC and low-frequency noise analysis for buried SiGe channel metamorphic PMOSFETs with high Ge content

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**Abstract—Measurements of current drive in p-$Si_{1-x}Ge_x$ MOSFETs, with $x$ = 0.7, 0.8 reveal an enhancement ratio of over 2 times as compared to a Si device at an effective channel length of 0.55 $\mu$m. They also show a lower knee voltage in the output *I-V* characteristics while retaining similar values of drain induced barrier lowering, subthreshold swing, and off current for devices with a Sb punch-through stopper. For the first time, we have quantitatively explained the low-frequency noise reduction in metamorphic, high Ge content, SiGe PMOSFETs compared to Si PMOSFETs.**

***Keywords*— *SiGe, metamorphic MOSFET, LF-noise, I-V, C-V, effective hole mobility.***

## 1. Introduction

Strained-Si NMOS and PMOS devices have made remarkable strides in the last year or two and both IBM and Intel are developing full CMOS processes [1, 2]. On the other hand, while there is particular advantage [3] to be gained in increasing the performance of the p-channel current drive, enhancements in this case have been less than those in the area of n-channel. Sugii *et al*. [4], for example, find a current drive enhancement ratio in the n-channel of 1.7 compared to their Si control, but only 1.5 in the p-channel, which is of particular relevance to the current work. A strained $Si_{1-x}Ge_x$ layer capped with strained Si is an attractive alternative that offers higher effective hole mobility than strained silicon only [5] while being also compatible with a full N/P CMOS configuration. In this work we report on PMOSFET devices containing strained $Si_{1-x}Ge_x$ channel with $x = 0.7$, 0.8 and the effective channel length of 0.55 $\mu$m. The devices have the maximum effective hole mobilities in the range of 760–500 cm$^2$/Vs at a vertical effective fields $E_{eff} = 0.08-0.2$ MV/cm, compared to 170–130 cm$^2$/Vs in bulk Si and 110 cm$^2$/Vs in our epitaxial Si control. This leads to a current drive enhancement ratio of a factor of more than two whilst maintaining short channel characteristics similar to those of the Si control. The drain current is sub-linear in gate overdrive, implying advantageous high lateral field transport.

The reduction of low-frequency (LF) noise is crucial for achieving high performance in analogue Si-based MOSFET devices [12]. One solution to this problem is via the incorporation of strained SiGe buried layers. Recently there have been several contradictory reports concerning the LF-noise properties of SiGe pseudomorphic FET devices [13–16]. The authors of [14,16] reported, for example, a decrease of the normalised drain current noise power spectral density (NPSD) of pseudomorphic SiGe MOSFETs in comparison with Si controls, others reported an increase of NPSD [12, 13]. LF-noise characteristics and mechanisms of LF-noise reduction in buried channel p-SiGe metamorphic MOSFETs are described.

## 2. MOSFET fabrication

The MOSFETs fabricated on multilayer SiGe heterostructures grown by two epitaxial techniques are compared. The first structure (Fig. 1) has a $Si_{0.3}Ge_{0.7}$ p-channel and was

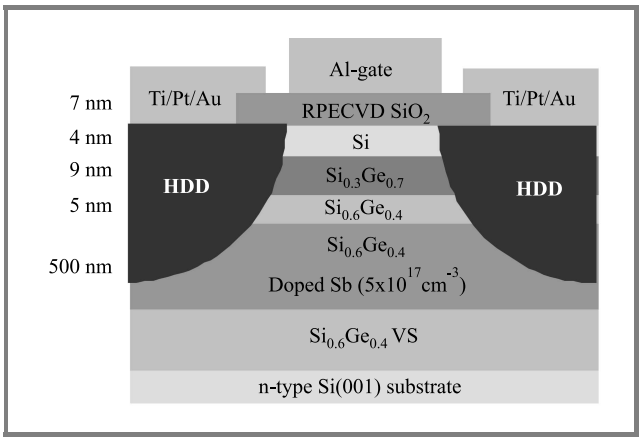


***Fig. 1.*** Schematic cross-section of p-$Si_{0.3}Ge_{0.7}$ MOSFET.

grown by solid-source molecular beam epitaxy (SS-MBE) on an n-type ($1 \cdot 10^{15}$ cm$^{-3}$) Si(001) wafer. It consist of a 2.5 $\mu$m relaxed $Si_{1-y}Ge_y$ virtual substrate (VS) linearly graded to the final Ge composition $y = 0.4$, 500 nm of $Si_{0.6}Ge_{0.4}$:Sb doped at $5 \cdot 10^{17}$ cm$^{-3}$ acting as a "punch-through stopper" to avoid short channel effects, a 5 nm $Si_{0.6}Ge_{0.4}$ spacer layer, a 9 nm compressively strained $Si_{0.3}Ge_{0.7}$ channel, and 4 nm tensile-strained Si cap layer.

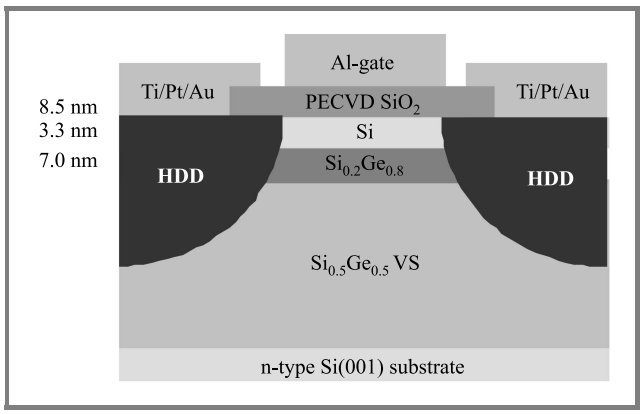


***Fig. 2.*** Schematic cross-section of p-$Si_{0.2}Ge_{0.8}$ MOSFET.

The second structure (Fig. 2) was grown by low energy plasma enhanced CVD (LEPECVD) and differs in that the VS terminates at $y = 0.5$, there is no punch through stopper and the p-channel is 7 nm of strained $Si_{0.2}Ge_{0.8}$. As $x - y = 0.3$ in both structures the strain in the p-channel will be the same. The PMOSFET devices were fabricated using reduced thermal budget processing at 650°C, to minimize Ge out-diffusion from the strained $Si_{1-x}Ge_x$ channel [7] and to avoid Sb penetration to the channel, with 200 nm of plasma enhanced CVD (PECVD) $SiO_2$ deposited as a field oxide. In the active transistor area the field oxide was removed by wet chemical etching. After a cleaning step the gate oxide on the first SS-MBE grown structure was deposited by remote plasma enhanced CVD (RPECVD) as a 7 nm $SiO_2$ layer at 300°C [18]. The gate oxide on the second LEPECVD grown structure was 8.5 nm PECVD deposited at 370°C, followed by annealing in a $N_2O$ atmosphere at 650°C for 1 min. Source and drain contacts were fabricated by $BF_2^+$ implantation at 40 keV, with a dose of $4 \cdot 10^{15}$ cm$^{-2}$ and activated at 650°C for 30 s. The surface of contact areas was etched for a short time to remove impurities increasing contact resistance. Finally, the Al gate and Ti/Pt/Au contact metallization were evaporated. The second p-$Si_{0.2}Ge_{0.8}$(2) device of Table 1 was made using the same process as for MBE-grown p-$Si_{0.3}Ge_{0.7}$ device [5], but the thickness of the $SiO_2$ layer is 11 nm.
The p-Si MOSFET devices were fabricated on SS-MBE grown 100 nm Si epilayer, grown on n-type ($1 \cdot 10^{17}$ cm$^{-3}$) Si(001) wafers using a self-aligned gate process, with 9 nm dry $SiO_2$ thermally grown at 800°C for 120 min and 300 nm p-type ($5 \cdot 10^{19}$ cm$^{-3}$) poly-Si gate. The row of geometrical gate lengths for all fabricated transistors was in the range $L = 0.4 - 50$ $\mu$m with the same gate width $W = 50$ $\mu$m.

Table 1
Electrical and structural properties of 0.55 $\mu$m p-$Si_{0.3}Ge_{0.7}$, p-$Si_{0.2}Ge_{0.8}$ and p-Si MOSFETs

| Parameter | Si | $Si_{0.3}Ge_{0.7}$ | $Si_{0.2}Ge_{0.8}$ | $Si_{0.2}Ge_{0.8}$ (2) |
|---|---|---|---|---|
| $SiO_2$ thickness [nm] | 9 | 7 | 8.5 | 11 |
| $g_{m\,(sat)}$ [mS/mm] | 40 | 84 | 95 | 63 |
| $S$ [mV/decade] | 85 | 95 | 130 | 200 |
| $V_{TH}$ [V] | –0.2 | –0.84 | –0.26 | –0.95 |
| $I_{ON}/I_{OFF}$ [$V_{DS} = -50$ mV] | $10^6$ | $10^6$ | $2.5 \cdot 10^3$ | $2.5 \cdot 10^3$ |
| $I_{ON}/I_{OFF}$ [$V_{DS} = -3$ V] | $10^4$ | $10^4$ | 15 | 26 |

## 3. DC characteristics

Current-voltage (*I-V*) and quasistatic capacitance-voltage (*C-V*) characteristics were measured using an Agilent 4156C parameter analyzer for all devices at a temperature of 293 K (the basic parameters are given in Table 1). The input *I-V* characteristics for the $Si_{0.3}Ge_{0.7}$ PMOSFET in Fig. 3 show reduced drain induced barrier lowering (DIBL)

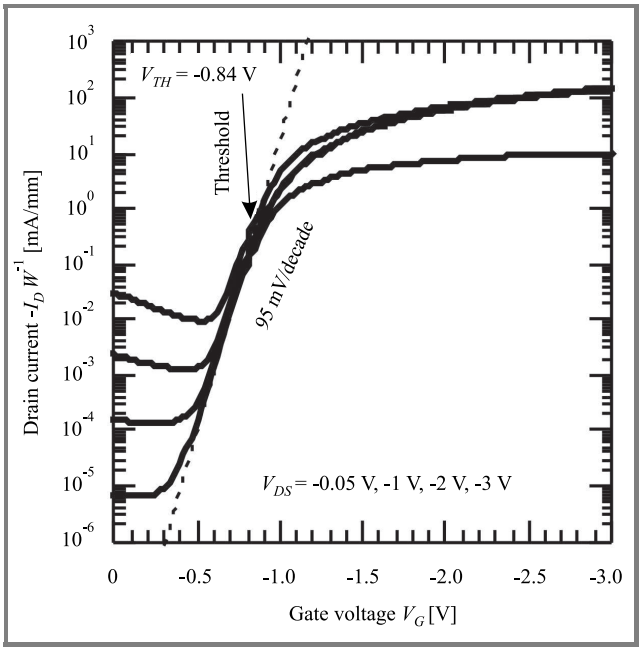


***Fig. 3.*** Input *I-V* characteristics for p-$Si_{0.3}Ge_{0.7}$ MOSFET with $L_{eff} = 0.55$ $\mu$m.

and an excellent subthreshold swing $S = 95$ mV/decade at $V_{DS} = -50$ mV, which demonstrates the efficiency of the "punch-through stopper" for sub-micron MOSFET operation. This device has an excellent $I_{ON}/I_{OFF}$ ratio of $10^6$ in the linear region ($V_{DS} = -50$ mV) and in saturation ($V_{DS} = -3$ V) $I_{ON}/I_{OFF} \approx 10^4$. The threshold voltage $V_{TH}$ is -0.84 V at $V_{DS} = -50$ mV.
The input *I-V* characteristics for the p-Si MOSFET are shown in Fig. 4. In this case, the subthreshold swing is 85 mV/decade and $I_{ON}/I_{OFF}$ is $10^6$ in the linear region and $10^4$ in saturation. The threshold voltage $V_{TH}$ is –0.2 V. Comparison of these two devices shows the metamorphic MOSFET is operating in an acceptable way and provides a competitive device at this technology node. The slight increase in $S$ in the p-$Si_{0.3}Ge_{0.7}$ device can be completely accounted for by the added capacitance of the strained Si overlayer.
The electrical characteristics of the p-$Si_{0.2}Ge_{0.8}$ MOSFET, which does not have a punch through stopper, are

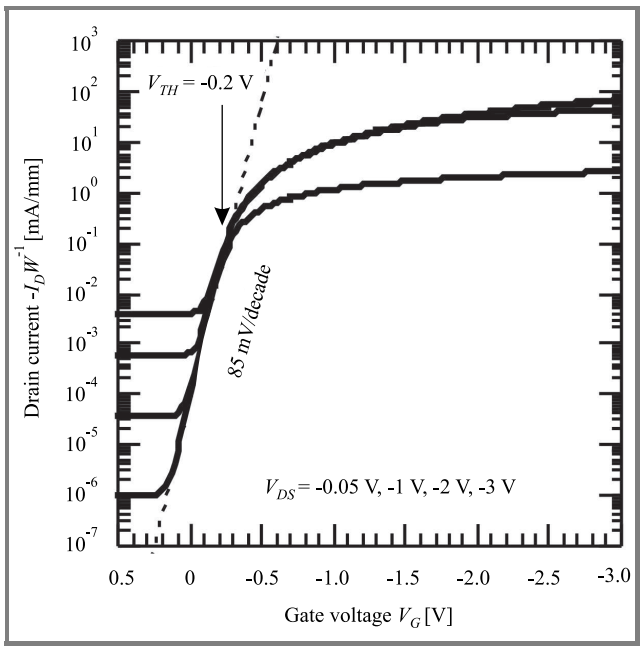


***Fig. 4.*** Input *I-V* characteristics for p-Si MOSFET with $L_{eff} = 0.55$ $\mu$m.

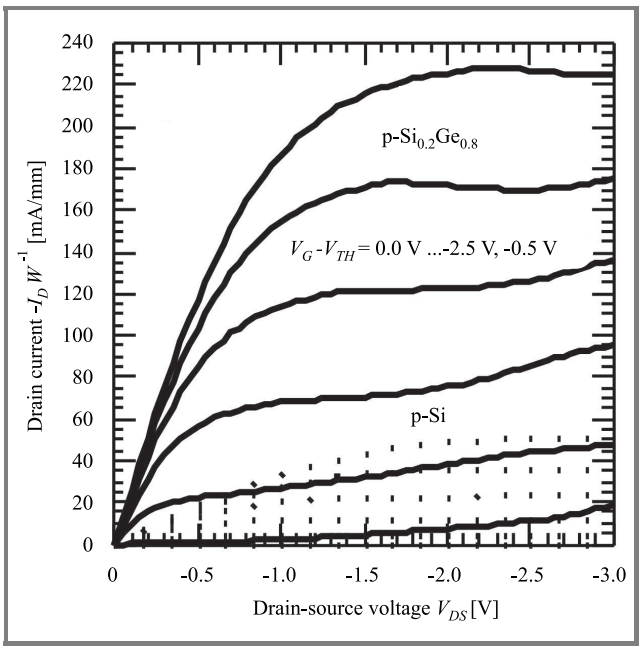


***Fig. 6.*** Output *I-V* characteristics of p-Si and p-Si$_{0.2}$Ge$_{0.8}$ MOSFET with $L_{eff} = 0.55$ $\mu$m at the same $V_G$–$V_{TH}$.

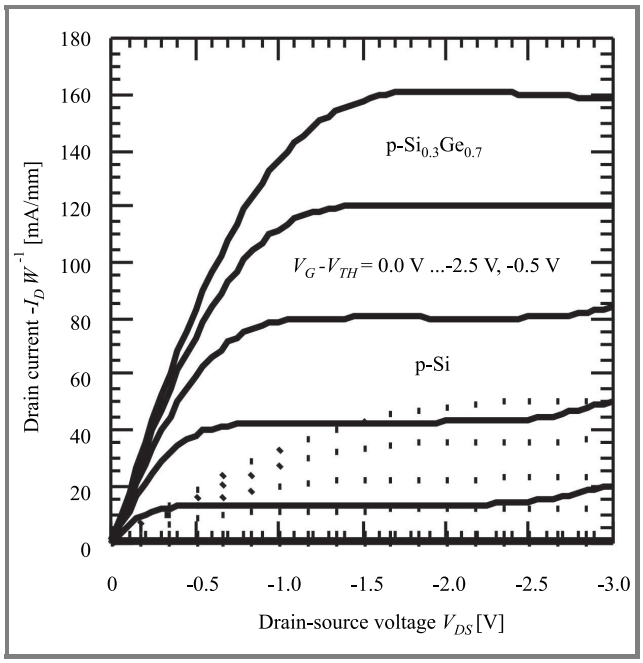


***Fig. 5.*** Output *I-V* characteristics of p-Si and p-Si$_{0.3}$Ge$_{0.7}$ MOSFET with $L_{eff} = 0.55$ $\mu$m at the same $V_G$–$V_{TH}$.

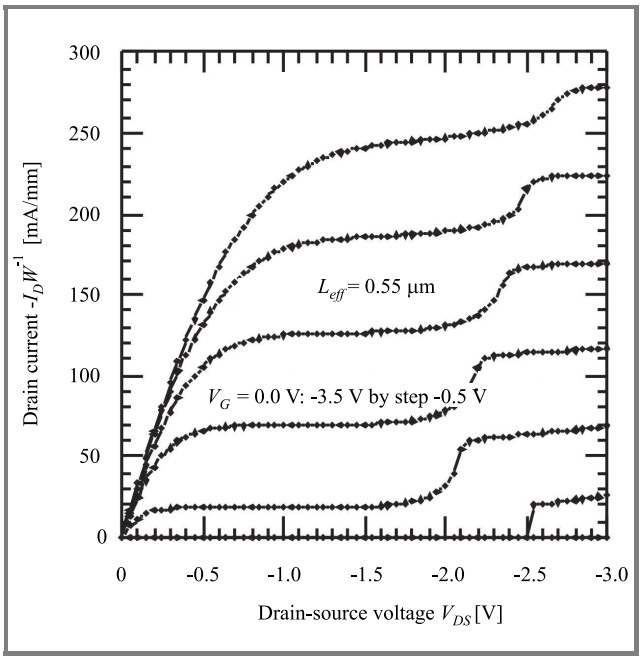


***Fig. 7.*** Kink effect on output *I-V* characteristics of p-Si$_{0.3}$Ge$_{0.7}$ at low temperatures $T = 77$ K.

not as impressive. The subthreshold slope is increased to 130 mV/decade and the device does not switch off well resulting in a much reduced $I_{ON}/I_{OFF}$ ratio. This is a consequence of the vertical architecture not being optimised for sub-micron device operation rather than any inherent problem with the channel material, as will be seen in the mobility measurements and output characteristics below.

The maximum transconductance in the saturation region is $g_m = 84$ and 95 mS/mm respectively compared to 40 mS/mm in the Si control. The maximum drain current at $V_G - V_{TH} = -2.5$ V is 165 mA/mm for p-Si$_{0.3}$Ge$_{0.7}$ and 230 mA/mm for p-Si$_{0.2}$Ge$_{0.8}$.

The output *I-V* characteristics measured on both the p-Si$_{0.3}$Ge$_{0.7}$ and p-Si$_{0.2}$Ge$_{0.8}$ MOSFETs are shown in Fig. 5 and Fig. 6, with comparisons to the p-Si device. Enhance-

ment in the saturated drain current by a factor of 2.5–3 is clearly visible in the output *I-V* characteristics of the $Si_{0.3}Ge_{0.7}$ PMOSFET (Fig. 5) at $V_{DS} = -2.5$ V, in comparison with the silicon control. Similar enhancement is seen at all values of drain bias. For the $Si_{0.2}Ge_{0.8}$ PMOSFET the enhancement factor in the normalised saturation drain current is actually higher than for the $Si_{0.3}Ge_{0.7}$ PMOSFET and is more than a factor of three above the control.

The *I-V* characteristics of the p-$Si_{0.2}Ge_{0.8}$(2) MOSFET are similar to those of p-$Si_{0.2}Ge_{0.8}$ MOSFET and differ only in slightly lower drain current values due to thicker gate dielectric.

The self-heating effect, which is responsible for the mobility degradation, threshold voltage lowering and negative differential conductance, was observed in all high Ge content metamorphic SiGe MOSFETs with gate length below 2 $\mu$m at high $V_{DS}$. The "kink" effect (Fig. 7) was clearly observed at low temperature (77 K) for devices with a punch-through stopper (p-$Si_{0.3}Ge_{0.7}$). This is due to the majority carriers generated by impact ionization that are collected in the body and increase the body potential (lower threshold voltage). For devices without a punch-through stopper (p-$Si_{0.2}Ge_{0.8}$) the "kink" effect was not observed. This behavior of our devices is similar to partially depleted silicon-on-insulator (SOI) MOSFETs [10].

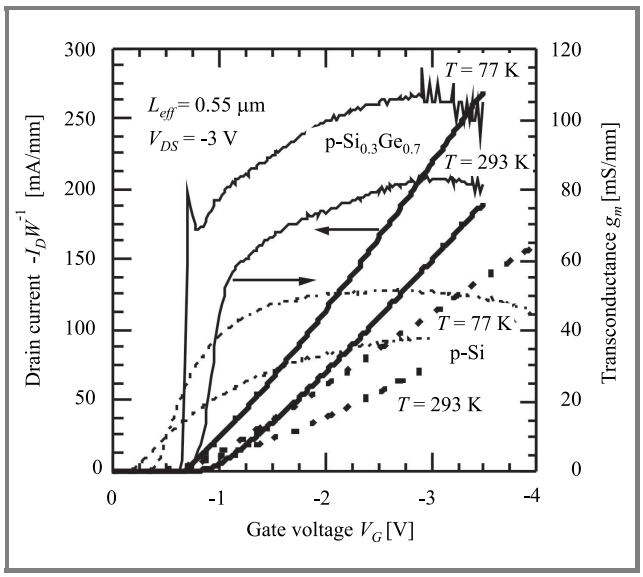


***Fig. 8.*** Drain current $I_D$ (thick lines) and transconductance $g_m$ (thin lines) versus gate voltage for p-$Si_{0.3}Ge_{0.7}$ (solid lines) and p-Si (dashed lines) MOSFETs with effective gate length 0.55 $\mu$m at room ($T = 293$ K) and nitrogen ($T = 77$ K) temperatures.

The low temperature measurements have been carried out in liquid nitrogen ($T = 77$ K). The input *I-V* characteristics for the p-$Si_{0.3}Ge_{0.7}$ MOSFET at $T = 77$ K in comparison with the characteristics obtained at room temperature $T = 293$ K are shown in Fig. 8. The threshold voltage $V_{TH}$ increases slightly with the temperature decreasing to 77 K. The maximum transconductance $g_m$ and maximum drain current $I_D$ in the linear regime increased 2.8 and 1.6 times, respectively, at 77 K when compared to the corresponding values measured at 293 K. The maximum transconductance $g_m$ and maximum drain current $I_D$ in saturation increased 1.4 and 1.3 times, respectively, at 77 K when compared to the respective values measured at 293 K.

The *C-V* characteristics were measured on devices with gate length $L = 50$ $\mu$m and gate width $W = 50$ $\mu$m. The p-$Si_{0.2}Ge_{0.8}$(2) MOSFETs with gate oxide thickness of 11 nm operate at the gate voltage range $-6\text{ V} \le V_G \le 6\text{ V}$ before breakdown. Figure 9 clearly shows that the Si cap starts to fill with carriers only at a gate overdrive voltage of 3.5 V. Very small changes in *C-V* curves measured at 77 K and at 293 K indicate low level of impurities in the heterostructure and low concentration of mobile charge inside the gate dielectric.

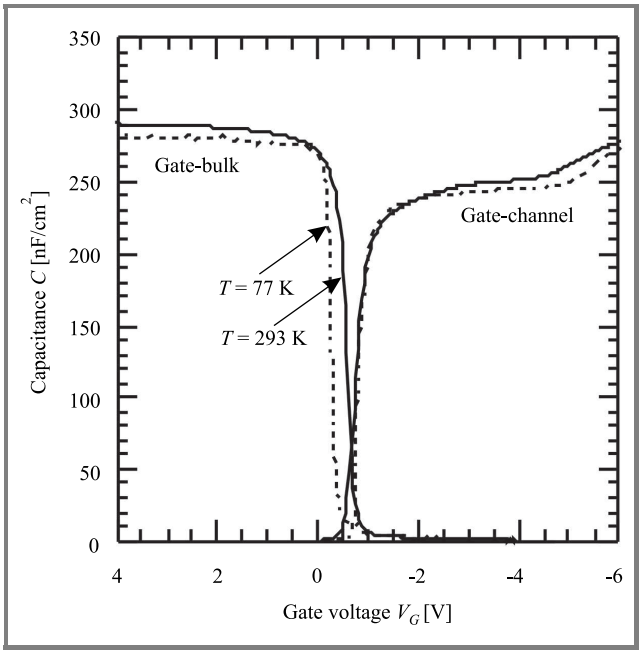


***Fig. 9.*** High frequency split *C-V* characteristics for MOSFET p-$Si_{0.2}Ge_{0.8}$(2) with effective gate length 50 $\mu$m at room temperature 293 K (solid lines) and at liquid nitrogen temperature 77 K (dashed lines).

The *C-V* characteristics for p-$Si_{0.3}Ge_{0.7}$ MOSFETs with $SiO_2$ thickness of 7 nm (Fig. 10) show that the Si cap is not filled up to 2 V gate overdrive voltage. The oxide breakdown limit for p-$Si_{0.3}Ge_{0.7}$ devices is around 4 V.

The depletion charge was extracted from quasistatic and high frequency *C-V* characteristics [11]. Figure 11 shows increasing of the depletion charge for p-$Si_{0.3}Ge_{0.7}$ heterostructure from the depth of 25 nm. The value of the depletion charge is $\sim 3 \cdot 10^{17}$ cm$^{-3}$ at maximum. It corresponded to the n-type doped SiGe buffer layer of 15 nm thickness that lays 5 nm beneath the channel. The depletion charge curve is broken abruptly at the depth of 40 nm, which points to a limitation of the depletion approximation. The depletion regime is changed to the inversion regime (holes accumulation) at this depth. No peculiarity was observed on the depletion charge curves for

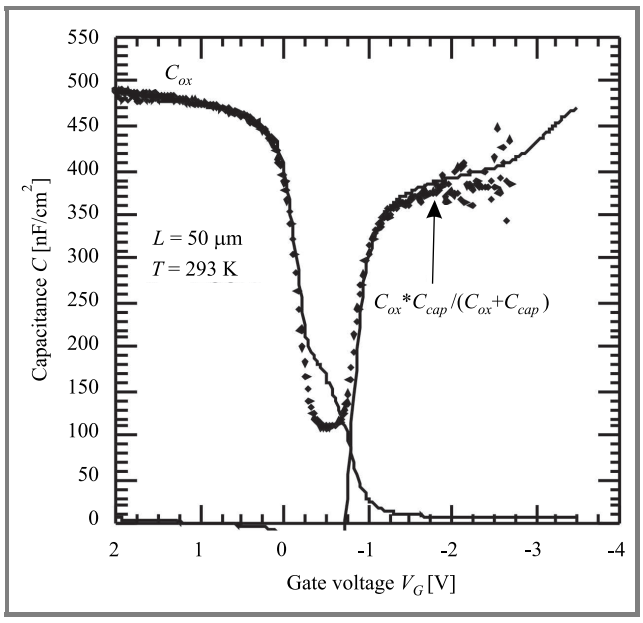


***Fig. 10.*** High frequency (solid line) and quasistatic (dots) *C-V* characteristics for MOSFET p-$Si_{0.3}Ge_{0.7}$ with effective gate length 50 $\mu$m at room temperature.

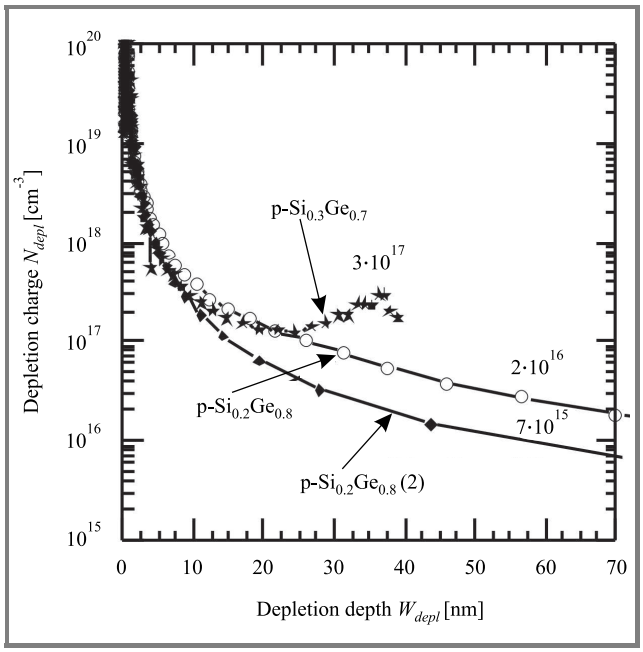


***Fig. 11.*** Depletion charge profiles extracted from quasistatic and high frequency *C-V* characteristics for p-$Si_{0.3}Ge_{0.7}$, p-$Si_{0.2}Ge_{0.8}$, and p-$Si_{0.2}Ge_{0.8}$(2) heterostructures.

p-$Si_{0.2}Ge_{0.8}$ and p-$Si_{0.2}Ge_{0.8}$(2) MOSFETs. This indicates that the under-channel area of these samples was not doped or was doped with background donor concentration less than $1\cdot10^{16}$ cm$^{-3}$. Also Fig. 11 shows lower impurity background of the p-$Si_{0.2}Ge_{0.8}$(2) heterostructure when compared to the p-$Si_{0.2}Ge_{0.8}$ heterostructure.

The effective mobility $\mu_{eff}$ (Fig. 12) has been determined as a function of $E_{eff}$ on large area MOSFETs (gate width $W$ and length $L$ both equal to 50 $\mu$m), from the input *I-V* at low $V_{DS} = -50$ mV and from quasistatic and high frequency split *C-V* characteristics [11]. 1D Poisson-Schrodinger simulation was used to obtain correct sheet densities inside the structure and recheck the parameters extracted from the depletion approximation by fitting the measured *C-V* data.

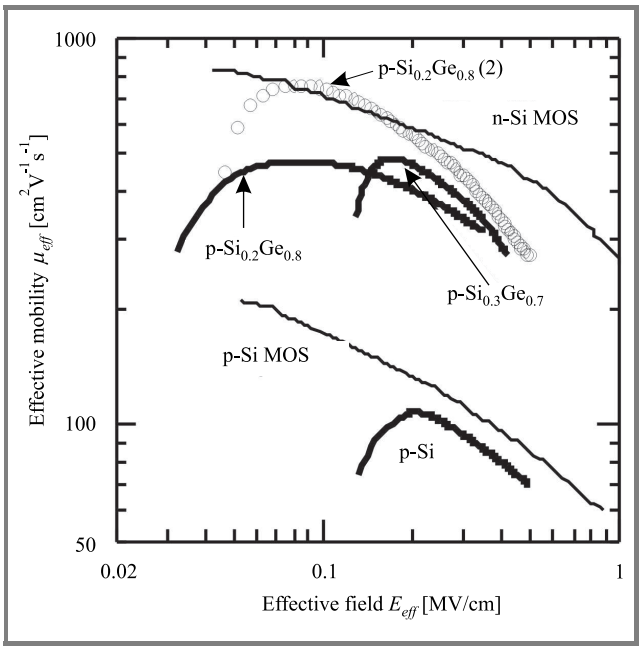


***Fig. 12.*** Effective mobility as a function of effective field for p-$Si_{0.3}Ge_{0.7}$, p-$Si_{0.2}Ge_{0.8}$, p-$Si_{0.2}Ge_{0.8}$(2) and p-Si MOSFETs, as well as universal curves for p-Si MOS and n-Si MOS after S. Takagi [9].

The p-$Si_{0.2}Ge_{0.8}$(2) heterostructure has the highest mobility 760 cm$^2$V$^{-1}$s$^{-1}$ at the field $E_{eff} = 0.08$ MV/cm due to the lowest background of ionized impurities. On the other hand, p-$Si_{0.2}Ge_{0.8}$(2) MOSFETs have the worst subthreshold slope, that could be explained by MOSFET short channel effects due to the absence of n-type "punch through" stopper (ionized impurities) underneath of p-$Si_{0.2}Ge_{0.8}$ channel.

## 4. Low-frequency noise

Conventional MOSFET characterisation techniques, such as the combination of *I-V* (current-voltage) and *C-V* (capacitance-voltage) measurements, are very problematic as device size decreases down to the deep sub-$\mu$m (DS-$\mu$m) scale. "Average per square" characteristic parameters obtained from large-scale devices cannot be suitable for DS-$\mu$m MOSFET analysis due to statistical uncertainty of fabrication technology together with the importance of mesoscopic quantum effects. Low-frequency noise measurements could be a powerful diagnostic technique for DS-$\mu$m MOSFET characterization in a wide range of device operation regimes [17]. Unfortunately, the commercially available current preamplifiers such as ITHACO-1211, SR-570, EG&G-181 have been optimised only for limited ranges

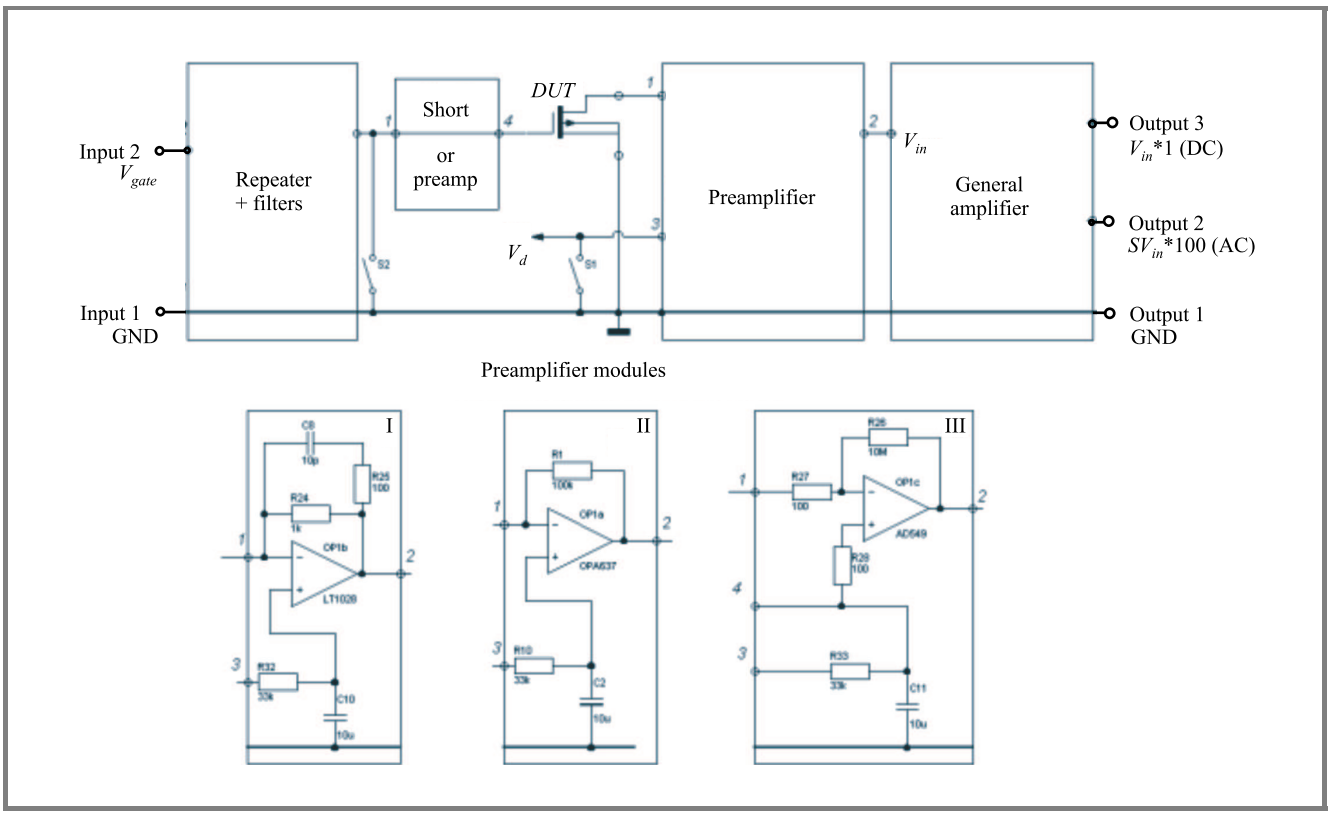


***Fig. 13.*** Schematic of the current preamplifier with modular design and interchangeable first stage for LF-noise measurements.

of device input impedance and their conventional "all-in-one" desktop design also introduces extra problems when long cables are used to connect the equipment to the sample test fixture. To overcome all the above problems we have used the optimised preamplifier modules as the first stages for gate leakage and drain current noise measurements of MOSFETs with input impedance 50 Ω–$10^8$ Ω in the frequency range of 1.0 Hz–$10^5$ Hz. A three-box modular design with interchangeable first stage preamplifiers (Fig. 13) was chosen to improve the reliability and to reduce the influence of the connection cables on measurement results. The best operational amplifiers (OAMPs) currently available with optimal voltage $v_n$ and current $i_n$ noise, AD549 ($v_n = 200$ nV Hz$^{-1/2}$, $i_n = 0.15$ fAHz$^{-1/2}$), OPA637 ($v_n = 3.7$ nVHz$^{-1/2}$, $i_n = 2.0$ fAHz$^{-1/2}$) and LT1028A ($v_n = 0.85$ nVHz$^{-1/2}$, $i_n = 1.0$ pAHz$^{-1/2}$) were used for the first stage module at each of the three chosen impedance ranges.

The LF-noise was measured using an HP 35670A dynamic signal analyzer and the custom-made preamplifier described above. Characteristics *I-V* and LF-noise were measured simultaneously to account for possible offset of the applied gate voltage $V_G$. All measurements were done on MOSFETs with a geometrical gate length of 1.0 $\mu$m (an effective gate length was extracted as 0.55 $\mu$m) and 10 $\mu$m in an electrically shielded room at 293 K. The SiGe MOSFETs show enhancement in the drain current and transconductance at the same gate overdrive voltages in comparison with p-Si devices. LF-noise has been measured in the linear regime of the output *I-V* characteristics ($V_{DS} = -50$ mV), from the sub-threshold through weak to strong inversion ($V_G - V_{TH}$ from 0.5 to −3 V) of the input *I-V*, in a wide range of drain-source conductance $g_d = I_D/V_{DS}$.

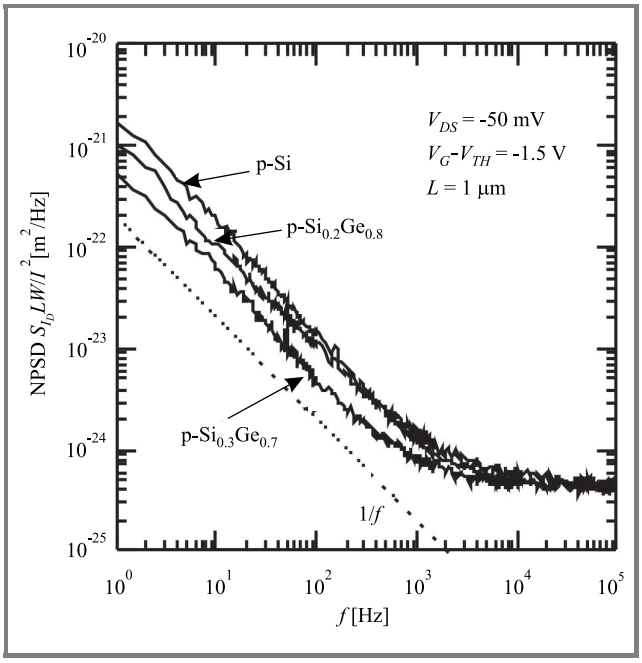


***Fig. 14.*** Normalized power spectral density of drain current fluctuations as a function of frequency for p-$Si_{0.3}Ge_{0.7}$ , p-$Si_{0.2}Ge_{0.8}$ and p-Si MOSFETs.

A typical normalized power spectral density (NPSD) $S_I/I^2$ of drain current fluctuations versus frequency in the range 1–$10^5$ Hz is presented in Fig. 14. Flicker, $1/f$ component, at low frequencies and thermal noise at high frequency range, dominate the spectra. In Fig. 14 the $1/f$ noise for the p-$Si_{0.3}Ge0.7$ MOSFET is clearly seen to be over three times lower than that for Si. We have not observed a generation-recombination (GR) noise component at any gate overdrive voltage. This is usually manifested as bumps in the spectra. GR noise could appear in the spectra due to Sb diffusion into the $Si_{0.3}Ge_{0.7}$ channel from the Sb-doped "punch-through" stopper or the existence of deep levels in the heterostructure. Thus we can confirm the absence of these defects and contaminations after the full MOSFET fabrication process.

The NPSD $S_{I_D}$ in the $1/f$ region is described in terms of carrier number fluctuations (CNF), correlated mobility fluctuations (CMF) and source-drain series resistance fluctuations (SDRF) [17]:

$$S_{I_D}/I_D^2 = \left(1+\alpha\mu_{eff}CI_D/g_m\right)^2\left(\frac{g_m}{I_D}\right)^2 S_{V_{fb}} + \left(\frac{I_D}{V_{DS}}\right)^2 S_{R_{SD}}, \tag{1}$$

where $\alpha$ is the Coulomb scattering coefficient, $\mu_{eff}$ is the effective mobility, $S_{V_{fb}} = S_{Q_{it}}/(WLC^2)$ with $S_{Q_{it}}$ being the interface charge spectral density per unit area, $C$ is the gate oxide capacitance $C_{ox}$.

The flat band voltage spectral density is defined by [17]:

$$S_{V_{fb}} = \frac{Q^2 k_B T N_{st}}{WLC_{ox}^2 f^\gamma} = \frac{q^2 k_B T \lambda N_t}{WLC_{ox}^2 f^\gamma}, \tag{2}$$

where $f$ is the frequency, $\gamma$ is the characteristic exponent close to unity, $k_BT$ is the thermal energy, $N_{st}$ is the density of traps near the $Si/SiO_2$ and/or Si/SiGe interface, $\lambda$ is the tunnel attenuation distance to Si cap and/or $SiO_2$, and $N_t$ is the volumetric trap density in the Si cap and/or $SiO_2$. The spectral density of the source-drain series resistance we defined by:

$$S_{R_{SD}} = \alpha_{H\_SD}\frac{R_{SD}^2}{fN_{SD}} \sim \frac{R_{SD}^3}{f}, \tag{3}$$

where $\alpha_{H\_SD}$ is the Hooge parameter for $1/f$ noise in the series resistance, $N_{SD}$ is the total number of free carriers and $R_{SD}$ is the source-drain series resistance.

The CMF can be important in both the weak and strong inversion regions of MOSFET operation. Typically, SDRF can appear at the highest gate voltages for the shortest channel lengths, when the channel resistance becomes comparable to the source-drain series resistance.

Figure 15 shows how measured and calculated power spectral density (PSD) varies with device conductance for the p-Si MOSFET. This curve was very well fitted by CNF, CMF and SDRF using Eq. (1). The Coulomb scattering coefficient $\alpha = 8\cdot10^4$ Vs/C extracted from the fitting of the experimental data for p-Si MOSFET is close to the predicted value of $10^5$ Vs/C for holes [17]. It is comparable to $\alpha^{PM\ \mathrm{Si\ cap}}$ for the Si cap of pseudomorphic p-SiGe devices and much higher than that for SiGe channels of the same pseudomorphic p-SiGe MOSFETs $\alpha^{PM\ \mathrm{SiGe}} = \sim 0.1\,\alpha^{PM\ \mathrm{Si\ cap}}$ [12].

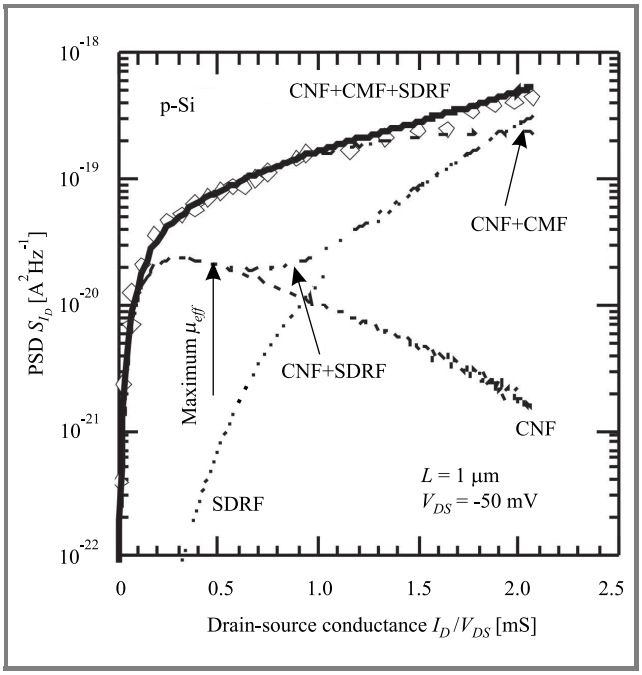


***Fig. 15.*** Power spectral density dependence on device conductance for p-Si MOSFET.

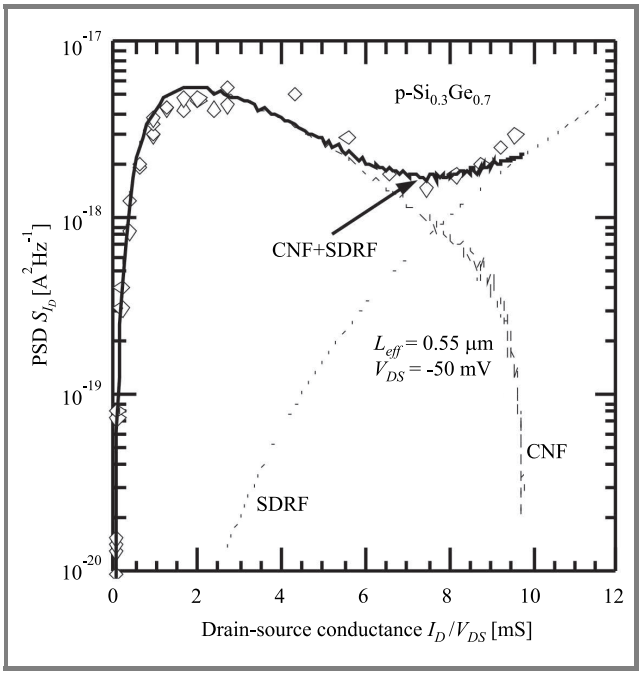


***Fig. 16.*** Power spectral density dependence on device conductance for p-$Si_{0.3}Ge_{0.7}$ MOSFET.

Figures 16 and 17 show the variation of PSD with device conductance for the p-$Si_{0.3}Ge_{0.7}$ and p-$Si_{0.2}Ge_{0.8}$ MOSFETs, respectively.

The variation is explained completely by CNF and SDRF, which reduce Eq. (1) for the NPSD to:

$$S_{I_D}/I_D^2 = \left(\frac{g_m}{I_D}\right)^2 S_{V_{fb}} + \left(\frac{I_D}{V_{DS}}\right)^2 S_{R_{SD}}\,. \qquad (4)$$

In the case of our metamorphic p-SiGe MOSFETs the CMF component was not observed ($\alpha << 5\cdot 10^2$ Vs/C) due to the presence of a thin Si cap layer (4–5 nm) between the SiGe channel and the Si-$SiO_2$ interface. The CMF component is more important as carriers locate closer to the $SiO_2$/Si interface. Thus, the signal to noise ratio in conventional MOSFET structure could be significantly improved in the case of heavily doped substrates or introduced punch-through stopper doping if SiGe buried channel heterostructures are used.

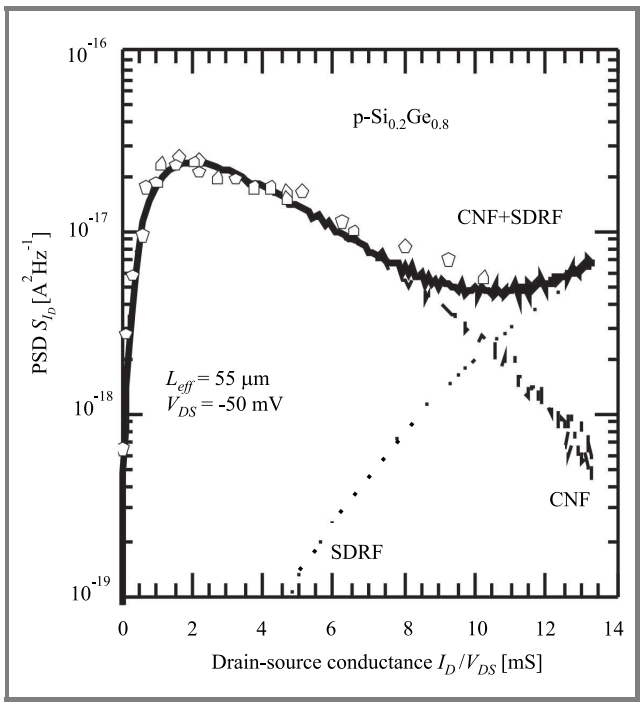


***Fig. 17.*** Power spectral density dependence on device conductance for p-$Si_{0.2}Ge_{0.8}$ MOSFET.

The SDRF component dominated in strong inversion for all the measured devices, and its value is 10–100 times lower in metamorphic p-SiGe MOSFETs than in p-Si due to their lower source-drain access resistance. Contact resistance estimated from the SDRF component decreased with Ge content increasing (Table 2).

Source-drain resistance $R_{SD}$ (noise) was calculated using equation (3) with suggestion that shape of contact areas ($L_{SD}$ – effective length of contacts area) is the same or very similar, and the values of Hooge parameter multiplied to mobility of carriers in contact area $\alpha_{H\_SD} \times \mu_{SD}$ are similar. This product also known as "noise reduced mobility" can be used as quality factor of the material in contact area [20]. The $R_{SD}$ (*I-V*) was obtained as a cross-over point of the lines drawn through points $R(V_G)$ for devices with different gate lengths $L$ at several fixed gate voltages $V_G$ (Terada-Muta method) [19].

Table 2
Source-drain resistance $R_{SD}$ extracted from *I-V* and $R_{SD}$ estimated from LF-noise results

| Sample | $S_{R_{SD}}$ [$\Omega^2$Hz$^{-1}$] | $R_{SD}/R_0$ | $R_{SD}$ (noise) [$\Omega\mu$m] | $R_{SD}$ (*I-V*) [$\Omega\mu$m] |
|---|---|---|---|---|
| p-$Si_{0.3}Ge_{0.7}$ | $1.2\cdot 10^{-7}$ | 1.00 | 2025* | 2025 |
| p-$Si_{0.2}Ge_{0.8}$ | $8.0\cdot 10^{-8}$ | 0.87 | 1769 | 2300 |
| p-Si | $7.0\cdot 10^{-6}$ | 3.88 | 7854 | 4680 |

* Resistance of 2025 $\Omega\mu$m of the sample p-$Si_{0.3}Ge_{0.7}$ measured using the Terada-Muta method [19] was used as a reference to estimate the resistance from LF-noise measurements.

The $R_{SD}$ extraction procedure from LF-noise requires just one device to be measured and one reference device. The results estimated from LF-noise are applied to the individual measured devices as opposed to the set of devices needed in the Terada-Muta method.

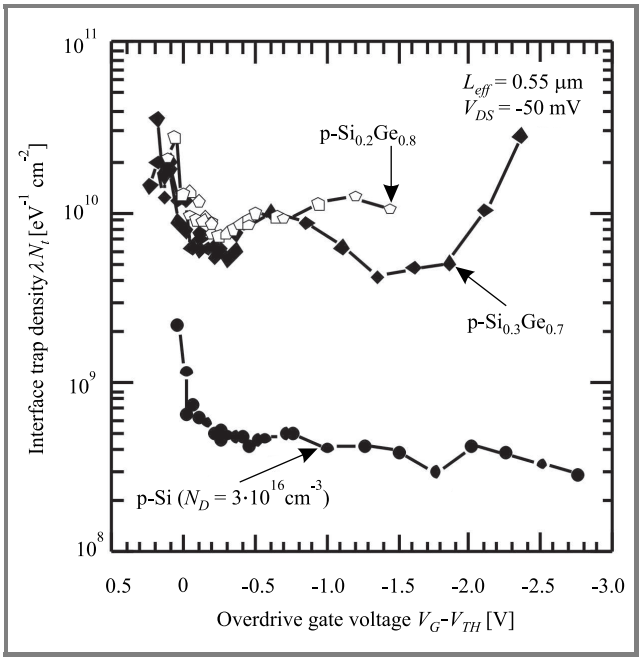


***Fig. 18.*** Interface trap density extracted from fitting of the data supplied by LF-noise measurements versus gate overdrive voltage for p-$Si_{0.3}Ge_{0.7}$, p-$Si_{0.5}Ge_{0.8}$ and p-Si heterostructures at room ($T = 293$ K) temperature.

The average densities of traps $\lambda N_t$ in $SiO_2$ involved in the trapping-detrapping process and presented in $1/f$ noise are extracted from LF-noise after fitting of all noise components. Figure 18 shows the lowest $\lambda N_t$ for conventional p-Si MOSFET and values higher by an order of magnitude

for p-SiGe MOSFETs. This could be explained by the difference in Si and SiGe fabrication technologies. The quality of $SiO_2$ for p-SiGe MOSFETs is worse, due to the lower thermal budget required for the whole processing. Also, average densities of traps $\lambda N_t$ extracted from LF-noise are less than values usually obtained from *C-V* characteristics. This could be explained if it is assumed that either not all the traps inside $SiO_2$ are involved in the trapping-detrapping process or other processes also affect the LF-noise.

## 5. Conclusions

In conclusion, all these results demonstrate the advantages of metamorphic MOSFETs with a high Ge content and strained $Si_{1-x}Ge_x$ p-channel grown on a relaxed $Si_{1-y}Ge_y$ buffer in comparison with a bulk p-Si MOSFET. Both SS-MBE and LEPECVD grown material shows very significant hole mobility improvement over bulk Si, with peak values of $\mu_{eff} = 760$ cm$^2$V$^{-1}$s$^{-1}$. Of the three types devices studied the SS-MBE grown $Si_{0.3}Ge_{0.7}$ structure produces the best performance as a sub-micron MOSFET device, mainly due to the incorporation of an Sb-doped punch-through stopper. This results in a SiGe device with similar to the Si control short channel properties at an effective channel length of 0.55 $\mu$m to the Si control. The current drive enhancement ratio of 2.0 over p-Si MOSFET is found in the p-$Si_{0.3}Ge_{0.7}$ MOSFET, and is due to higher hole mobility $\mu_{eff} = 500$ cm$^2$V$^{-1}$s$^{-1}$ in the $Si_{0.3}Ge_{0.7}$ quantum well. The highest drive current is found in the p-$Si_{0.2}Ge_{0.8}$ MOSFET, with a current drive enhancement ratio of more than 3.0 over the p-Si MOSFET. These studies demonstrate clearly the potential of using strained $Si_{0.3}Ge_{0.7}$ and $Si_{0.2}Ge_{0.8}$ heterostructures for the PMOSFETs in CMOS structure.

Also, the results presented in this paper demonstrate a significant reduction in LF-noise NPSD, achieved in metamorphic p-$Si_{0.3}Ge_{0.7}$ and p-$Si_{0.2}Ge_{0.8}$ MOSFETs compared to bulk p-Si. This advantage is observed in sub-micron devices relevant to the current Si-CMOS technology. In the linear region of MOSFET operation the reduction in $1/f$ noise is higher than a factor of three. The reduction is attributed to the existence of the Si cap layer in the p-SiGe MOSFETs, which further separates the holes in the buried $Si_{0.3}Ge_{0.7}$ and $Si_{0.2}Ge_{0.8}$ channels from the traps near the $Si/SiO_2$ interface, and an immeasurably low influence of traps at the Si/SiGe interface. LF-noise performance of p-SiGe MOSFETs could be significantly improved after technology of gate dielectric fabrication will be improved.

The influence of a "punch-through" stopper on the device reliability was analysed. It reduces short channel effects in sub-micron developed MOSFETs and provides perfect performance of devices especially in the subthreshold region as it is most important for switching devices (CMOS logic). Also $1/f$ noise is not significantly increased in buried channel p-SiGe devices with a "punch-through" stopper as in conventional p-Si MOSFETs with heavily doped substrate due to a 4–5 nm Si cap used. On the other hand, the introduced "punch-through" stopper slightly decreases the maximum current of the device and increases the influence of the negative effects due to impact ionization in the drain depletion area. These effects could be reduced through the optimization of the contact shape and doping profile. Better results could possibly be obtained using p-SiGe buried channel heterostructures together with SOI technology (analogue of fully depleted SOI MOSFETs [10]).

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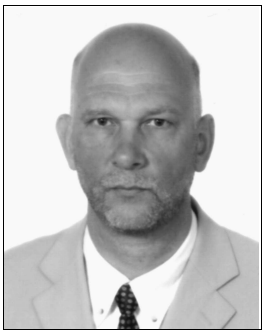

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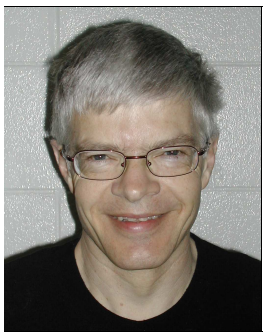

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