Paper

Effects of stress annealing on the electrical and the optical properties of MOS devices

Witold Rzodkiewicz, Andrzej Kudła, Zbigniew Sawicki, and Henryk M. Przewłocki

Abstract—In this paper we show the results of a study of the effects of high-temperature stress annealing in nitrogen on the refraction index of SiO_2 layers and electrical properties in metal-oxide-semiconductor (MOS) devices. We have experimentally characterized the dependence of the reduced effective contact potential difference (ECPD), the effective oxide charge density (N_{eff}), and the mid-gap interface trap density (D_{it}) on the annealing conditions. Subsequently, we have correlated such properties with the dependence of the refraction index and oxide stress on the annealing conditions and silicon dioxide thickness. Also, the dependence of mechanical stress in the Si-SiO_2 system on the oxidation and annealing conditions has been experimentally determined. We consider the contributions of the thermal-relaxation and nitrogen incorporation processes in determining changes in the SiO_2 layer refractive index and the electrical properties with annealing time. This description is consistent with other annealing studies carried out in argon, where only the thermal relaxation process is present.

Keywords— *stress, MOS, Si-SiO_2 system, electrical parameters, refractive index.*

1. Introduction

The annealing of metal-oxide-semiconductor (MOS) devices in nitrogen at high temperatures is broadly used to reduce fixed-charge densities at the Si-SiO_2 interface [1]. We have studied the effect of high-temperature annealing in nitrogen on the stress properties, the optical properties, and the electrical properties of MOS devices. In this paper, we report our findings of the influence of annealing in nitrogen on the basic electrical parameters of MOS devices, namely the effective charge density N_{eff}, the mid-gap interface trap density D_{it}, and the reduced effective contact potential difference ϕ^*_{MS}, as well as on the thickness-averaged stress in SiO_2 layers and on the refractive index of such layers. These investigations have been extensively described in [2, 3].

2. Experimental details

In this study 4-inch (100) n-type silicon wafers of different resistivities were used. High-resistivity wafers (3–5 Ω/cm) were doped with phosphorus, while low-resistivity (0.005–0.02 Ω/cm) ones were antimonium-doped. After an initial hydrogen-peroxide-based cleaning sequence, the wafers were subjected to a thermal oxidation process at 1000°C in order to grow silicon-dioxide layers with the thickness of approximately 20, 60, and 160 nm. The wafers were subsequently annealed in nitrogen for periods of 0, 120, and 1440 minutes at 1050°C. The front-side metallization was deposited in a thermal evaporator. The thickness of the obtained aluminum layer was approximately 35 and 400 nm. The thin front-side Al is necessary for MOS photoelectric measurements. The front-side Al was patterned using optical lithography. The backside oxide was etched prior to the deposition of backside metallization. The post-metallization annealing was carried out at 450°C for 20 minutes.

The oxide thickness t_{ox} and its refractive index n were determined using either a Gaertner-scientific 115B single-wavelength ellipsometer operating at $\lambda = 632.8$ nm or a J. A. Woollam variable angle spectroscopic ellipsometer (VASE). The analysis of spectroscopic ellipsometry data by means of a model consisting of a silicon substrate, SiO_2-Si interface layer and silicon dioxide layer was carried out. The interface layer thickness was assumed to be 1 nm. The curvature radius R of the wafer was measured using a Tencor FLX-2320 system.

The relationship between the refractive index n and the stress σ_{ox} in the oxide is given by [4–6]:

$$n(\sigma_{ox}) = n_0 + \Delta\sigma_{ox} \cdot \frac{\Delta n}{\Delta\sigma_{ox}}, \tag{1}$$

where: n_0 is the refractive index of a completely relaxed (stress-free) oxide. The value of n_0 is 1.46 [6–8]. The oxide stress σ_{ox} is calculated in this work using Stoney's formula [9–12]:

$$\sigma_{ox} = \frac{1}{6 \cdot R} \cdot \frac{E_{\mathrm{Si}}}{(1-\nu_{\mathrm{Si}})} \cdot \frac{t^2_{\mathrm{Si}}}{t_{ox}}, \tag{2}$$

where: t_{Si} is the silicon wafer thickness, E_{Si} – Young modulus for silicon, and ν_{Si} – Poisson's ratio for silicon. The ratio of $E_{\mathrm{Si}}/(1-\nu_{\mathrm{Si}})$ is 180.5 GPa for (100) silicon [13, 14].

The effective contact-potential difference ϕ_{MS} was measured with the accuracy of ±10 mV using the photoelectric method [15] implemented in the PIE MSPS photoelectric measurement system. The mid-gap interface trap density D_{it} was measured by means of the HF-LF method using a Keithley PKG 82 system. The general characterization of the electrical properties of the MOS structures was carried out using a SSM 450i system.

The effective contact potential difference (ϕ_{MS} or ECPD) is defined as [1]:

$$\phi_{MS} \equiv \phi_M - \left(\chi_{\rm Si} + \frac{E_{g,\rm Si}}{2q} + \phi_F\right), \quad (3)$$

where: ϕ_M is the barrier height at the gate-dielectric interface, $\chi_{\rm Si}$ – the electron affinity in the silicon substrate, $E_{g,\rm Si}$ – the silicon band gap, and ϕ_F – the Fermi level in the silicon substrate measured from the mid-gap level. The effective contact potential difference is determined from [15]:

$$\phi_{MS} = V_{G0} = \phi_{S0}\,, \quad (4)$$

where: V_{G0} is the gate voltage corresponding to zero potential drop across the dielectric, which is determined by the photoelectric method, and ϕ_{S0} the silicon surface potential when $V_G = V_{G0}$.

The reduced effective contact potential difference ϕ^*_{MS} is defined as:

$$\phi^*_{MS} \equiv \phi_M - \chi_{\rm Si} \quad (5)$$

or

$$\phi^*_{MS} = \phi_{MS} + \frac{E_{g,\rm Si}}{2q} + \phi_F\,. \quad (6)$$

The electrical parameter described above depends on the barrier heights on both sides of the dielectric but is independent of the doping concentration in the substrate. On the contrary, ϕ_{MS} depends on the doping concentration in the substrate.

The density of the effective charge N_{eff} or Q_{eff}/q is calculated from:

$$Q_{eff} = C_{ox}\left(\phi_{MS} - V_{FB}\right), \quad (7)$$

where: C_{ox} – oxide capacitance per unit area. C_{ox} is determined from the measured capacitance $C_{acc}(F)$ in accumulation using $C_{ox} = C_{acc}/A$, where A is the device area.

3. Results and discussion

The results of the measurements carried out on samples with $t_{ox} \approx$ 20, 60 and 160 nm have been shown in Figures 1–10. We must emphasize that the above mentioned results are based on the premise that the mechanical stress in the wafers prior to processing is not crucial. Therefore it is assumed that it is initially the same in all wafers. All results presented in our paper are fairly consistent with this assumption.

Observations and measurements carried out on the wafers with silicon dioxide thickness of about 20 nm indicate that wafer deformation due to the oxidation process doesn't occur in the form of a spherical cap. This is due to the fact that the silicon dioxide layer is too thin to effectively deform the wafer. The stress measurements were carried out both before and after the backside oxide layers were completely removed from the back side of the wafers.

The relationship between the average compressive stress σ_{ox} in the silicon dioxide layer and its thickness is shown in Fig. 1.

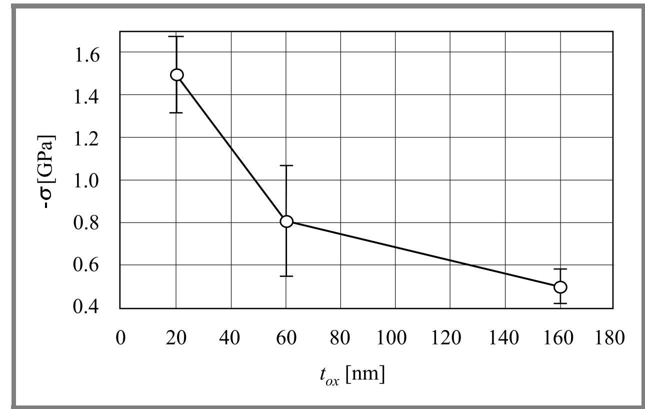

Fig. 1. The average compressive oxide stress $-\sigma_{ox}$ in the SiO_2 layer versus oxide thickness t_{ox}.

As expected, the magnitude of the compressive stress in the silicon dioxide increases as the SiO_2 thickness is decreased. The dependence of SiO_2 refractive index n_{SE} obtained by spectroscopic ellipsometry on the silicon dioxide thickness is portrayed in Fig. 2.

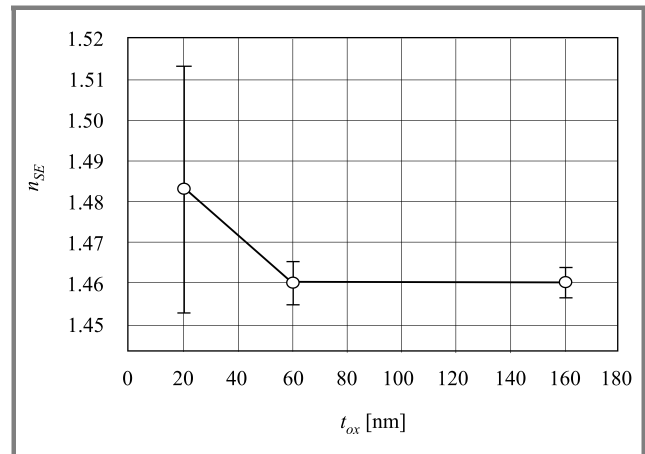

Fig. 2. SiO_2 refractive index n versus oxide thickness t_{ox}.

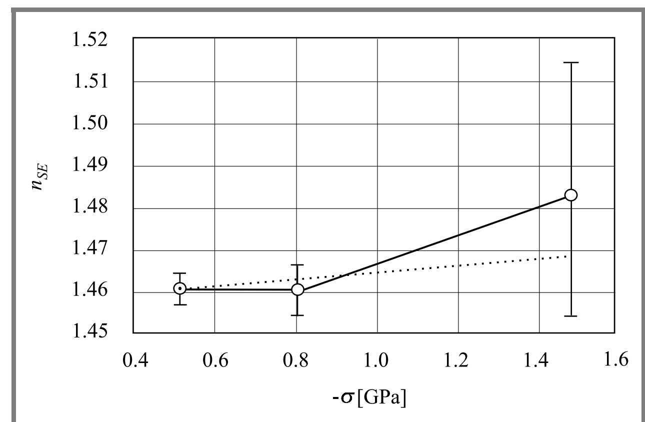

Fig. 3. The average refractive index of SiO_2 as a function of average silicon dioxide compressive stress.

By combination of the results from Figs. 1 and 2, we obtain Fig. 3, which shows the relationship between the average refractive index of SiO_2 and average compressive stress in the oxide. In this plot we point out that the refractive index increases with an increase of the compressive stress.

The effects of extended annealing in nitrogen on the average compressive stress σ_{ox} and the refractive index of SiO_2 are shown in Figs. 4 and 5. In these figures, we observe, that σ_{ox} and n have a tendency to decrease as a result of prolonged anneals due to stress relaxation in the oxide layers by viscous flow and/or decompaction. However, the increase of the oxide refractive index observed for longer annealing times results from nitrogen incorporation in the SiO_2 layer in the vicinity of the Si-SiO_2 interface.

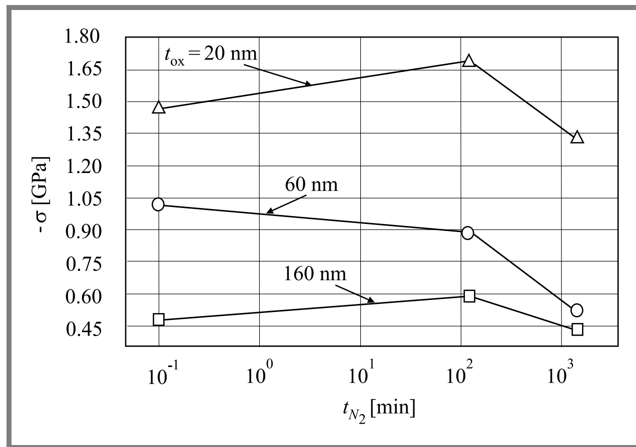

Fig. 4. The average compressive oxide stress $-\sigma_{ox}$ in the SiO_2 layer versus nitrogen-annealing time t_{N_2} for three silicon dioxide thicknesses of 20, 60, and 160 nm.

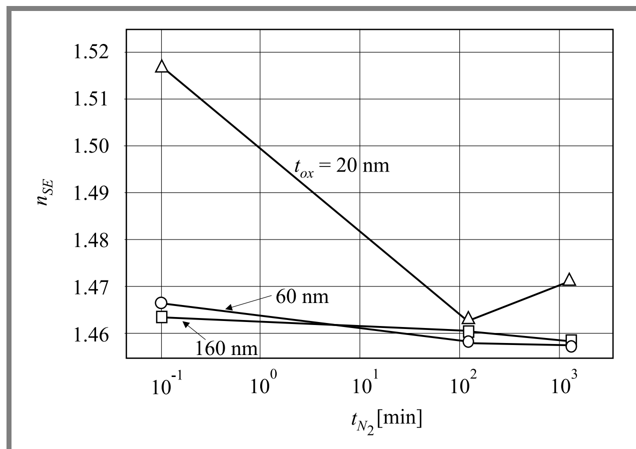

Fig. 5. SiO_2 refractive index n versus nitrogen-annealing time t_{N_2} for three silicon dioxide thicknesses of 20, 60, and 160 nm.

In Fig. 6 the dependence of the mid-gap interface trap density D_{it} on the duration of annealing in nitrogen t_{N_2} is shown. This parameter is particularly sensitive to both the nitrogen-annealing time and the oxide thickness (Fig. 7).

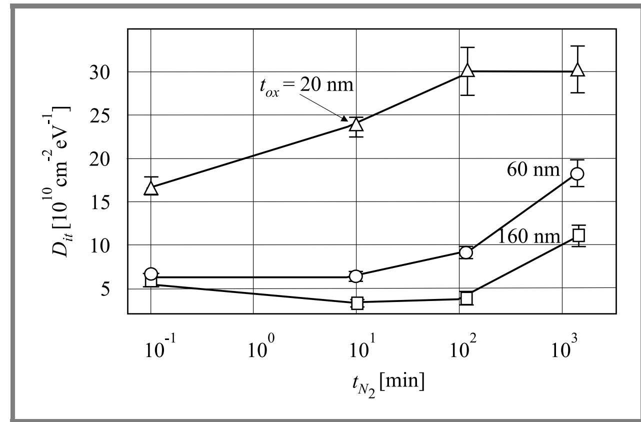

Fig. 6. Mid-gap interface trap density D_{it} versus nitrogen-annealing time t_{N_2} for three silicon dioxide thicknesses of 20, 60, and 160 nm.

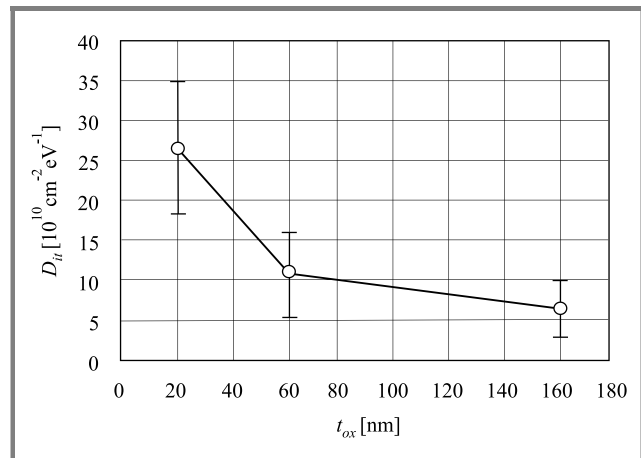

Fig. 7. Mid-gap interface trap density D_{it} versus oxide thickness.

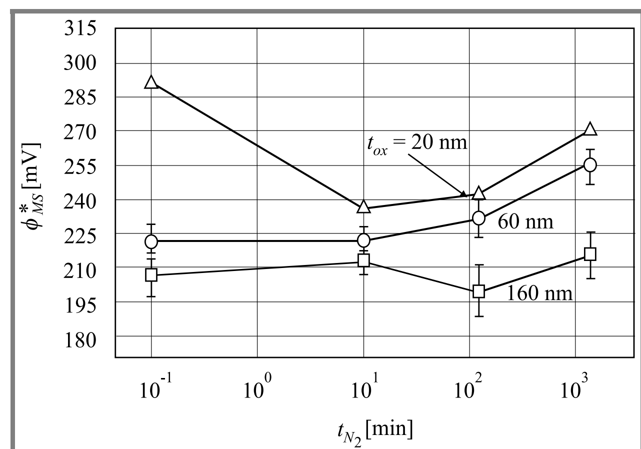

Fig. 8. The reduced effective contact potential difference ϕ^*_{MS} on nitrogen-annealing time t_{N_2} for three silicon dioxide thicknesses of 20, 60, and 160 nm.

Photoelectric measurements allowed the effective contact potential difference (the ϕ_{MS} factor or EPCD) to be determined. The reduced effective contact potential differ-

ence ϕ^*_{MS} is shown as a function of nitrogen-annealing time and oxide thickness in Figs. 8 and 9 for the three oxide thicknesses studied.

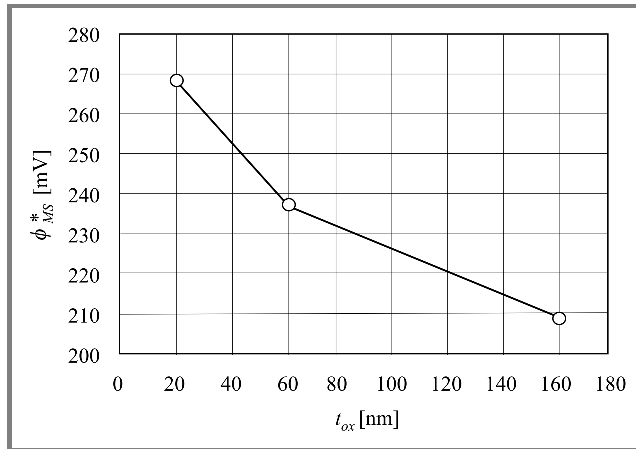

Fig. 9. The reduced effective contact potential difference ϕ^*_{MS} versus oxide thickness.

The dependence of the effective oxide charge density (N_{eff}) on the nitrogen-annealing time (t_{N_2}) is illustrated in Fig. 10.

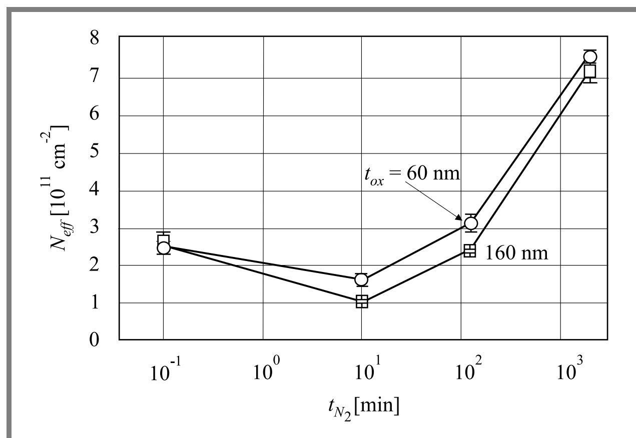

Fig. 10. Effective charge density N_{eff} in the oxide versus nitrogen-annealing time t_{N_2} for three silicon dioxide thicknesses of 60 and 160 nm.

The shape of the $\sigma_{ox}(t_{N_2})$, $n(t_{N_2})$, $D_{it}(t_{N_2})$, $\phi^*_{MS}(t_{N_2})$, and $N_{eff}(t_{N_2})$ plots results from the combination of two competing processes. The first of those is thermal-relaxation that occurs in the initial phases of annealing. The second is nitrogen incorporation that takes place in the SiO_2 layer in the vicinity of the Si-SiO_2 interface. The latter occurs at longer times of annealing in nitrogen. The trends in the above described plots are such that both the SiO_2 refractive index and the electrical parameters decrease in the case of short annealing times then start increasing when annealing times become longer.

4. Conclusions

We have investigated the effect of high-temperature stress annealing in the ambient of nitrogen on the optical and electrical properties of MOS devices. Based on the changes occurring in the refractive index of the SiO_2 layer and electrical parameters of MOS structures, we claim that two processes are present during annealing: thermal relaxation and nitrogen incorporation. The first process is responsible for the initial trends in the silicon dioxide properties. The second process is, however, responsible for the trends in the SiO_2 properties at longer annealing times.

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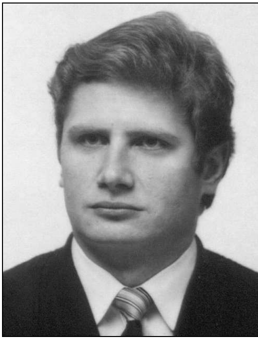

Witold Rzodkiewicz was born in Warsaw in 1971. He received the M.Sc. degree in material science and engineering from the Warsaw University of Technology in 1995. His Masters project in "Studies of the structural perfection of GaInAsSb quaternary layers grown by LPE on GaSb substrates" was carried out at the Institute of Electron Technology (IET) in Warsaw. From 1995 to 1998, he was with the Department of Materials and Semiconductor Structures Research of the Institute of Electron Technology in Warsaw as a Research Assistant, working in the area of process-induced defects in semiconductor structures. From 1998 till now, he is with the Department of MOS System Studies in IET as a Research Assistant.

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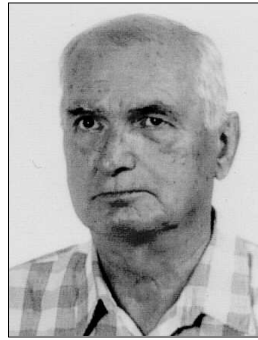

Zbigniew Sawicki was born in 1932. From 1951 to 1956 he studied astrophysics at the Warsaw University. Since 1958 he is engaged in the research of semiconductor technology. His special interest was oxidation and diffusion processes in silicon.

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Andrzej Kudła, Henryk M. Przewłocki – for biography, see this issue, p. 39.