Paper

Standardization of the compact model coding: non-fully depleted SOI MOSFET example

Władysław Grabiński, Daniel Tomaszewski, Laurent Lemaitre, and Andrzej Jakubowski

Abstract— The initiative to standardize compact (SPICE-like) modelling has recently gained momentum in the semiconductor industry. Some of the important issues of the compact modelling must be addressed, such as accuracy, testing, availability, version control, verification and validation. Most compact models developed in the past did not account for these key issues which are of highest importance when introducing a new compact model to the semiconductor industry in particular going beyond the ITRS roadmap technological 100 nm node. An important application for non-fully depleted SOI technology is high performance microprocessors, other high speed logic chips, as well as analogue RF circuits. The IC design process requires a compact model that describes in detail the electrical characteristics of SOI MOSFET transistors. In this paper a non-fully depleted SOI MOSFET model and its Verilog-AMS description will be presented.

Keywords—Verilog-AMS, compact model coding, SOI MOSFET.

1. Introduction

Most compact models developed in the past did not account for several key issues that are of highest importance when introducing a new compact model to the semiconductor industry in particular going beyond the ITRS roadmap technological 100 nm node [1]. Compact models were developed in several different ways by dedicated modelling groups including university research, internal company research and developments. Individual groups were targeting different domains and providing application specific solutions. Each modelling group uses individual tools and techniques for these modelling tasks, which are in many cases strongly dependent on the selected target simulation tool. At this time there is no standardized language to formulate compact model equations. Most developers write first drafts of their device models in interpreted languages. Most currently used interpreted modelling languages are those offered by commercial interactive mathematical tools. Other researchers prefer to use open-source interpreters and compilers.

Generally speaking, compact device modelling suffers from a lack of well-established, standardized methodology. Moreover, neither approach provides the option to share the code between different modelling teams and industrial partners. Nevertheless, to provide reliable industrial solution a compact model and its description have to be standardized. Development of compact device models involves different tasks which could be summarized as follows: building physics based constitutive equations; encoding constitutive equations in computer language; implementing the code into electrical simulators; validating compact device model implementation. In this paper, we exploit hardware behaviour languages (HDL) as the basis for device model developments. More specifically, we demonstrate how compact modelling can be standardized using Verilog-AMS [2], one of the most popular HDL. Already at the model coding phase, the developers can evaluate the validity and robustness of their model using any electrical circuit simulator that supports Verilog-AMS.

The current standardization efforts include models for bulk and SOI MOSFETs, and Si/SiGe BJT technologies. The silicon-on-insulator CMOS integrated circuits (ICs) offer many advantages as compared to their conventional bulk silicon counterparts. An important application for non-fully depleted SOI technology is high performance microprocessors, other high speed logic chips as well as analogue RF circuits. The IC design process requires a compact model that describes in detail the electrical characteristics of SOI MOSFET transistors. In this paper the non-fully depleted SOI MOSFET model [3] and its Verilog-AMS description will be presented.

2. Compact modelling with Verilog-AMS

Verilog-AMS provides a new dimension of design, simulation, and testing capability for electronic systems. The powerful features of Verilog-AMS language can be used for fast testing of analog and mixed-signal systems. The analog and mixed signal languages, such as Verilog-AMS, VHDL-AMS and Verilog-A, are primarily viewed as simulation tools for mixed-signal and mixed-domain systems. However, the versatility of the behaviour languages at the device-level abstraction allows to apply them to compact modelling as well.

The Verilog-AMS is a superset of Verilog and Verilog A, respectively. Besides the digital components, the language also supports analog behavioural constructs. The behavioural languages for digital system modelling, i.e., Verilog-Digital or Verilog-D proceed with the discrete change in signals at discrete points in time. However, Verilog-AMS simulation takes place in the analog

domain and all the differential algebraic equations (DAEs) are solved at every point in time. The generalized form of Kirchhoff's potential (KPL) and flow laws (KFL) formulates the DAEs.
Each model may require a different approach, yet some of the general guidelines can be followed to make the process systematic.

2.1. Analog behavioural modelling

The behavioural description with the Verilog A language can be used to represent different types of behaviours, including linear, nonlinear, integro-differential and analog event driven or any combination thereof. It is important to note that it is valid in the time domain and encapsulates a large signal behaviour. Performing linearization of the large signal model around its operation point allows small signal AC analysis to be performed as well. All behavioural models strongly depend on the understanding of the model, its formulation for the well defined regions of valid operation. The model must be stable as well as continuous in the description of its main region of operation. The model developer is responsible for the model stability. The Verilog-A language provides capabilities to effectively handle model non-continuity but still relies on the developer for recognizing and utilizing these capabilities.
In the Verilog-A language, all analog behaviour description is defined within the analog statement. That statement encompasses all necessary statements used to describe interrelations of input and output signals of a given module. The analog statement is used to define the behaviour model in terms of contributions statements, control flow and/or analog events statements. Valid syntax is shown below:

analog begin
    <statements>
end

The groups of the statements within the analog block are processed sequentially in the given order and at each time step during a transient simulation. This formulation allows the model developer to define the flow of control within the block module which has implications in the formulations of the analog behaviours for stability and robustness.
Parameter declarations are extensions of the basic variable type definitions supported by Verilog-A and have similar meaning to other programming languages. In addition, parameter definition supports an extended declaration syntax for range checking which allow developers to control acceptable parameter ranges or parameter values. Specifying the default value and valid range of its values assigned during model initialization, the user is able to restrict the parameter values to guarantee proper use of the model. The basic parameter syntax is shown below:

parameter real W= 1E-6 **from**(0.0 **: inf**);

The parameter W has the value of 1 μm, which is considered constant during model evaluations. An optional range specification limits any inputs of W between zero (0.0) and infinity (*inf*) but excluding upper and lower limits.

```
'include "disciplines.h"
//
// Module declaration
module soi(d, fg, s, bg)
//
// Terminal declaration
input      d, fg, s, bg;
electrical d, fg, s, bg;
//
// Parameter declaration
parameter real L= 1E-6
from [0.0:inf];
parameter real W= 1E-6
from [0.0:inf];
//
// Internal variables declaration
real Gammaf, EpsSi, Qdopm, Coxf;
//
// Analog block
analog begin
//
Vds=V(d,s); //Access function
//
//
Gammaf = sqrt(2.0*EpsSi*QDop)/Coxf;
//
Idc(s,d) < + TotIS + TotID;
end //analog
endmodule
```

Fig. 1. A Verilog-A template for a compact MOSFET model.

The flows and potentials on nets, ports, and branches in Verilog-AMS can be accessed using *access functions*. The name of the access function is taken from the discipline of the net, port, or branch associated with the signal (Fig. 1), i.e.,

Vds = **V(**d, s**)**;

The function above creates an unnamed branch from d to s (if it does not already exist) and then accesses the branch flow. In the following example $I(d)$ does the same from d to the global reference node (*ground*).
In Digital Verilog, the behavioural description always uses blocks, integer variables and bit signals. With Verilog-A, the behavioural description uses analog block, integer and real variables and analog signals. Analog signal is declared following a discipline. A discipline is an abstract data type that describes a continuous domain by associating the potential and flow nature. To assign an expression to a signal, Verilog-A introduces the *contribution operator* $<+$. It is used in a contribution statement where a behaviour relation is described between input and output signal:

output_signal $<+$ f(input_signal);

The generalized form of the contribution statement above consists of two parts, a left-hand side, and a right-hand

side, separated by the *contribution operator* $<+$. Any real-number expression may be used as the right-hand side. The left-hand side specifies the source branch signal that the right-hand side is to be assigned to. It must consist of an access function applied to a branch. The access function within the expression function may be used in any mode of operation: linear, nonlinear, algebraic or dynamic, as well as constants and parameters. It can be applied to any nodes or ports following the corresponding discipline definition.
The example below illustrates the assignment of the gain of the amplifier without including frequency effects:

```
V(out) <+ -gain * V(in)
```

This type of functional models is used for top level system architecture design and analysis but can be easily applied to the transistor level modelling.

2.2. Multi-discipline description

The Verilog-A language can support the description of systems used in many domains, such as electrical, mechanical, fluid dynamics and thermodynamics. For this purpose, the language provides a standard definition file where the main disciplines are defined. In the same module, nodes from different disciplines can be mixed.
Several semiconductor companies provide Verilog-AMS models of their products for simulation purposes. In addition, most of the common digital as well as analog blocks are freely available on the world wide web in the form of HDL models. If these HDL codes are converted to Verilog-AMS, they can be extremely useful for testing the analog ICs, particularly the ICs under development. Following sections show Verilog-AMS applications to compact modelling of the non-fully depleted SOI MOSFET modelling.

3. Non-fully depleted SOI MOSFET

The non-fully depleted SOI MOSFETs model presented in the paper is based on the general formula (1):

$$i_S(t) + i_{Gf}(t) + i_D(t) + i_{Gb}(t) = 0\,, \tag{1}$$

where $i_S(t)$, $i_{Gf}(t)$, $i_D(t)$, $i_{Gb}(t)$ denote currents flowing into the device at any time instant t. The equation (1) is to be solved for a floating body-source voltage $v_{BS}(t)$, which is the main variable of the model. The condition (1) expresses the overall electrical neutrality of the MOSFET. The formula (1) is illustrated in Fig. 2, which shows the approximate spatial distribution of paths of carriers in the device. This diagram also shows the main phenomena relevant to the non-fully depleted SOI MOSFET operation and accounted for in the model:

– transport at the Si-SiO_2 interface ($I_{c,f/b}$ – diffusion/drift at the front/back Si-SiO_2 interface);

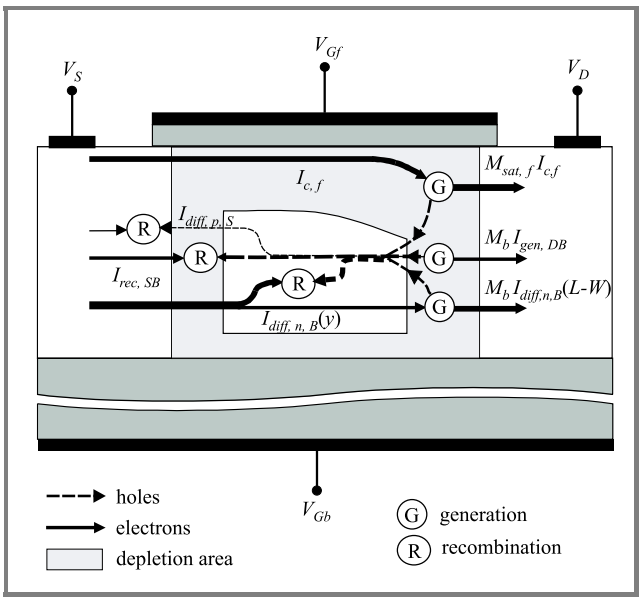


Fig. 2. Approximation of the distribution of currents components in the non-fully depleted SOI MOSFET.

– diffusion of electrons in the floating body ($I_{diff,n,B}$);

– thermal generation/recombination in the space-charge areas ($I_{rec,SB}$, $I_{gen,DB}$);

– avalanche ionization in the regions with strong electric field (M_b in the case of the drain-body junction, $M_{sat,f/b}$ in the case of the pinch-off regions);

– displacement currents (in the case of AC analysis only).

The DC model has been developed as a solution of (1) using the sinusoidal steady-state analysis (S^3A) method [4]. According to this method any time-dependent variable in the device may be expressed as:

$$u(t) = U + u^* \cdot \mathrm{e}^{\mathrm{j}\omega t} \tag{2a}$$

or

$$v(y,t) = V(y) + v^*(y) \cdot \mathrm{e}^{\mathrm{j}\omega t}\,, \tag{2b}$$

where: y – spatial coordinate along the channel; U, $V(y)$ – steady-state components; u^*, $v^*(y)$ – complex amplitudes.

This approach allows for efficient formulation of consistent DC and AC models of the corresponding device. These models account for identical sets of phenomena. Moreover, the AC models do not suffer from the requirement to partition the channel charge into source- and drain-related components. The AC models of nodal currents may be used for straightforward calculation of device inter-nodal admittances (conductances and capacitances), which are in general bias- and frequency-dependent.
Separation of the steady-state and non-steady-state components of (1) leads to the general expressions describing DC

Eq. (3a) and AC Eq. (3b) models of the non-fully depleted SOI MOSFET characteristics:

$$I_S + I_D = 0\,, \tag{3a}$$

$$i_s^* + i_{gf}^* + i_d^* + i_{gb}^* = 0\,. \tag{3b}$$

The solution of these two equations allows the DC and AC components of the floating body potential $v_{BS}(t)$ to be determined. The accuracy of the obtained result depends, of course, on the accuracy of DC current modelling. The model used in this paper will be presented in the next section.

3.1. Current formulation

The total DC source current I_S may be viewed as a superposition of the source-body junction current I_{SB} and the channel current $I_{c,f/b}$:

$$I_s = I_{SB} - I_{c,f/b}\,. \tag{4}$$

Similarly, the total DC drain current I_D may be considered as the difference between the drain-body junction current I_{DB} and the channel current $I_{c,f/b}$ multiplied by the appropriate factor of avalanche multiplication within the "pinch-off" region:

$$I_D = -I_{DB} + M_{sat,f/b} I_{c,f/b}\,. \tag{5}$$

A simple model of the inversion layer current has been used. For simplicity only front inversion layer currents are described below. In general similar expressions are valid also for back interface. The non-saturation region is described with the simple model:

$$I_{c,f} = \frac{W\mu_{c,f}C_{ox,f}}{L}\left(V_{GfS} - V_{TH,f} - \frac{V_{DS}}{2}\right)V_{DS}\,, \tag{6}$$

where: L, W – channel length and width, respectively, $\mu_{c,f}$ – channel mobility at the front interface, $V_{TH,f}$ – front gate threshold voltage.

In saturation the model is as follows:

$$I_{c,f} = \frac{W\mu_{c,f}C_{ox,f}}{L - \Delta L_{sat,f}}\left(V_{GfS} - V_{TH,f} - \frac{V_{DSsat,f}}{2}\right)V_{DSsat,f}\,, \tag{7}$$

where: $V_{Dsat,f}$ – saturation voltage for the front MOS structure, $\Delta L_{sat,f}$ – front channel length reduction in saturation. These variables are defined as follows:

$$V_{DSsat,f} = V_{GfS} - V_{TH,f} + L\,E_{sat,f} - \sqrt{\left(V_{GfS} - V_{TH,f}\right)^2 + \left(LE_{sat,f}\right)^2}\,, \tag{8}$$

$$\Delta L_{sat,f} = \sqrt{\frac{2\varepsilon_{\mathrm{Si}}}{qN_B}\left(V_{DS} - V_{DSsat,f}\right) + \left(\frac{\varepsilon_{\mathrm{Si}}E_{sat,f}}{qN_B}\right)^2} - \frac{\varepsilon_{\mathrm{Si}}E_{sat,f}}{qN_B}\,. \tag{9}$$

In the above equations $E_{sat,f}$ denotes the critical field resulting in the saturation of carrier velocity at the front interface.

The source-body junction current consists of two components: the diffusion current at the "source" border of the quasi-neutral region of density $J_{diff,n,B}$, and the recombination current originating from the source-body junction space-charge region. The area of the source-body junction may be calculated as the product of the channel width W and the difference between body thickness t_{Si} and depletion widths formed by the front and back gates (W_{GfB} and W_{GbB}, respectively). The depletion widths depend on the gate-body voltage (in the depletion and weak inversion range) or body-source voltage (in the strong inversion range). Thus the following formula for the source-body junction current can be formulated:

$$I_{SB} = W\left(t_{\mathrm{Si}} - W_{GfB} - W_{GbB}\right) \times \left[J_{diff,n,B}(W_{SB}) - qW_{SB}\langle R_{th,SB}\rangle\right]. \tag{10}$$

In the above formula W_{SB} is the source-body junction width whereas $\langle R_{th,SB}\rangle$ denotes a mean value of the recombination rate in the source-body junction. It is described with formula (11) derived elsewhere [6]:

$$\langle R_{th,SB}\rangle = \frac{n_i}{2\tau_j}\cdot\frac{\sqrt{\mathrm{e}^{-u_{SB}} - 1}}{u_{bi} + u_{SB}} \times 2\,\mathrm{arctg}\left|\frac{\dfrac{N_{SD}}{n_i} - \dfrac{n_i}{N_B}\mathrm{e}^{-u_{SB}}\sqrt{\mathrm{e}^{-u_{SB}} - 1}}{\mathrm{e}^{-u_{SB}} - 1 + \left(\dfrac{N_{SD}}{n_i} + 1\right)\left(\dfrac{n_i}{N_B}\mathrm{e}^{-u_{SB}} + 1\right)}\right|, \tag{11}$$

where: n_i – intrinsic carrier concentration, N_{SD} – source/drain doping, τ_j – junction lifetime, u_{SB}, u_{bi} – source-body and built-in voltage, respectively, normalized to thermal voltage $V_t = \mathrm{k}T/q$.

The diffusion current in the quasi-neutral region is described in the following way:

$$J_{diff,n,B}(y) = q\frac{D_{n,B}}{L_{n,B}}\frac{n_i^2}{N_B} \times \frac{\mathrm{e}^{-u_{DS}-u_{SB}}\cdot\mathrm{ch}\dfrac{y - W_{SB}}{L_{n,B}} - \mathrm{e}^{-u_{SB}}\mathrm{ch}\dfrac{L - W_{DB} - y}{L_{n,B}}}{\mathrm{sh}\dfrac{L - W_{SB} - W_{DB}}{L_{n,B}}}\,, \tag{12}$$

where: $D_{n,B}$ – diffusion coefficient, $L_{n,B}$ – diffusion length, W_{DB} – drain-body junction width.

The drain-body junction current consists of two components: the diffusion current at the "drain" border of the quasi-neutral region and the recombination current originating from the drain-body junction space-charge region.

Moreover, these two currents are multiplied within the drain-body junction depletion area. Thus the drain-body junction current can be described in the following way:

$$I_{DB} = W(t_{Si} - W_{GfB} - W_{GbB})M_{DB} \times \left[J_{diff,n,B}(L - W_{DB}) - qW_{DB}\langle G_{th,DB}\rangle\right]. \quad (13)$$

In the above formula $\langle G_{th,DB}\rangle$ denotes the mean value of the generation rate in the drain-body junction. Formula $\langle G_{th,DB}\rangle$ is described with formula (14) derived in [6]:

$$\langle G_{th,DB}\rangle = \frac{n_i}{2\tau_j}\frac{\sqrt{1-e^{-u_{DS}-u_{SB}}}}{u_{bi}-u_{DS}-u_{SB}} \times \left(\ln\left|\frac{\frac{N_{SD}}{n_i}+1-\sqrt{1-e^{-u_{DS}-u_{SB}}}}{\frac{N_{SD}}{n_i}+1+\sqrt{1-e^{-u_{DS}-u_{SB}}}}\right| + \ln\left|\frac{\frac{n_i}{N_B}e^{-u_{DS}-u_{SB}}+1+\sqrt{1-e^{-u_{DS}-u_{SB}}}}{\frac{n_i}{N_B}e^{-u_{DS}-u_{SB}}+1-\sqrt{1-e^{-u_{DS}-u_{SB}}}}\right|\right), \quad (14)$$

where: u_{DS} – drain-source and voltage, normalized to thermal voltage $V_t = kT/q$; other variables have the same meanings as in the case of $\langle R_{th,SB}\rangle$ (see Eq. (11)).

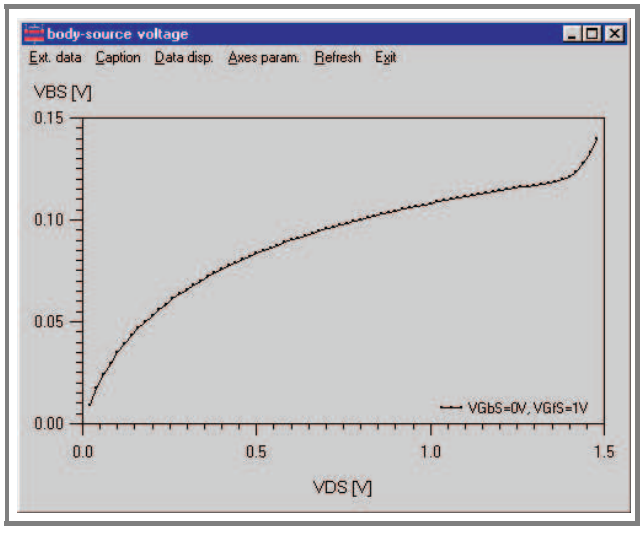


Fig. 3. Body-source voltage versus drain bias in the model of a non-fully depleted SOI MOSFET.

Rather complex formulae describing thermal generation/recombination currents in the space-charge regions have been derived using Shockley-Read-Hall generation/recombination model under the assumption of quasi-linear electric field distribution inside the space charge area. The main reason for this approach was to develop a closed-form model valid particularly for low bias conditions. In the case of a small V_{DS} voltage generation/recombination model is very important for obtaining the solution of Eq. (3a).

Figure 3 shows that in the presented model the iterative solution of this equation leads to a proper source-body voltage behaviour regardless of the drain bias. This is not the case with several other models of non-fully depleted devices.

3.2. Charge definition

After the solution of Eq. (3a) (V_{BS} voltage) was found all other variables describing the device operation can be calculated. Finally charges associated with the source (Q_S), front gate (Q_{Gf}), drain (Q_D) and back gate (Q_{Gb}) electrodes can be obtained in the presented model in a typical way:

$$Q_S = W\left[\int_0^L\left(1-\frac{y}{L}\right)q'_{c,f}(y)dy + \int_0^L\left(1-\frac{y}{L}\right)q'_{c,b}(y)dy\right], \quad (15)$$

$$Q_{Gf} = W\int_0^L q'_{Gf}(y)dy, \quad (16)$$

$$Q_D = W\left[\int_0^L\frac{y}{L}q'_{c,f}(y)dy + \int_0^L\frac{y}{L}q'_{c,b}(y)dy\right], \quad (17)$$

$$Q_{Gb} = W\int_0^L q'_{Gb}(y)dy, \quad (18)$$

where $q'_{Gf}(y)$, $q'_{Gb}(y)$ denote densities (per unit area) of the gates charges, whereas $q'_{c,f}(y)$, $q'_{c,b}(y)$ are densities of the inversion layer charges at the front and back Si-SiO_2 interfaces. The densities of the charges corresponding to the front interface are given with the following formulae:

$$q'_{c,f}(y) = -C_{ox,f}\left[V_{Gf} - V_{FB,f} - \psi_{s,f}(y) + \frac{q'_{B,f}(y)}{C_{ox,f}}\right], \quad (19)$$

$$q'_{G,f}(y) = C_{ox,f}\left[V_{Gf} - \Phi_{MS,f} - \psi_{s,f}(y)\right]. \quad (20)$$

Both expressions mentioned above require surface potential distribution $\Psi(y)$. It depends on gate bias. In the case of accumulation, depletion and weak inversion conditions it is almost constant along the gate, whereas in the case of strong inversion conditions it follows the Fermi

quasi-level. Analogous expressions are of course valid for the back interface.

4. Automatic device model synthesizer modelling example

This section concludes the paper by describing the simulator implementation of the non fully-depleted SOI MOSFET model using the automatic device model synthesizer (ADMS) tool [4].

Creating a new SPICE model consists of two main steps: defining the parameters that the user will enter from the net list or schematic level, writing the model *c*-code itself. Following these steps a new SPICE model can be used in linear, nonlinear (i.e., harmonic balance), transient and circuit envelope simulation modes depending on the simulator capabilities. The ADMS processes both steps. Based on the Verilog-AMS compact model description [2, 3], the ADMS tool generated all necessary *c*-code to handle the model and its instance parameters, model codes including all additional functions, as well as the required derivatives with respect to terminal voltages. The ADMS tool also generates the needed make files to simplify the procedure of compiling and linking

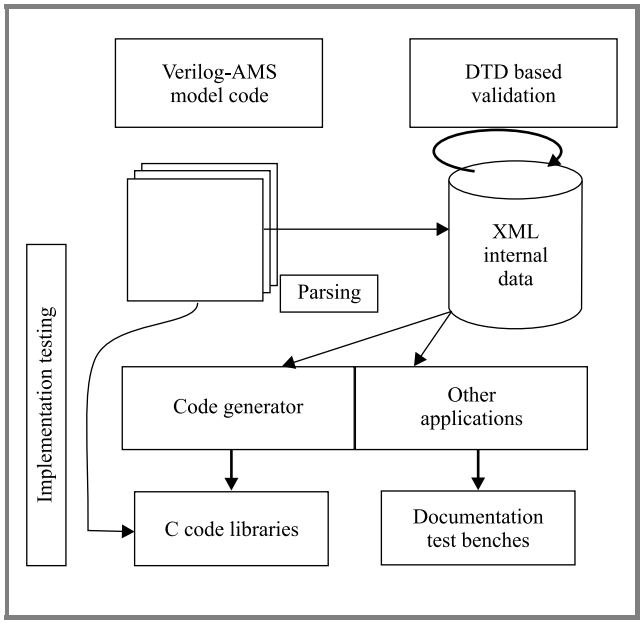


Fig. 4. Basic component of the ADMS system and internal data flows.

the new model with the simulator. ADMS reduces the implementation efforts of compact device definition using Verilog-AMS model description. At the same time, it offers a way to substantially improve the robustness of new compact device models. Implementation of the same model across different electrical circuit simulators is automated [7, 8].

Figure 4 shows basic component of the ADMS tool and illustrates the internal data flow. The main data representations used in ADMS are based on XML, which is the universal format for structured documents and data on the world wide web. XML provides a large set of technologies that simplify the design of robust, re-usable code. It offers a simple way to validate internal data. Rules that organize valid data are written in a subset of XML. The set of rules forms the so-called document type definition (DTD). Embedding of an external DTD is possible. This feature favors the re-use of well established formats. Technologies built around XML give a powerful means to manipulate XML data.

5. Conclusion

The behavioural modelling futures of the Verilog-AMS merged with the ADMS tool [4] offers an excellent compact modelling environment. It facilitates faster development of advanced models and allows faster implementation into commercial IC design tools. Existing models could be smoothly extended to include important effects such as RF and thermo-dynamical effects. Furthermore, developers of new compact models now have access to the a coherent and highly reliable modelling framework simplifying model evaluation procedures and verification tasks across different simulation platforms and operating systems.

References

[1] ITRS Roadmap Update, 2003, http://www.public.itrs.net

[2] Open Verilog International, "Verilog-AMS, Language Reference Manual", Version 1.9, 1999, http://www.accellera.org/

[3] D. Tomaszewski, "Consistent DC and AC models of non-fully depleted SOI MOSFETS in strong inversion", in *Proc. 9th Int. Conf. Mix.-Sig. Des. Integr. Cir. Syst. MIXDES*, Wrocław, Poland, 2002, pp. 111–114.

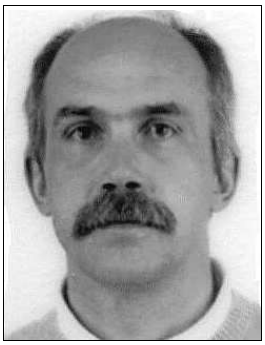
[4] L. Lemaitre, C. McAndrew, and S. Hamm, "ADMS – automatic device model synthesizer", in *Proc. IEEE CICC 2002*, Florida, USA, 2002, pp. 27–30.

[5] J. R. Hauser, "Small signal properties of field effect devices", *IEEE Trans. Electron Dev.*, vol. 12, pp. 605–618, 1965.

[6] D. Tomaszewski, "A small-signal model of SOI MOSFETs capacitances". Ph.D. thesis, Institute of Electron Technology, Warsaw, 1998.

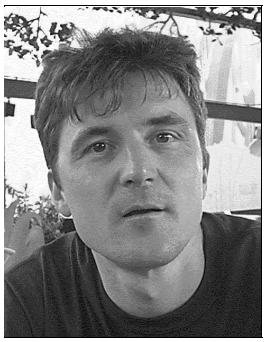
[7] L. Lemaitre, W. Grabiński, and C. McAndrew, "Compact device modeling using Verilog-A and ADMS", in *Proc. 9th Int. Conf. Mix.-Sig. Des. Integr. Cir. Syst. MIXDES*, Wrocław, Poland, 2002, pp. 59–62.

[8] C. Lallement, F. Pêcheux, and W. Grabiński, "High level description of thermodynamical effects in the EKV 2.6 most model", in *Proc. 9th Int. Conf. Mix.-Sig. Des. Integr. Cir. Syst. MIXDES*, Wrocław, Poland, 2002, pp. 45–50.



Władysław Grabiński was a Research Assistant, from 1991 to 1998, at the Integrated Systems Lab, ETH Zürich, Switzerland, supporting the CMOS and BiCMOS technology developments by electrical characterization of the processes and devices. From 1999 to 2000, he was with LEG, EPF Lausanne, and was engaged in the compact MOSFET model developments supporting numerical device simulation and parameter extraction. Since 2000, he is Technical Staff Engineer at Freescale (launched by Motorola), Geneva Modeling Center, Switzerland. He is responsible for modeling, characterization and parameter extraction of MOS transistors for the design of RF CMOS circuits. His current research interests are in high-frequency characterization, compact modeling and device numerical simulations of MOSFETs for wireless applications. He is IEEE member and also involved in activities of the MOS-AK compact modeling group and has been serving as a coordinating manager since 1999.

e-mail: w.grabinski@freescale.com
Freescale, Geneva Modeling Center
207 route de Ferney
CH-1218 Le Grand Saconnex, Switzerland



Laurent Lemaitre is with Freescale (launched by Motorola) since 1995. His main work involves the development and support of compact modeling. He is a member of the Verilog-AMS subcommittee responsible for compact modeling extensions. He received his master's degree and in electrical engineering from ENSERG-Grenoble in 1987 and his Ph.D. degree from the Swiss Polytechnic Institute of Technology-Lausanne in 1994.

e-mail: Laurent.Lemaitre@freescale.com
Freescale, Geneva Modeling Center
207 route de Ferney
CH-1218 Le Grand Saconnex, Switzerland

Daniel Tomaszewski – for biography, see this issue, p. 93.

Andrzej Jakubowski – for biography, see this issue, p. 75.