Invited paper

Variation Analysis of CMOS Technologies Using Surface-Potential MOSFET Model

Hans Jürgen Mattausch, Akihiro Yumisaki, Norio Sadachika, Akihiro Kaya, Koh Johguchi, Tetsushi Koide, and Mitiko Miura-Mattausch

Abstract— An analysis of the measured macroscopic within-wafer variations for threshold voltage (V_{th}) and on-current (I_{on}) over several technology generations (180 nm, 100 nm and 65 nm) is reported. It is verified that the dominant microscopic variations of the MOSFET device can be extracted quantitatively from these macroscopic variation data by applying the surface-potential compact model Hiroshima University STARC IGFET model 2 (HiSIM2), which is presently brought into industrial application. Only a small number of microscopic parameters, representing substrate doping (NSUBC), pocket-implantation doping (NSUBP), carrier-mobility degradation due to gate-interface roughness (MUESR1) and channel-length variation during the gate formation (XLD) are found sufficient to quantitatively reproduce the measured macroscopic within-wafer variations of V_{th} and I_{on} for all channel length L_g and all technology generations. Quantitative improvements from 180 nm to 65 nm are confirmed to be quite large for MUESR1 (about 70%) and $L_{\min}$(XLD) (55%) variations, related to the gate-oxide interface and the gate-stack structuring, respectively. On the other hand, doping-related technology advances, which are reflected by the variation magnitudes of NSUBC (30%) and NSUBP (25%), are found to be considerably smaller. Furthermore, specific combinations of extreme microscopic parameter-variation values are able to represent the boundaries of macroscopic fabrication inaccuracies for V_{th} and I_{on}. These combinations are found to remain identical, not only for all L_g of a given technology node, but also for all investigated technologies with minimum L_g of 180 nm, 100 nm and 65 nm.

Keywords— compact model, fabrication inaccuracy, field-effect transistor, macroscopic, microscopic, potential at channel surface, silicon, within wafer.

1. Introduction

As the dimensions of metal oxide semiconductor field effect transistors (MOSFETs) are scaled down, the effects of microscopic fabrication inaccuracies due to process variations are increasingly affecting the macroscopic variation of MOSFET performances and turn out to be increasingly difficult to manage and mitigate [1]. Experimental and theoretical variation analysis is normally based on macroscopic MOSFET properties like threshold voltage V_{th} or on-current I_{on}. Determining the correlation of the macroscopic variation data with microscopic MOSFET properties, like doping concentrations, structure parameters or carrier mobility, has been always a difficult task. An important reason is that the standard V_{th}-based compact models for circuit simulation, like BSIM4 [2], don't provide a sufficiently physical correlation between macroscopic MOSFET performance and microscopic MOSFET parameters, so that numerical technology computer aided design (TCAD) software has to be applied for this purpose. One recent method for improving this situation is the application of predictive technology models (PTM) in combination with a V_{th}-based compact model [3], but having the predictability already included in the compact model is of course preferable. Many studies also focus on just one type of the macroscopic variation aspects like V_{th} [4], because a comprehensive analysis of several macroscopic-variation aspects is more difficult and hard to accomplish.

We report an analysis of V_{th} and I_{on} variations over 3 process generations and verify that microscopic variations can be extracted by applying surface-potential compact models like Hiroshima University STARC IGFET model 2 (HiSIM2) [5], [6], which are presently in the process of being brought into industrial application. Only 4 microscopic parameters, which are related to substrate doping (NSUBC), pocket-implantation doping (NSUBP), gate-interface-roughness carrier-mobility degradation (MUESR1) and channel-length variation during gate structuring (XLD) are found sufficient to quantitatively reproduce within-wafer variation of V_{th} and I_{on} over all channel length (L_g) and all 3 technology generations with a minimum L_g of 180 nm, 100 nm and 65 nm. All of the 3 analyzed technologies apply a pocket-implantation technology for suppressing the performance degradations due to the short-channel effects and are chosen from different manufactures to obtain a more general picture of the technology trends.

2. Surface-Potential Compact Models

A new generation of compact models for circuit simulation, like HiSIM2 [5], [6] or PSP [7], uses a model concept

based on the surface-potential ϕ_S in the MOSFET channel below the gate oxide and incorporates the complete drift-diffusion theory for the MOSFET device [6], [8]. These surface-potential compact models replace the regional approach of V_{th}-based models like BSIM4 with a single equation, which is valid for all operating conditions and whose parameters have a close correlation to the structural and physical MOSFET parameters.

For example, the V_{th} variation due to the substrate doping NSUBC (called NDEP in BSIM4) of a long and wide MOSFET, depicted for BSIM4 and HiSIM2 in Fig. 1,

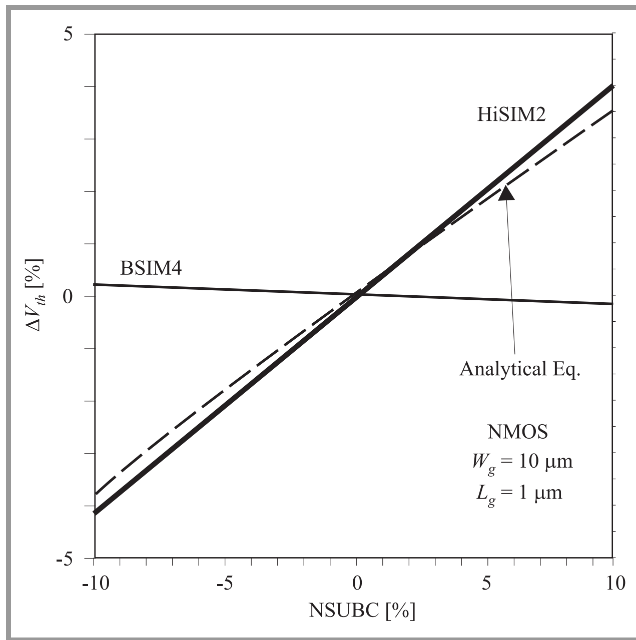


Fig. 1. Comparison of V_{th} as a function of substrate impurity variations for a long and wide MOSFET as predicted by the surface-potential model HiSIM2 and by the threshold-voltage-based model BSIM4 for a 100 nm technology. The result with the conventional analytical V_{th} equation, which neglects the pocket-implantation contributions, is also shown by a dashed line.

with model parameters extracted from a 100 nm CMOS technology, is obviously not correctly reproduced by the V_{th}-based model BSIM4. On the other hand, HiSIM2 is close to the standard analytical solution with a slight deviation explained by the fact that the analytical solution neglects the pocket implantation. Correct scaling properties of the HiSIM2 model parameters are confirmed with 3 wafers fabricated in the same 100 nm process, but with deliberately different substrate doping.

Figure 2 verifies, that the extraction of HiSIM2 parameters from the typically-implanted wafer's (wafer CCC) nominal chip is sufficient to predict the $I_{on} - V_{th}$ characteristics of the 2 differently implanted wafers, namely wafer FFC with reduced substrate doping and wafer SSC with increased substrate doping, by only adjusting the respective parameter NSUBC in the HiSIM2 model appropriately. This predictability of MOSFET characteristics through adjustment of the correlated physical parameter is even true for current derivatives with respect

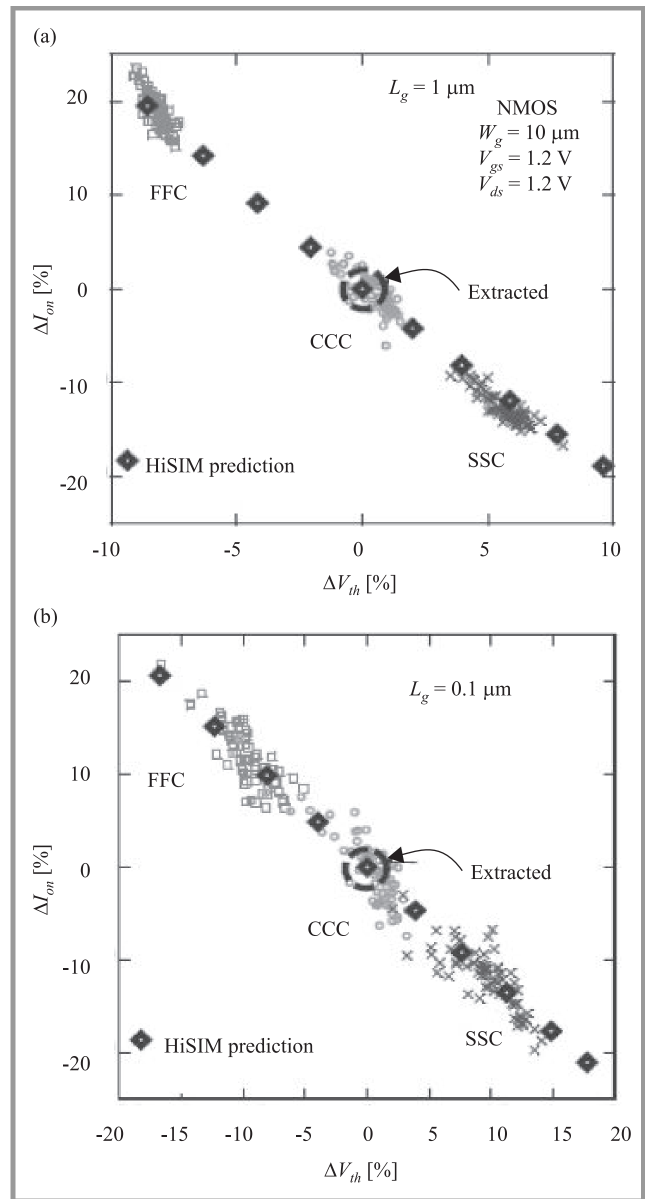


Fig. 2. Prediction of the inter-wafer variations of V_{th} and I_{on} due to the microscopic variation of the substrate doping (NSUBC) with the surface-potential-based compact model HiSIM2 for $L_g = 1\ \mu$m (a) and for $L_g = 0.1\ \mu$m (b). Measurements are shown by square symbols (wafer FFC with reduced substrate doping), circle symbols (wafer CCC with typical substrate doping) and cross symbols (wafer SSC with increased substrate doping), respectively. The model parameter extraction has been performed for the chip denoted by "extracted" from the wafer denoted by CCC. The large black symbols are calculated results with the surface-potential model HiSIM2 by only varying the NSUBC parameter in the extracted model card of parameters.

to V_{gs} (called transconductance g_m) or V_{ds} (called output conductance g_{ds}) as verified in Fig. 3 for the transconductance g_m.

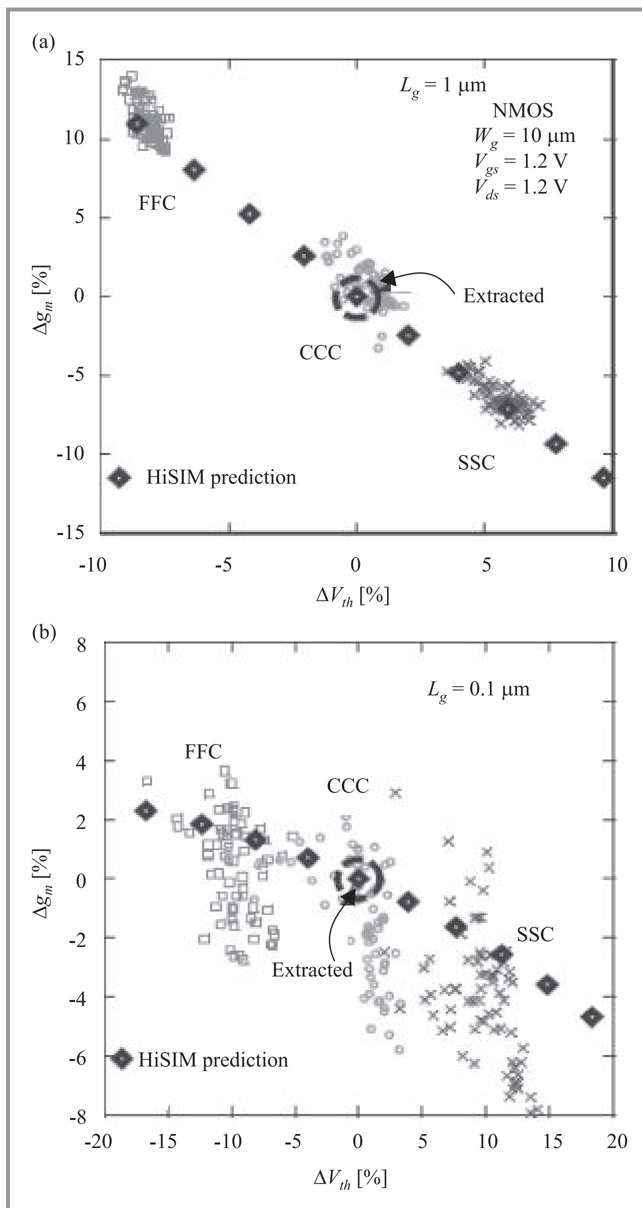


Fig. 3. Comparison of predicted and measured transconductance g_m variations on 3 different wafers (FFC, CCC, and SSC) with different substrate impurity concentrations (modeled with the parameter NSUBC) for $L_g = 1\ \mu$m (a) and $L_g = 0.1\ \mu$m (b). The meanings of the symbols are the same as in Fig. 2. These data verify the predictive capabilities of the surface-potential-based compact model HiSIM2 even for the inter-wafer variations of the V_{gs} derivatives of macroscopic $I-V$ characteristics of the MOSFET.

3. Sensitivity of Model Parameters and Variation-Extraction Method

For correlating the macroscopic variation of the MOSFET characteristics to the microscopic physical MOSFET parameters of the surface-potential model, it is necessary to determine those parameters which most sensitively influence the MOSFET characteristics.

Figure 4 shows the parameter-sensitivity analysis of simulated V_{th} and I_{on} for an 180 nm technology. The results

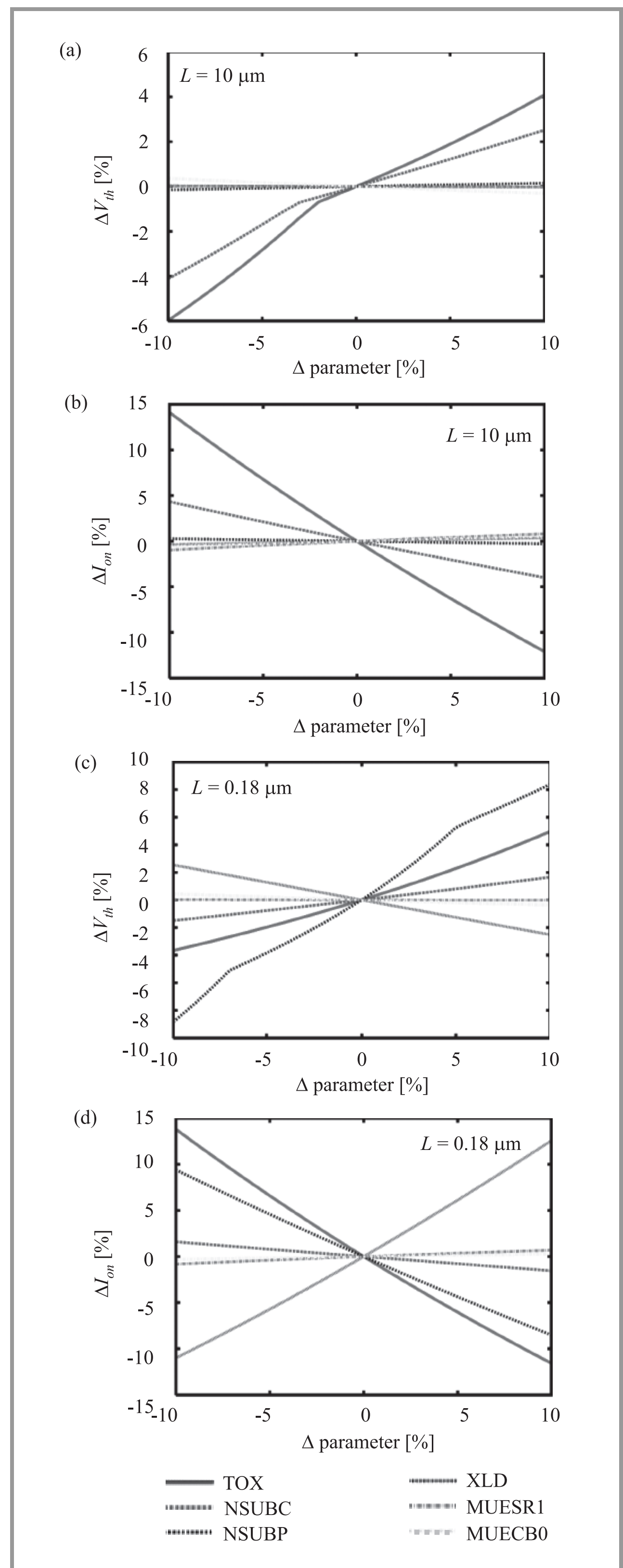


Fig. 4. Sensitivity of surface-potential model parameters for the threshold voltage V_{th} (a), (c) and the on-current I_{on} (b), (d) of NMOSFETs fabricated in a 180 nm CMOS technology. The most sensitive parameters are different for MOSFETs with long channel length $L_g = 10\ \mu$m (a), (b) and short channel length $L_g = 0.18\ \mu$m (c), (d).

for NMOSFETs with long channel lengths ($L_g = 10\ \mu$m) and short channel length ($L_g = 0.18\ \mu$m) are listed in Fig. 5 and show a large TOX sensitivity in all cases. However, the other sensitive parameters are different for $L_g = 10\ \mu$m (NSUBC, MUESR1, MUECB0) and $L_g = 0.18\ \mu$m (XLD, NSUBP). For the average oxide thickness (determining variation of TOX) and the substrate-lattice quality (determining the variation of MUECB0), process control during fabrication is known to be very good. In particular, the average TOX variation within a wafer is usually kept much smaller than an atomic layer, which means that variations of the properties of the gate-oxide interface can be expected to be of main importance in practice. Therefore, we first restrict the variation analysis of the microscopic parameters to the other 4 parameters NSUBC, MUESR1, NSUBP and XLD, to see whether this is already sufficient for reproducing the measured macroscopic V_{th} and I_{on} variations on the basis of the microscopic parameters in the HiSIM2 compact model.

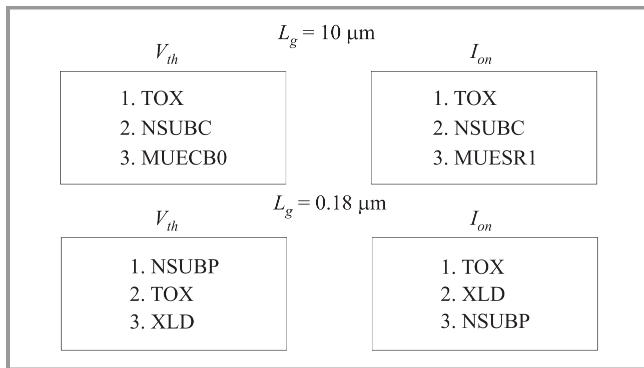
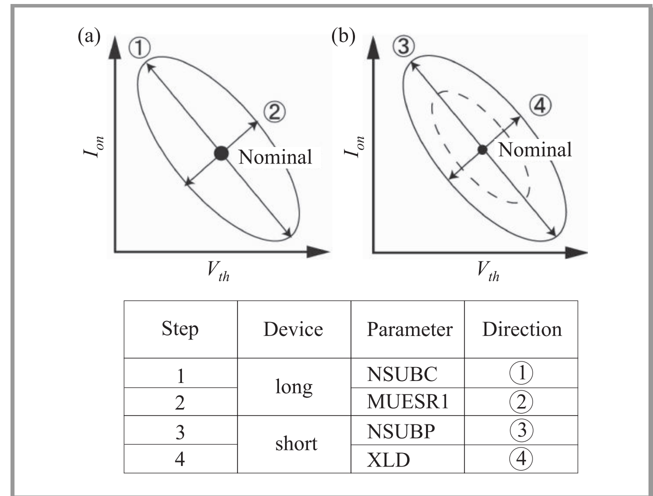


Fig. 5. Most sensitive model parameters from the sensitivity analysis of Fig. 4. The sensitivity with respect to gate-oxide thickness (TOX) is large in all cases. Other sensitive parameters are different for long channel ($L_g = 10\ \mu$m) and short channel ($L_g = 0.18\ \mu$m) MOSFETs. For $L_g = 10\ \mu$m, substrate doping (NSUBC) as well as the mobility parameters for phonon scattering (MUECB0) and surface roughness (MUESR1) are sensitive. For $L_g = 0.18\ \mu$m, the pocket doping (NSUBP) and the fabrication-process-related channel-length change (XLD) in comparison to the designed channel length are sensitive.

For carrying out the extraction procedure of microscopic variations, a typical die is first selected based on the condition that MOSFETs on this die occupy a central position in the measured $I_{on} - V_{th}$ variation for all channel length L_g. Then a nominal HiSIM2 reference-parameter set is extracted, which reproduces the $I - V$ characteristics of the MOSFETs on this selected die for all L_g. The variation of microscopic HiSIM2 parameters with respect to this nominal parameter set is then determined from the measured within-wafer $I_{on} - V_{th}$ variation data according to the 4-step procedure of Fig. 6. Taking into account the L_g-dependence of the respective sensitivities and their influence on the distribution shape, the microscopic variations are first determined for NSUBC and MUESR1 form the long L_g data and then for NSUBP and XLD from the short L_g data. By applying this method, changes in the effective channel doping concentration and the effective



Step	Device	Parameter	Direction
1	long	NSUBC	①
2		MUESR1	②
3	short	NSUBP	③
4		XLD	④

Fig. 6. Extraction strategy of the microscopic parameter variation from the measured macroscopic V_{th} and I_{on} variation data. As the process control is very good for oxide thickness and phonon scattering, these 2 parameters are assumed to have negligible influence on macroscopic variation and a 2 step procedure for extracting the variation of the other sensitive parameters is applied. In the first step the variation of substrate doping (NSUBC) and surface roughness (MUESR1) are determined from the long-channel data (a). In the second step the short-channel data (b) are used to extract the variation of pocket doping (NSUBP) and fabrication related channel-length change (XLD).

mobility degradation as a function of L_g in comparison to their long L_g values, represented by the NSUBC and MUESR1 variations, are correctly captured with the surface-potential model HiSIM2.

4. Microscopic-Variation Extraction for 3 Technology Generations

The microscopic within-wafer parameter variations of NMOSFETs for the 180 nm, 100 nm and 65 nm technology generations have been analyzed according to the method described in Section 3. A nominal die of each wafer has been selected for each technology generation, based on the condition that the MOSFETs on this die occupy a central position (determined by the median values) in the measured $I_{on} - V_{th}$ variation for all L_g. The HiSIM2 reference-parameter set has then been obtained from a fit to the electrical MOSFET characteristics on this selected die. The fitting results of the $I - V$ characteristics of the 100 nm technology are shown for long and short channel length L_g in Fig. 7 as an example for the good reproduction of the nominal electrical MOSFET characteristics. With this reference-parameter set, the variation of microscopic parameters has then been deter-

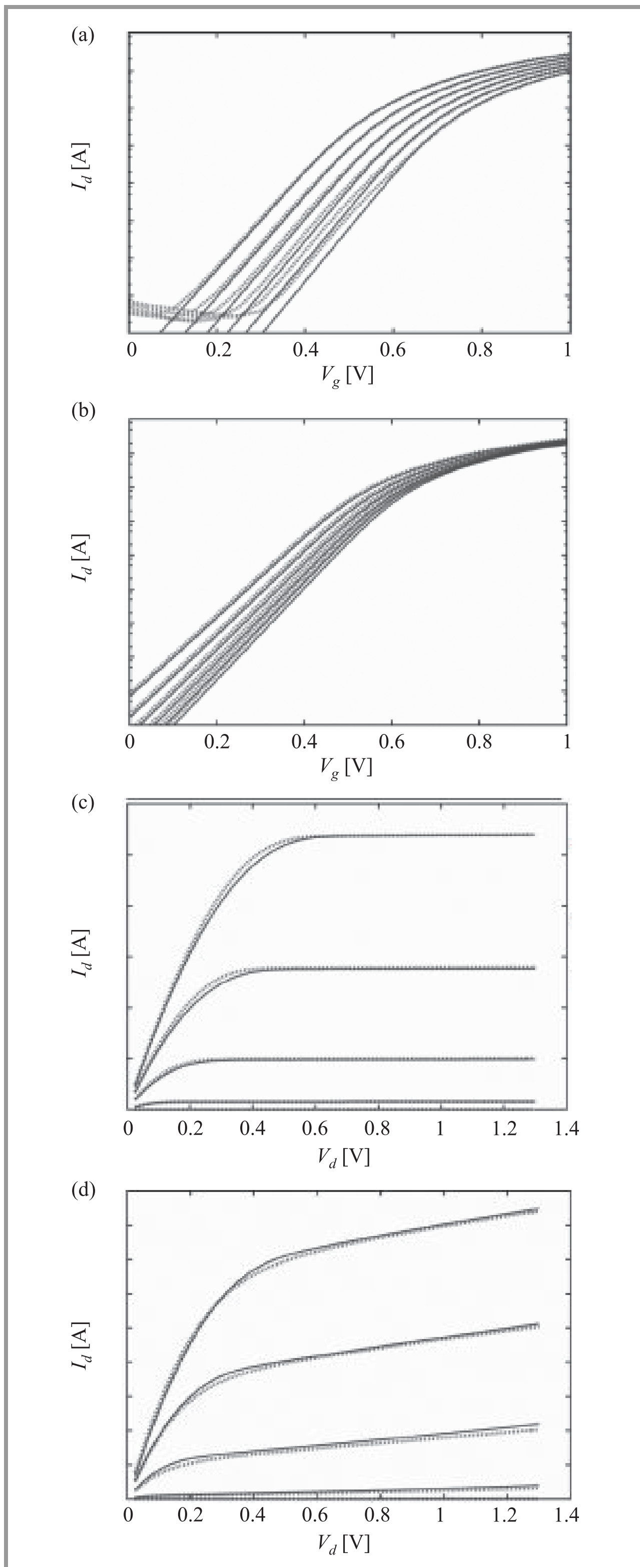
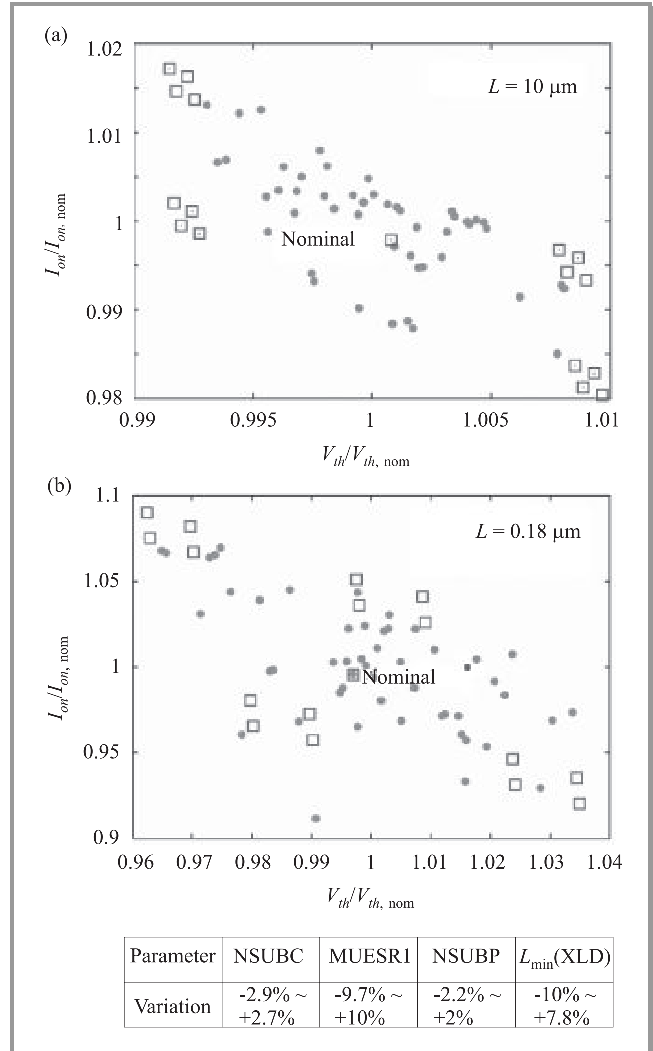


Fig. 7. Example of the parameter extraction results for the selected nominal MOSFET of the analyzed 100 nm CMOS technology by fitting the parameters of the surface-potential model HiSIM2 so that the measured $I-V$ data (solid lines) are accurately reproduced by the simulated data with the compact model (dotted lines). $I_d - V_g$ plots are on logarithmic scale for long L_g in (a), short L_g in (b) and on linear scale for long L_g in (c), short L_g in (d).

mined from the measured within-wafer $I_{on} - V_{th}$ variation according to the 4-step procedure of Fig. 6 as explained in the previous section.

The extracted microscopic variations are shown in Figs. 8, 9, and 10 for the 180 nm, 100 nm, and 65 nm technologies, respectively.

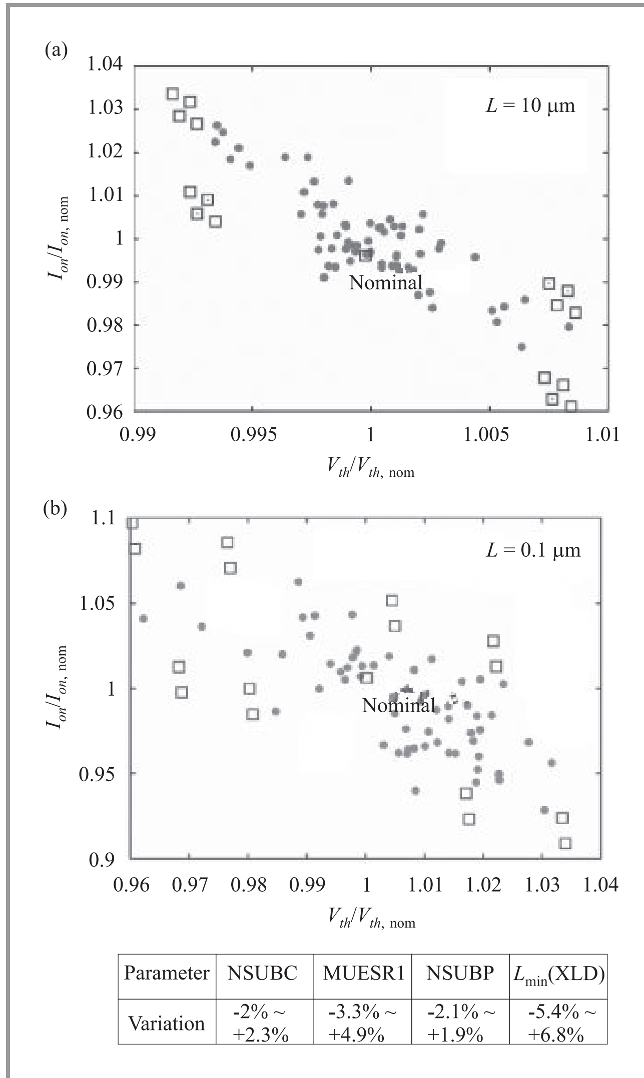


Parameter	NSUBC	MUESR1	NSUBP	L_{min}(XLD)
Variation	-2.9% ~ +2.7%	-9.7% ~ +10%	-2.2% ~ +2%	-10% ~ +7.8%

Fig. 8. Variation extraction of the most sensitive microscopic parameters for the NMOSFETs of a 180 nm technology applying the pocket implantation. Data points in the $I_{on} - V_{th}$ graphs for long (a) ($L_g = 10$ μm) and short (b) ($L_g = 0.18$ μm) MOSFETs are plotted on a scale relative to the selected nominal measured devices. Points show measured data and open squares show the nominal compact model data as well as all 16 combinations of the variation boundaries for the microscopic parameters.

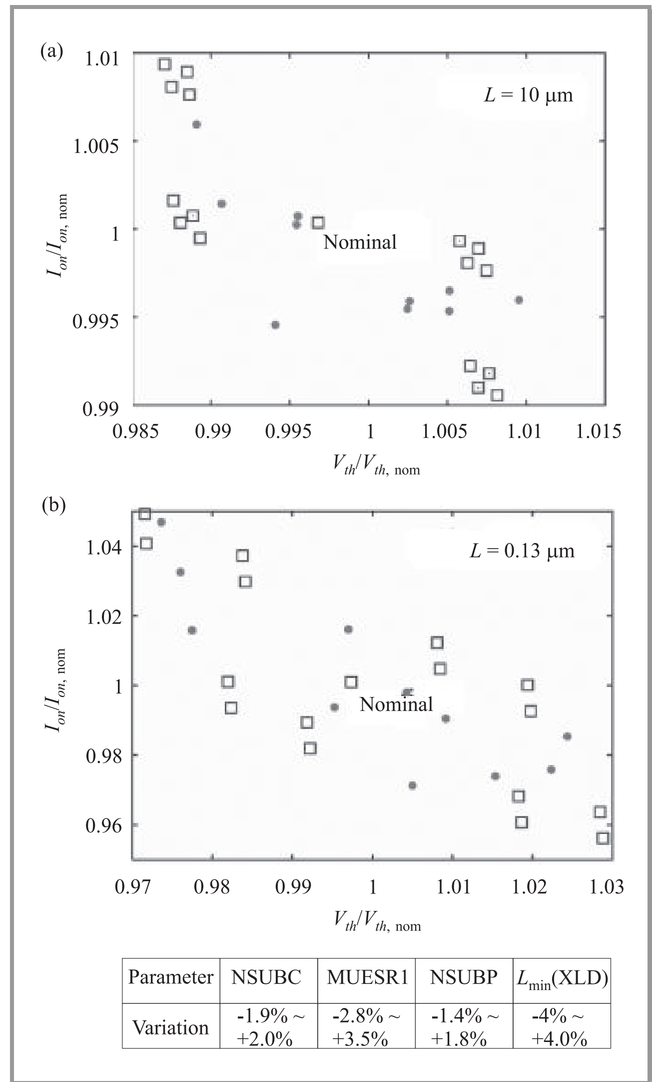
Asymmetric properties of the variation boundaries reflect the systematic component of the within-wafer variation across the wafer. Although only measured transistors down to 130 nm were available for the 65 nm technology, this has no practical negative influence on the accuracy of the extracted microscopic parameter variations of this technology. The 2 graphs in each figure are plotting measured long and short-channel data for

$I_{on} - V_{th}$ variations (points) together with simulated data for the nominal parameter set and the 16 extreme combinations of the microscopic-parameter variations (open squares).



Parameter	NSUBC	MUESR1	NSUBP	L_{min}(XLD)
Variation	-2% ~ +2.3%	-3.3% ~ +4.9%	-2.1% ~ +1.9%	-5.4% ~ +6.8%

Fig. 9. Variation extraction of the most sensitive microscopic parameters for the NMOSFETs of a 100 nm technology applying the pocket implantation. Data points in the $I_{on} - V_{th}$ plots for long (a) ($L_g = 10\ \mu$m) and short (b) ($L_g = 0.1\ \mu$m) MOSFETs are plotted in the same manner as in Fig. 8.



Parameter	NSUBC	MUESR1	NSUBP	L_{min}(XLD)
Variation	-1.9% ~ +2.0%	-2.8% ~ +3.5%	-1.4% ~ +1.8%	-4% ~ +4.0%

Fig. 10. Variation extraction of the most sensitive microscopic parameters for the NMOSFETs of a 65 nm technology applying the pocket implantation. Data points in the $I_{on} - V_{th}$ plots for long (a) ($L_g = 10\ \mu$m) and short (b) ($L_g = 0.13\ \mu$m, which was the smallest measured device) MOSFETs are plotted in the same style as in Fig. 8.

Figures 8, 9, and 10 confirm good agreement between measured and simulated within-wafer variations and verify that the main sources of measured $I_{on} - V_{th}$ variations can be correlated to the microscopic variations of just 4 physical MOSFET properties over 3 technology generations from 180 nm to 65 nm, namely, to substrate and pocket doping concentrations (NSUBC, NSUBP), mobility degradation due to gate-oxide surface-roughness scattering (MUESR1), and channel-length variation due to gate-stack structuring (XLD).

Quantitative improvements of these microscopic parameter variations with the technological advances in each generation of advancing fabrication technologies are plotted in Fig. 11.

Improvements for MUESR1 (70%) and L_{min}(XLD) (55%), related to gate-oxide interface and gate-stack structuring have been quite large in the course of fabrication-technology advances. On the other hand, doping-related technology improvements, reflected by NSUBC (30%) and NSUBP (25%), have been considerably smaller. The average gate-oxide thickness TOX seems to be well controlled, to a level much below the atomic-layer thickness. On the other hand, gate-oxide-interface properties seem to be much more difficult to control. Consequently, the influence of gate-oxide roughness and charged interface traps on the inversion-layer carrier mobility, captured by MUESR1,

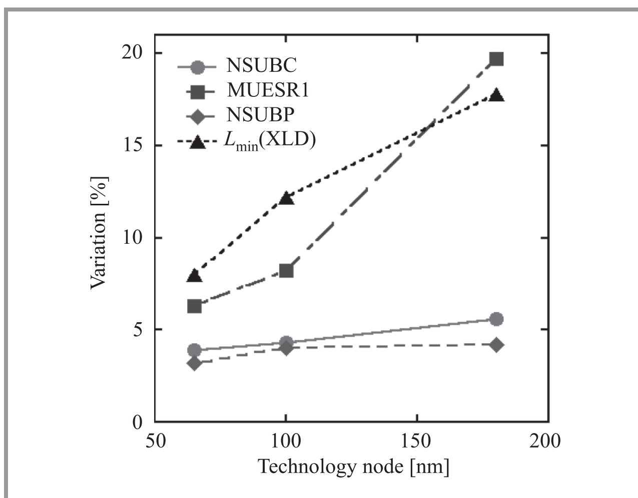


Fig. 11. Extracted variation trends of microscopic device parameters, which are most relevant for within-wafer variations of the macroscopic NMOSFET characteristics of threshold voltage V_{th} and on-current I_{on}, from the 180 nm to the 65 nm technology node.

remain substantial and reflect the variability effects due to the imperfect gate-oxide interface.

5. Conclusion

Surface-potential-based compact models can quantitatively correlate variations of macroscopic MOSFET-performance characteristics with microscopic variations of the physical MOSFET parameters. The most variation-sensitive microscopic parameters are substrate and pocket doping concentrations (NSUBC, NSUBP), the carrier-mobility degradation due to gate-oxide-surface roughness (MUESR1) and effective channel length due to the gate structuring (XLD). Quantitative analysis of $I_{on} - V_{th}$ variation data for NMOSFETs over technology nodes from 180 nm to 65 nm, applying the pocket-implantation technology, confirms that microscopic parameter variations have been continuously improved. The magnitude of these improvements could be extracted from the measured MOSFET-performance data, quantitatively amounting to 70%, 55%, 30% and 25% improvement for MUESR1, $L_{\min}$ (XLD), NSUBC and NSUBP, respectively. The gate-oxide thickness variation is found negligible for the within-wafer variation of I_{on} and V_{th}, but the effect of gate-oxide surface-roughness variations, including the effect of trapped charges, is found to be substantial.

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