Invited paper

Scattering mechanisms in MOS/SOI devices with ultrathin semiconductor layers

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Abstract — Main scattering mechanisms affecting electron transport in MOS/SOI devices are considered within the quantum-mechanical approach. Electron mobility components (i.e., phonon, Coulomb and interface roughness limited mobilities) are calculated for ultrathin symmetrical DG SOI transistor, employing the relaxation time approximation, and the effective electron mobility is obtained showing possible mobility increase relative to the conventional MOSFET in the range of the active semiconductor layer thickness of about 3 nm.

Keywords — ultrathin SOI, scattering mechanisms, electron mobility.

1. Introduction

Silicon devices based on the MOS structure are still the dominating group of semiconductor devices that are subjected to continuous technological progress – in terms of both dimension downscaling and modifying the basic structure of the device and/or developing new ones. The latter tendency is exemplified by silicon-on-insulator (SOI) technology, which is a growing up advantageous alternative to the conventional bulk CMOS technology. In addition to overcoming some of the drawbacks and limitations of the CMOS technology, the SOI concept gives direct entry to nanoelectronics, which is achieved in various forms of ultrathin SOI devices (especially in fully depleted single gate (SG) or double-gate (DG) SOI transistors) by decreasing the thickness of the semiconductor active layer far below 10 nm [1, 2]. Figure 1 shows schematically structural differences between conventional n-channel bulk MOS, SG SOI and DG SOI transistors.

Since transport properties of charge carriers determine their mobility and the overall current – voltage behavior of the device, scattering processes are of special interest when modeling the device operation. Therefore channel carriers mobility models have been continuously developed for decades along with MOS technology growth, with main goals to reflect the actual/measured device performance as well as to investigate the physical phenomena experienced by carriers in the channel area. The physical approach is particularly important since it allows for better understanding of the device operation and is necessary if one wants to make reliable predictions when changing the device operation conditions and/or its configuration, as is the case with the transition from the conventional CMOS to SOI technology.

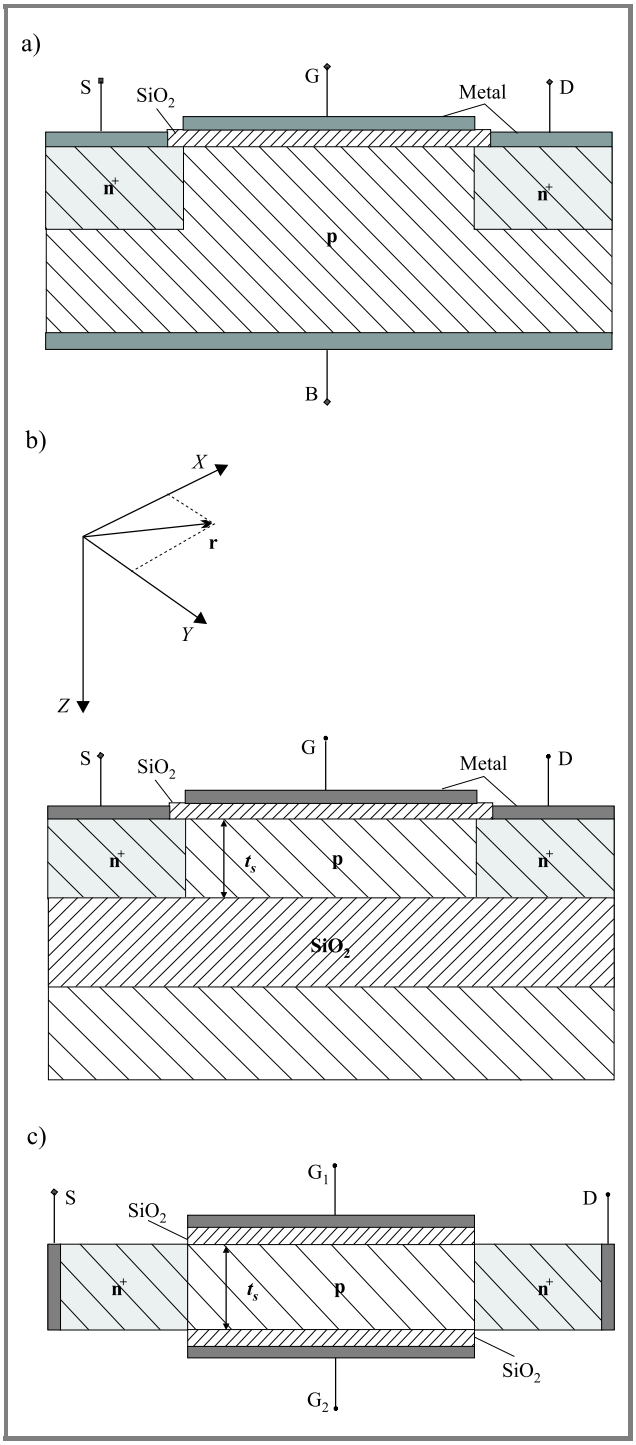

Fig. 1. Schematic cross-sections of (a) bulk MOS, (b) SG SOI and (c) DG SOI transistors.

Because in MOS transistors carriers are spatially confined within a near-surface layer of very small thickness (tens of nanometers), quantum-mechanical effects occur affecting the spatial distribution of the carriers and imposing quantization of their energy [3, 4]. Therefore one of the milestones in MOS transport modeling was the inclusion of the quantum-mechanical phenomena into the device theory after which one could distinguish between "classical" and "quantum-mechanical" descriptions.

Whereas the "classical" approach based on the solution to the Poisson's equation alone was acceptable to a certain extent when modeling the conventional bulk MOS transistors, the quantum-mechanical approach is rigorously imposed in the case of SOI devices with ultrathin active layers and solution to the Schrödinger equation must be included self-consistently with that to Poisson's equation. In the nanometric range of the active layer thickness, quantum effects determine the behavior of the SOI device and substantial differences arise between the bulk MOSFETs and ultrathin SOI transistors with respect to potential and carriers distributions, as well as the dynamics of scattering mechanisms, which additionally depend now on the semiconductor thickness [5–8].

In this paper we present some aspects of scattering processes in MOS/SOI transistors following the quantum-mechanical modeling approach and concentrating on electron mobility in ultrathin n-channel symmetrical double-Al-gate SOI transistors with uniform substrate doping. The main mechanisms, i.e. the phonon, Coulomb and interface roughness scattering, limiting the channel electron mobility, will be discussed briefly, pointing out the most important differences between the cases of bulk NMOSFETs and ultrathin DG SOI devices, as well as showing the influence of the semiconductor thickness variation. The scattering rates will be obtained and analyzed within the perturbation theory after obtaining the self-consistent solution within the effective mass approximation. Next, electron mobilities corresponding to particular scatterers will be obtained utilizing the relaxation time approximation, and eventually the effective electron mobility will be assembled and plotted vs. the transverse effective field in the channel.

2. Two-dimensional electron gas (2DEG) in MOS/DG SOI transistor channel

As already mentioned, the spatial confinement of electrons within a very narrow layer of MOSFET as well as SOI transistor channel area, defined in terms of energy by the potential energy barrier of Si/SiO_2 interface and the conduction band bottom, results in quantization of kinetic energy corresponding to motion in the direction z perpendicular to the surface. The total electron kinetic energy wave vector relationship near the energy band minimum may be approximated as:

$$E(\mathbf{k}) = E_i + \frac{\hbar^2 k_x^2}{2m_x} + \frac{\hbar^2 k_y^2}{2m_y} \tag{1}$$

being a set of energy subbands with discrete minima E_i and quasi-continuous energies of motion in the two remaining directions (x,y) parallel to the surface (hence the 2DEG term). Moreover, the electron spatial distribution within the potential well follows now quantum-mechanical principles and is defined by envelope wave functions $\xi_i(z)$. Assuming that the potential energy $V(z)$ varies in the z direction only, the eigenstates $(E_n, \xi_n(z))$ may be obtained by the solution to the system of Poisson's and the time-independent Schrödinger one-dimensional equations:

$$\frac{d^2\phi}{dz^2} = \frac{e}{\varepsilon_{Si}}\Big(N_A(z) + n(z) - p(z)\Big), \tag{2}$$

$$\left(-\frac{\hbar^2}{2m}\frac{d^2}{dz^2} + V(z)\right)\xi_i(z) = E_i\xi_i(z) \tag{3}$$

along with the equations describing the electron distribution $n(z)$ and the number of electrons N_i in each subband:

$$n(z) = \sum_i N_i\big|\xi_i(z)\big|^2 + \sum_i N_i'\big|\xi_i'(z)\big|^2, \tag{4}$$

$$N_i = \frac{n_v m_d K_B T}{\pi\hbar^2}\ln\left(1 + \exp\left(\frac{E_{Fn} - E_i}{K_B T}\right)\right). \tag{5}$$

Because of the conduction band energy minima configuration in **k**-space (Fig. 2), one obtains two series of eigenstates when the $Si\text{-}SiO_2$ interface is the (100) plane – the first one (nonprimed) corresponding to twofold valleys of the effective mass in the quantization direction $m = m_l = 0.916\, m_0$ and the second one (primed) corresponding to fourfold valleys of the effective mass in the quantization direction $m = m_t = 0.19\, m_0$.

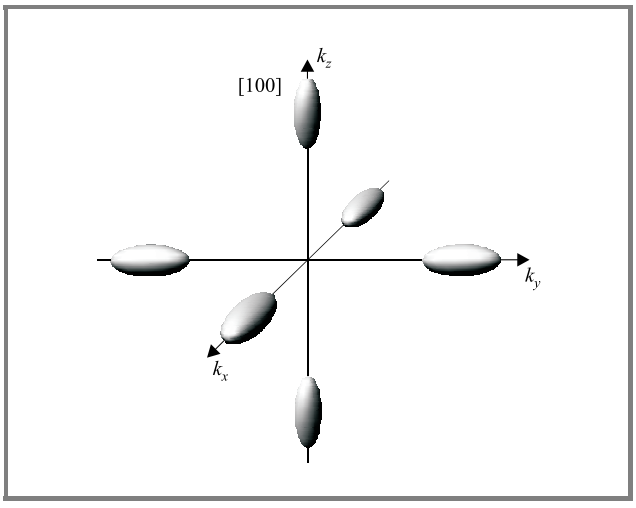

Fig. 2. Constant energy surfaces ($E(\mathbf{k}) = \text{const}$) in the vicinity of the silicon conduction band minima.

In this paper we assume infinite potential barrier height at the SiO_2-Si interface, which is a common practice. In other words we do not consider here a possible penetration of electron wave functions into the dielectric layer. Figures 3 and 4 show examples of the distributions of energy levels and eigenfunctions obtained within this approximation for both the conventional bulk NMOS and DG SOI transistors, respectively. The envelope functions have been scaled for illustration purposes, since:

$$\int_0^\infty \left|\xi_i(z)\right|^2 dz = 1\,. \tag{6}$$

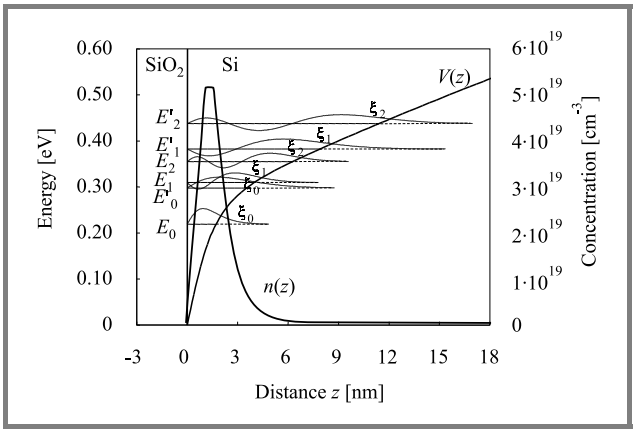

Fig. 3. Energy diagram of a bulk NMOS transistor ($T = 300$ K, $N_A = 10^{17}$ cm^{-3}, $t_{ox} = 3$ nm, $V_{GS} = 1.8$ V, $V_{FB} = -0.922$ V, Al- gate).

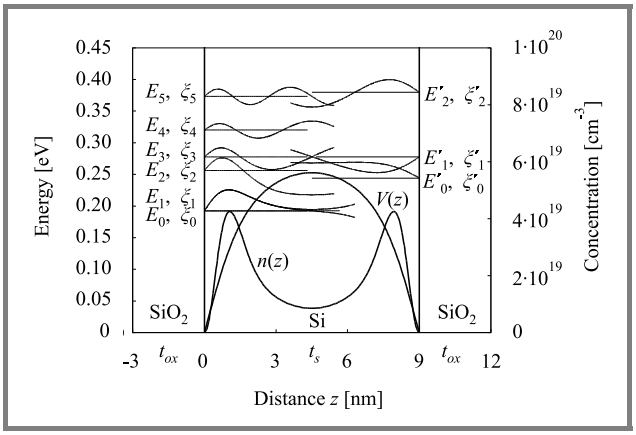

Fig. 4. Energy diagram of a symmetrical DG SOI transistor ($T = 300$ K, $N_A = 10^{17}$ cm^{-3}, $t_{ox} = 3$ nm, $t_{ox} = 9$ nm, $V_{GS} = 1.5$ V, $V_{FB} = -0.922$ V, Al- gates).

The difference between the m_l and m_t effective masses results in a split between the nonprimed and primed series in the energy scale and hence leads to different electron occupation of the corresponding energy subbands. Moreover, the density of states masses differ for both series since $m_{d2} = m_t = 0.19 \cdot m_0$ for the twofold valleys, while $m_{d4} = (m_l \cdot m_t)^{1/2} = 0.417 \cdot m_0$ for the four-fold valleys, and the corresponding average conduction effective masses are: $m_{c2} = 0.19 \cdot m_0$, $m_{c4} = 2/(1/m_l + 1/m_t) \approx 0.315 \cdot m_0$. These differences will strongly affect the resultant transport properties.

The substantial difference between the bulk MOS and the symmetrical DG SOI structure in terms of quantum effects is the channel potential well shape. In the former case the potential well is triangle-like, while in the latter it may be additionally affected by the bias applied to both gates, as well as the thickness of the semiconductor layer. Volume inversion occurs in ultrathin structures of DG SOI, meaning that the inversion charge distribution centroid moves towards the center of the structure.

3. Theoretical approach

In this paper we focus on the main, usually considered scattering mechanisms, i.e. the phonon, Coulomb and interface roughness scattering, since these are believed to influence the device performance to the highest extent at room temperatures [4, 9, 10]. We do not consider here neither high-energy nor ballistic transport problems.

Scattering processes are typically analyzed and modeled within the perturbation theory treating a scattering mechanism as a source of perturbation energy $\mathbf{H}'$ introduced into the regular periodic potential of the lattice, which generates transitions of carriers between different quantum states. According to this approach, the transition probability per unit time between the initial and final states φ_i and φ_f, is given in a general form by the Fermi Golden Rule:

$$P_{fi} = \frac{2\pi}{\hbar}\left|M_{fi}\right|^2 \delta\Big(E_f - \big(E_i \pm \hbar\omega\big)\Big), \tag{7}$$

where the matrix element M_{fi} depends on a particular scatterer and is defined as:

$$M_{fi} = \int d^3 r \varphi_f^* \mathbf{H}' \varphi_i. \tag{8}$$

The δ-function in (7) corresponds to the energy conservation law including the energy absorption/emission in the case of inelastic scattering (e.g. with optical phonons), as well as no energy exchange in the case of elastic scattering when $\hbar\omega \approx 0$ (e.g. scattering by low-energy acoustic modes, Coulomb centers and interface roughness). Electron transitions in silicon conduction band may be additionally divided into intravalley scattering processes and intervalley scattering processes, depending on the target valley. Intervalley scattering involves relatively high transition wave vectors and is mainly assigned to optical phonons and high-energy acoustic phonons.

Furthermore, intrasubband and intersubband transitions may be defined in the case of 2DEG in the MOS/SOI type transistor channel. An example of a transition scheme between the initial electron wave vector $\mathbf{k}$, the final wave vector $\mathbf{k}'$ and the scattering wave vector $\mathbf{q}$ is shown in Fig. 5 for an intersubband elastic transition.

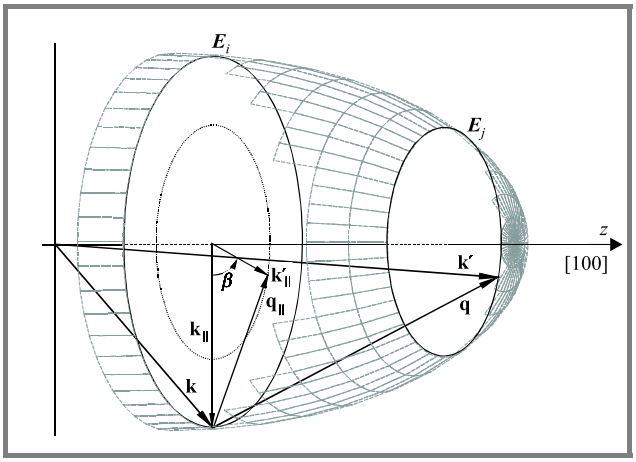

Fig. 5. Illustration of wave vector exchange in 2DEG.

As opposed to a three-dimensional case, the momentum conservation law in the above 2DEG system is fulfilled only for momentum components parallel to the surface being the plane of the considered transport, or in other words, for the components perpendicular to the direction of quantization:

$$\mathbf{k}'_{||} = \mathbf{k}_{||} \pm \mathbf{q}_{||}\,. \tag{9}$$

One can define the energy dependent rate $1/\tau_{ij}(E)$ of scattering by a given scattering mechanism for transition between subbands i and j by adding all possible final states $\mathbf{k}'$. Similarly, the total scattering rate $1/\tau_i(E)$ associated with the ith subband is determined by adding transitions into other subbands including intrasubband transitions ($i = j$) and taking into account intervalley transitions by the application of the corresponding valley degeneration factors.
Having the scattering rates, the Boltzmann equation may be solved and electron mobility may be obtained either by means of a precise full Monte Carlo analysis or within much simpler relaxation time approximation. We follow the second approach believing that in terms of the basic scattering mechanisms it reflects the mobility behavior well enough to recognize the most significant trends. Thus, we calculate ith subband mobility for a given scatterer:

$$\mu_i = \frac{e}{m_{ci}}\langle\tau_i\rangle \tag{10}$$

by averaging the subband relaxation times over the energy distribution:

$$\langle\tau_i\rangle = \frac{\sum\limits_{\mathbf{k}} E(k)\tau_i\big(E(k)\big)\Big(-\frac{\partial f}{\partial E(k)}\Big)}{\sum\limits_{\mathbf{k}} E(k)\Big(-\frac{\partial f}{\partial E(k)}\Big)}. \tag{11}$$

Then, the average rth-scattering mechanism limited mobility is calculated depending on the relative subband occupation:

$$\mu_r = \frac{\sum\limits_i \mu_{r,i} N_i}{N_{inv}}\,, \tag{12}$$

where N_{inv} denotes the inversion charge density. Finally, the total effective electron mobility due to considered scattering mechanisms may be derived by applying Matthiessen's rule:

$$\frac{1}{\mu_{eff}} \approx \frac{1}{\mu_{ph}} + \frac{1}{\mu_{imp}} + \frac{1}{\mu_{sr}} \tag{13}$$

and expressed as a function of effective transverse electric field defined as:

$$E_{eff} = \frac{\int\limits_0^{Z_f} n(z)\big(\partial\phi(z)/\partial z\big)dz}{\int\limits_0^{Z_f} n(z)dz}\,, \tag{14}$$

where Z_f is the integration range equal to $Z_f = \infty$ for MOSFET and $Z_f = t_s/2$ for the symmetrical DG SOI structure.

4. Phonon scattering

Due to lattice vibrations, which occur even at 0 K, phonon scattering is an inherent mechanism limiting electron mobility and is of particular importance at room temperature. This type of scattering is described as collisions between electrons and the vibrating lattice during which the lattice energy quantum $\hbar\omega_{\mathbf{q}}$ (a phonon) and quasi-momentum $\hbar\mathbf{q}$ transfer occurs. Phonons are believed to cause local perturbations of the band structure affecting the electron transport. This effect is conventionally described within the deformation potential approximation. Because of relatively small energies of long wavelength acoustic phonons, electron transitions induced by those phonons are typically treated as elastic and are believed to be mainly intravalley processes.
For the z-direction momentum components, the conservation law is not fulfilled (see Eq. (9)). Instead, the matrix element depends on the form-factor [11]:

$$\mathrm{I}_{ij}(q_z) = \int\limits_0^{\infty} \xi_i(z) e^{iq_z z}\xi_j(z)dz\,. \tag{15}$$

We stay here within frequently used energy equipartition and isotropic approximations applying effective deformation potential Ξ_{eff} value, irrespective of the phonon wave vector direction [12, 13]. In such a case, the following identity is utilized:

$$\frac{1}{2\pi}\int\limits_{-\infty}^{\infty}\Big|\mathrm{I}_{ij}(q_z)\Big|^2 dq_z \equiv \int\limits_0^{\infty}\xi_i(z)^2\xi_j(z)^2dz = F_{ij} \tag{16}$$

and the ith subband intravalley scattering rate is obtained:

$$\frac{1}{\tau_i(E)} = \frac{K_B T}{\hbar^3\rho u^2}\sum_j \theta\big(E - E_j\big)m_d\Xi_{eff}^2 F_{ij}\,, \tag{17}$$

where ρ is crystal density, u – sound velocity, and $\theta(E)$ is the step function.

Similarly, deformation potential constants D_r and phonon energies E_r are defined for intervalley transitions of different types – g transitions between parallel valleys and f transitions between perpendicular valleys. The corresponding intervalley scattering rate is given by:

$$\frac{1}{\tau_i(E)} = \sum_r \frac{n_v (D_r)^2 m_d}{\hbar \rho E_r} \begin{pmatrix} n_r \\ n_r + 1 \end{pmatrix} \sum_j \theta\left(E \pm E_r - E_j\right) F_{ij}\,, \tag{18}$$

where n_r denotes a number of rth type phonons and n_v is the degeneracy factor of the final valleys.

The upper/lower symbols correspond to phonon absorption/emission. The deformation potentials are still a matter of investigation and are taken as empirical or fitting parameters [13, 14]. Here we utilize typical phonon parameters [15] (Table 1).

Table 1
Phonon parameters

Phonon type	Energy E_r [meV]	Deformation constant D_r [10^8 eV/cm]
f_1	19	0.3
f_2	47.5	2.0
f_3	59.1	2.0
g_1	12.1	0.5
g_2	18.6	0.8
g_3	62.2	11.0
Acoustic deformation potential Ξ_{eff} [eV]		12.0

Following the theory outlined above, we have determined phonon limited mobility of electrons for conventional bulk NMOS transistor and DG SOI transistor, varying the active semiconductor layer thickness. The results were then plotted in Fig. 6 as a function of the effective field.

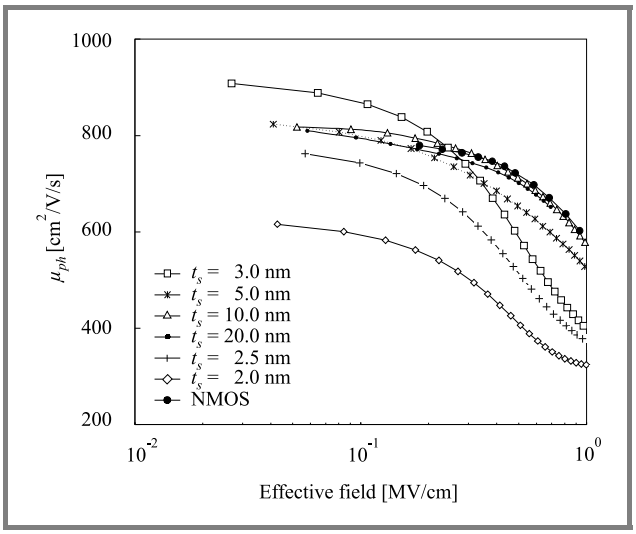

Fig. 6. Phonon mobility for NMOS (black dots) and DG SOI transistor for different values of the semiconductor thickness.

One can observe that the obtained phonon-limited mobility values are generally smaller for DG SOI than for NMOS except for a particular semiconductor thickness, about 3 nm, and in the range of lower fields. This tendency in mobility behavior may be better seen when plotted as a function of the semiconductor thickness (Fig. 7).

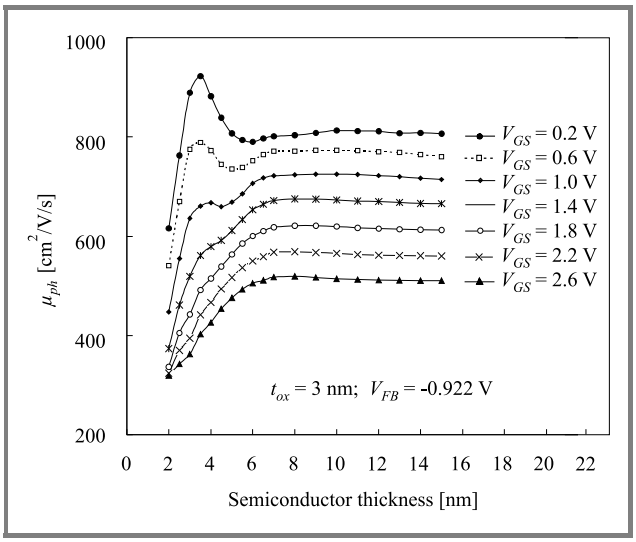

Fig. 7. Phonon-limited mobility of electrons in DG SOI transistor vs. semiconductor thickness t_s for different gate voltage biases ($t_{ox} = 3$ nm).

Here, it can be seen that the calculated phonon-limited mobility reaches a local maximum at the semiconductor thickness of about 3 nm and for low gate voltages. The maximum decreases then gradually with increasing gate voltage and finally vanishes, following the general trend. The phonon-limited mobility decrease for ultrathin SOI relative to the bulk NMOSFET values results from stronger spatial confinement of carriers, which is a direct consequence of the semiconductor thickness decrease for the SOI case. The confinement broadens the electron wave function spectrum in the direction z allowing for the interaction with a wider range of phonons, which increases the coefficient (16). The other observed tendency, i.e. the mobility increase for $t_s \approx 3$ nm, is the effect of relative subband configuration/occupation which, for the case of DG SOI, favors the nonprimed series of lower density-of-states and conduction masses when decreasing the semiconductor thickness and/or the gate voltage bias. Thus, the two counteracting effects determine the resultant phonon-limited electron mobility in ultrathin DG SOI transistor, giving a range of the semiconductor thickness and the gate voltage values where some increase of the mobility may be predicted.

5. Coulomb scattering

This type of scattering is associated with the presence of electrostatic centers affecting the motion of channel carriers. The scatterers are believed to be mainly impurity ions, interface states, charges in the oxide and the gate material.

Scattering potential of Coulomb centers is neutralized to some extent by free carriers, which modify their spatial distribution and screen the bare external scattering potential. Therefore, this screening effect substantially reduces the scattering strength, particularly in the range of higher inversion charge concentrations. Another phenomenon inherently connected with the electrostatic interaction between the scatterers and carriers in a MOSFET channel is the image potential induced due to a sandwich-like structure of the device consisting of several layers with different dielectric constants. Additional effects of Coulomb nature are predicted and investigated when scaling down device dimensions to the nanometric range, such as remote charge scattering, and a change of the image model is suggested [16].

Here we concentrate on the image charge effect and briefly report differences between the image potential influence on the impurity-ion-limited mobility in conventional MOS and DG SOI transistors [17].

Conventionally, semi-infinite SiO_2-Si layers are assumed and only one image charge $Q' = (\varepsilon_{Si} - \varepsilon_{ox})/(\varepsilon_{Si} + \varepsilon_{ox}) \cdot Q$ of a scattering center Q is taken into account in the MOSFET theory, optionally with an image charge due to the finite width of the space charge layer in the semiconductor [9].

In an ultrathin SOI structure, however, additional interfaces are present and the image charge model becomes more complicated. Let us assume semi-infinite oxide layers as a first approximation, which corresponds to the above-mentioned conventional MOS case. Due to the other Si-SiO_2 interface, the total image potential ϕ induced by an impurity ion Q present in the channel at coordinates $(\mathbf{r}_0, z_0)$ may be developed into an infinite series:

$$\phi(\mathbf{r}, z) = \frac{Q}{4\pi\varepsilon_{Si}} \left\{ \frac{\widetilde{\varepsilon}}{\left((\mathbf{r}-\mathbf{r}_0)^2 + (z+z_0)^2\right)^{\frac{1}{2}}} + \right.$$
$$+ \sum_{n=1} \left(\frac{\widetilde{\varepsilon}^{2n-1}}{\left((\mathbf{r}-\mathbf{r}_0)^2 + |z-(2nt_s - z_0)|^2\right)^{\frac{1}{2}}} + \right.$$
$$+ \frac{\widetilde{\varepsilon}^{2n}}{\left((\mathbf{r}-\mathbf{r}_0)^2 + |z-(2nt_s + z_0)|^2\right)^{\frac{1}{2}}} +$$
$$+ \frac{\widetilde{\varepsilon}^{2n}}{\left((\mathbf{r}-\mathbf{r}_0)^2 + |z-(z_0 - 2nt_s)|^2\right)^{\frac{1}{2}}} +$$
$$\left. \left. + \frac{\widetilde{\varepsilon}^{2n+1}}{\left((\mathbf{r}-\mathbf{r}_0)^2 + (z+z_0+2nt_s)^2\right)^{\frac{1}{2}}} \right) \right\}, \qquad (19)$$

where $\widetilde{\varepsilon} = (\varepsilon_{Si} - \varepsilon_{ox})/(\varepsilon_{Si} + \varepsilon_{ox})$, which can be illustrated by the series of induced image charges shown in Fig. 8.

As can be seen, one could expect the scattering image potential to be higher for the case of a SOI device than for a conventional MOSFET. The situation becomes however more complex if the device is a truly ultrathin DG SOI device, i.e. if the oxide layers are of ultrathin range. Then oxide layers with the thickness comparable to that of the semiconductor layer, or even thinner, must be taken into account, as well as the gate material influence. We utilize the following solution for the image potential in the Metal-SiO_2-Si system (Fig. 9) [18]:

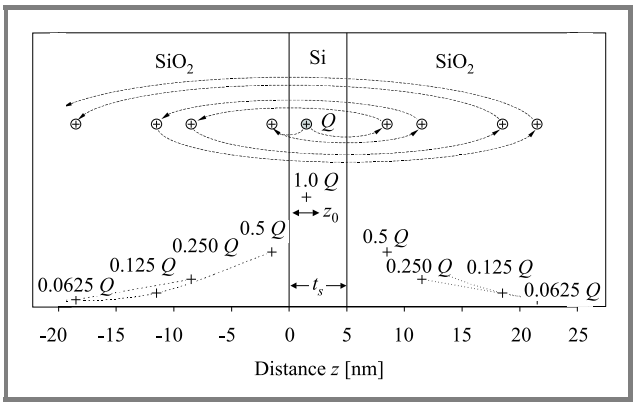

Fig. 8. Image charges seen in SOI device with $t_{ox} = \infty$.

$$\phi(\mathbf{r}, z) = \frac{Q}{4\pi\varepsilon_{Si}} \sum_{n=0} \left(\frac{\widetilde{\varepsilon}^{n+1}}{\left((\mathbf{r}-\mathbf{r}_0)^2 + (z+2nt_{ox}+z_0)^2\right)^{\frac{1}{2}}} + \right.$$
$$\left. - \frac{\widetilde{\varepsilon}^{n}}{\left((\mathbf{r}-\mathbf{r}_0)^2 + (z+2(n+1)t_{ox}+z_0)^2\right)^{\frac{1}{2}}} \right). \qquad (20)$$

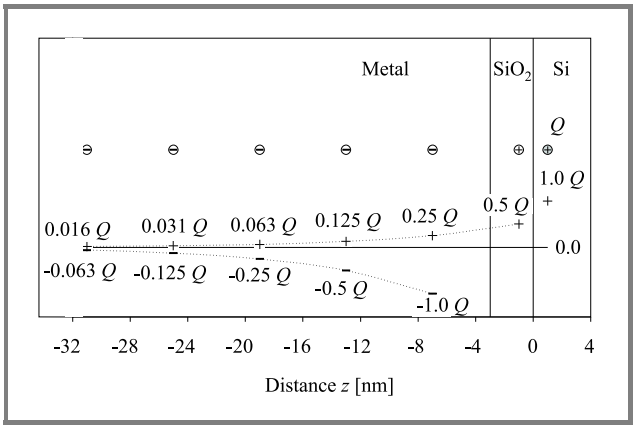

Fig. 9. Image charge affecting the potential felt in Si (Me-SiO_2-Si system).

Then we perform the superposition of the solutions (19) and (20) in order to obtain the image-charge distribution in the Me-SiO_2-Si-SiO_2-Me system, as shown in Fig. 10. Now, both metallic gates affect the resultant image potential, inducing image charge of opposite sign, and thus reducing the total scattering potential.

Next, we derive Coulomb scattering rates and the electron mobility limited by impurity ions (of assumed concentration of $N_A = 10^{17}$ cm^{-3}) located in the channel area, employing the model [4] and including the screening effect, which is also affected by the modified image-charge

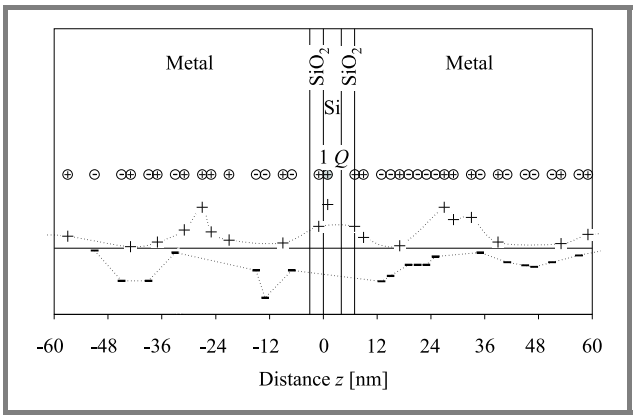

Fig. 10. Image charge affecting the potential felt in Si (Me-SiO_2-Si-SiO_2-Me system).

distribution. The calculated mobilities are plotted versus effective transverse electric field for DG SOI with various values of semiconductor thickness (from 15 nm to 2 nm) and for NMOSFET (Fig. 11), as well as for various gate oxides (Fig. 12). As can easily be seen, the obtained mobilities are much higher for ultrathin DG SOI devices than for the NMOSFET. As already mentioned, this is the consequence of energy level configuration in DG SOI, which favors electron occupation of the non-primed E_0 subband when thinning the semiconductor layer and/or decreasing the gate bias. Moreover, **the surface density of impurity ions is reduced in thinner semiconductor layers**. However, no interface states have been included here, which may change the overall picture due to doubled interface influence.

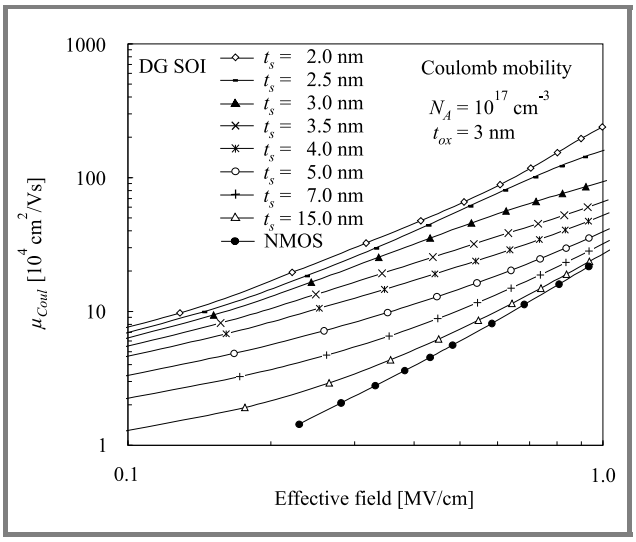

Fig. 11. Coulomb electron mobility for the DG SOI and NMOSFET transistors.

Figure 12 shows the mobility with the gate oxide as a parameter and it presents a comparison of different image charge models in the case of a NMOS transistor and a DG SOI transistor with the silicon layer thickness equal to 2 nm. The "conv." points (black dots) correspond to the conventional model of "one real – one image" charge, typically employed in MOSFETs, while the curve "∞" (for DG SOI only) corresponds to the infinite thickness of both oxide layers, as shown in Fig. 8. The curves for different oxide layers were obtained including the influence of a metallic gate on the image potential. The image

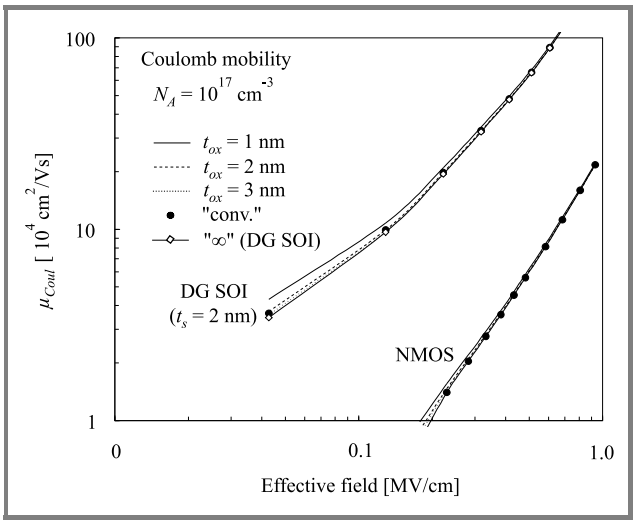

Fig. 12. Coulomb electron mobility for different t_{ox}.

charge reduces the scattering potential introduced by an impurity ion, but it also affects the inversion charge, and thus reduces the screening effect controlled by the inversion charge. Considering the screening, the image charge induced in the gate material replaces the inversion charge. Therefore, only a slight increase of the Coulomb mobility relative to the conventional model is noticeable for oxides below about 3 nm and mainly in the range of lower fields, since for higher fields the inversion charge of high concentration dominates as a screening factor. Here the model taking into account the specificity of the DG SOI structure gives results similar to those obtained with the conventional MOSFET-dedicated model.

6. Interface roughness scattering

Since carrier transport in MOS/SOI devices takes place in the near-surface layer of the semiconductor at the border with the dielectric layer, surely all irregularities of this interface, called surface roughness, must contribute to scattering, thus limiting the effective carrier mobility. This scattering mechanism is believed to dominate in the range of higher fields, where the electrons are forced towards the surface.

Statistical parameters of the Si-SiO_2 interface, which determine its scattering properties, are typically described by the autocovariance function $C(\mathbf{r}) = \langle \Delta(\mathbf{r}')\Delta(\mathbf{r}'-\mathbf{r})\rangle$ and the corresponding spectrum $S(\mathbf{q}_{||}) = |\Delta(\mathbf{q}_{||})|^2$ of the function $\Delta(x,y)$ (usually unknown) of local deviations from the ideally smooth interface. The form of the auto-covariance function is still a matter of investigation, and usually

Gaussian or exponential forms are employed with some modifications [19, 20]. Here we assume the exponential one:

$$C(\mathbf{r}) = \Delta^2 \exp\left(-\frac{\sqrt{2}r}{\lambda}\right), \tag{21}$$

$$S(\mathbf{q}_{||}) = \pi\Delta^2\lambda^2\left(1+\frac{q_{||}^2\lambda^2}{2}\right)^{-3/2}. \tag{22}$$

In each case the key parameters are Δ – the rms value of the deviations and λ – the correlation length.
The spatial deviations of the interface result in deviations of the potential experienced by electrons in the channel. The corresponding spatial shift of the potential energy:

$$\Delta V(z) = V'(z) - V(z) \tag{23}$$

(see Fig. 13) is treated as the perturbation and usually approximated by:

$$\Delta V(z) \approx \Delta(\mathbf{r})\frac{\partial V(z)}{\partial z}. \tag{24}$$

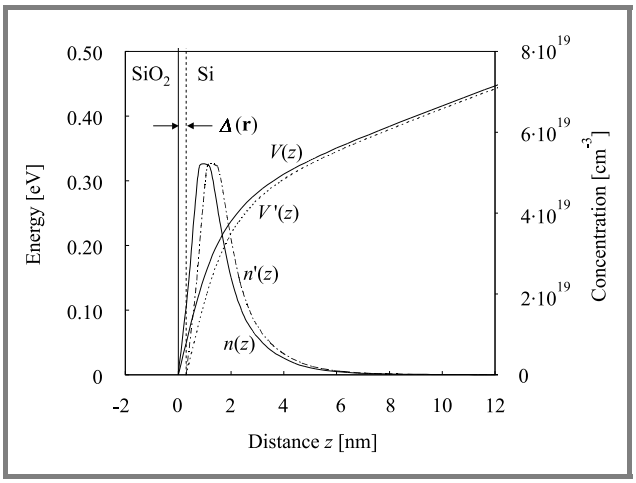

Fig. 13. Illustration of local deviation of the Si-SiO_2 interface from the ideal plane.

Therefore, taking into account this "geometrical" effect only, the matrix element is expressed in terms of the transverse electric field $E(z)$:

$$M_{ij} = e\int \xi_i(z)\Delta(\mathbf{r})E(z)\xi_j(z)dz. \tag{25}$$

Assuming that only the lowest subband is occupied (as in the low-temperature regime), one obtains a direct dependence of the matrix element on the effective field:

$$M_{00} = e\Delta(\mathbf{r})E_{eff} \tag{26}$$

which is a commonly employed approximation when modeling the surface roughness mobility.
It has been reported, however, that in the case of ultrathin SOI devices the approximation (24)-(25) cannot be further employed and the perturbation potential should be rather derived based on the definition (23) [21]. On the other hand, a still more complex description of surface roughness scattering includes additional effects due to electron distribution shift and extra electric field due to the deformed interface, as well as the image-charge modification [4]. This "full" matrix element is given by:

$$M_{ij}\left[q_{||}(\beta)\right] = \int_0^\infty dz\left(\xi_i(z)\frac{\partial V(z)}{\partial z}\xi_j(z)\right) + \\ + \frac{e^2}{\varepsilon_{\mathrm{Si}}}\frac{\varepsilon_{\mathrm{Si}}-\varepsilon_{ox}}{\varepsilon_{\mathrm{Si}}+\varepsilon_{ox}}\int_0^\infty dz\xi_i(z)\gamma(q_{||})\xi_j(z), \tag{27}$$

where:

$$\gamma(q_{||}) = \left(N_{inv}+N_{depl}\right)e^{-q_{||}z} + \\ + \frac{q_{||}^2}{16\pi}\left(\frac{K_1(q_{||}z)}{q_{||}z} - \frac{(\varepsilon_{\mathrm{Si}}-\varepsilon_{ox})}{2(\varepsilon_{\mathrm{Si}}+\varepsilon_{ox})}K_0(q_{||}z)\right) \tag{28}$$

and K_1, K_0 are the modified Bessel functions.
The surface roughness scattering rate is given by:

$$\frac{1}{\tau_{ij}\left(E(k)\right)} = \frac{2\pi}{\hbar}\frac{1}{2\pi\hbar^2}\theta\left(E(k)-E_j\right)\times \\ \times\int_0^{2\pi}\frac{d\beta}{2\pi}\, m_d\; S\left[q_{||}(\beta)\right]\left|M_{ij}\right|^2\left(1-\cos\beta\right). \tag{29}$$

In this work we compare the three models mentioned above employing them in the case of an ultrathin DG SOI transistor. We denote them as: Model 1, corresponding to the simplified form (25) of the matrix element, Model 2, corresponding to the matrix element derived using definition (23), and Model 3, which not only employs the matrix element according to Model 2 but also includes additional

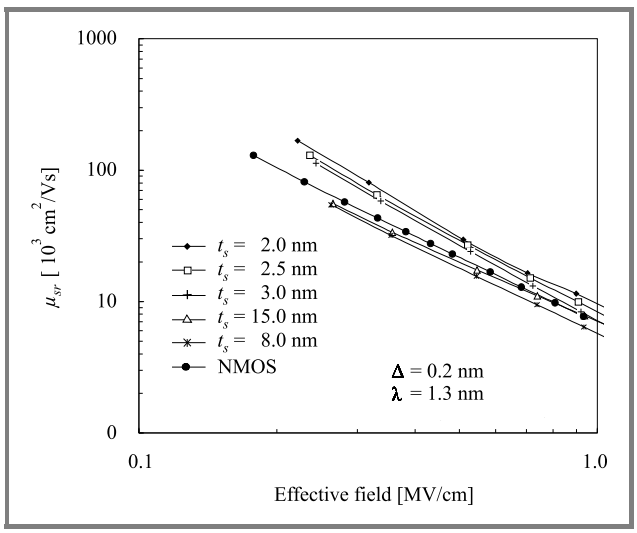

Fig. 14. Surface roughness mobility – Model 1.

effects (expressions (27)-(28)). In all these cases screening by inversion electrons is included. The interface parameters employed are $\Delta = 0.2$ nm and $\lambda = 1.3$ nm. The results

are shown as surface roughness mobility plotted vs. effective field for various semiconductor thicknesses of DG SOI. The results corresponding to a NMOS transistor serve as a reference. Figure 14 shows the mobility obtained using Model 1. As can be seen, the calculated dependencies for the DG SOI transistor follow approximately the $(E_{eff})^{-2}$ slope, as is typically recognized for MOSFETs. However, when analyzing these results in terms of the active semiconductor layer thickness, the observed tendency is somewhat surprising and doubtful. Here, the mobilities increase with the thinning of the semiconductor layer in DG SOI.

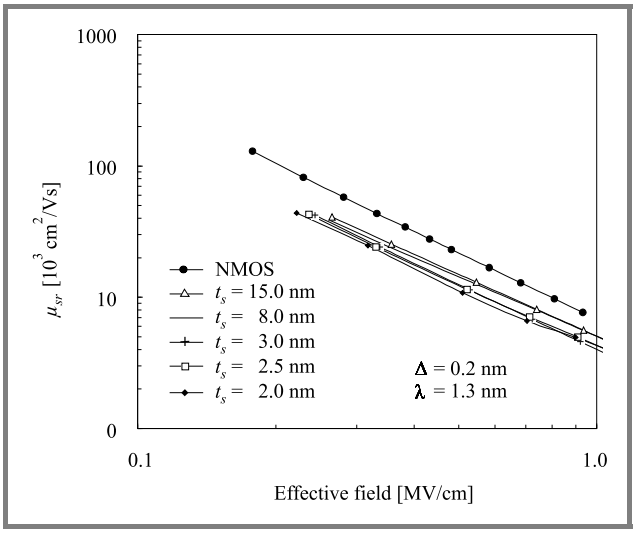

Fig. 15. Surface roughness mobility – Model 2.

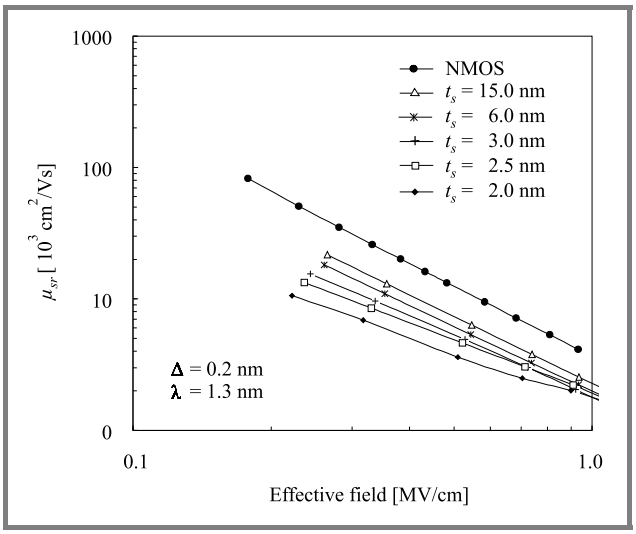

Fig. 16. Surface roughness mobility – Model 3.

Moreover, they exceed the mobility of the NMOS, even in the range of the thinnest layers (2–3 nm). One may intuitionally expect the SOI devices to exhibit a quite opposite trend, since the second SiO_2-Si interface is also rough and surely contributes to the scattering. Additionally, a given roughness height Δ becomes of higher importance when decreasing the semiconductor thickness, particularly in the ultrathin range. Better results, in this regard, are obtained with a more precise Model 2 (Fig. 15), since all the DG SOI points lie below the NMOS curve. However, still no unequivocal and strong enough trend is observed in terms of the semiconductor thickness. Model 3, being of the highest complexity, "improves" the picture accordingly to our expectations – the calculated surface roughness mobility strongly decreases with the semiconductor layer thickness decrease (Fig. 16).

7. Conclusions

Having derived the mobility components, we compose, according to (13), the effective electron mobility for the symmetrical DG SOI and NMOS transistors and plot it vs. the effective field (Fig. 17) and as a function of the semiconductor thickness (Fig. 18).

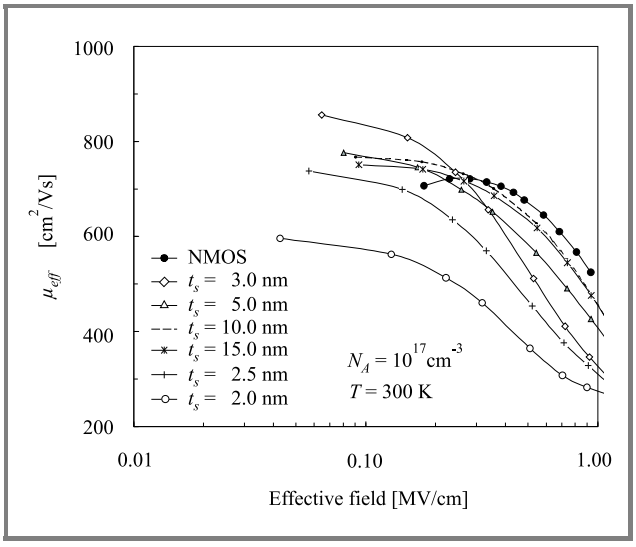

Fig. 17. Effective electron mobility versus transverse effective field.

The effective mobility is mainly determined by the phonon scattering at room temperatures, and it is additionally suppressed by the Coulomb scattering in the range of lower fields and by the interface roughness scattering in the range of higher transverse fields.

The phonon scattering is generally more intense in ultrathin DG SOI structures than in the conventional bulk MOS transistor and its impact increases with the thinning of the active semiconductor layer due to stronger spatial confinement of electrons in narrowed potential bounds.

However, another effect affecting transport properties of electrons may be observed in ultrathin symmetrical DG SOI devices oriented in the (100) plane. The energy separation between the primed and nonprimed eigenstates series increases when the semiconductor layer becomes thinner and/or the gate bias is relaxed, thus favoring the occupation of the lower nonprimed series (the lowest energy level E_0 subband, to be precise) of lower electron mass

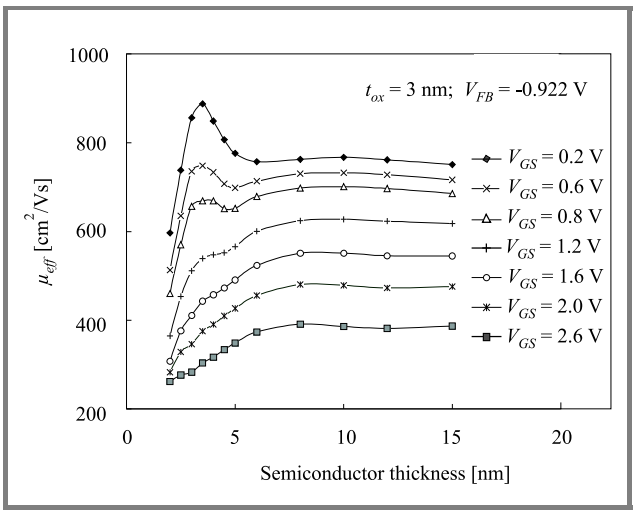

Fig. 18. Effective electron mobility in DG SOI transistor versus semiconductor layer thickness.

in the transport direction. This is illustrated in Fig. 19, where it can be seen that in the ultrathin range of the semiconductor thickness the combined population of the subbands E_0 and E_1 relative to the total inversion charge, reaches nearly 100%. Because of the two counteracting effects mentioned above, a certain increase of the phonon mobility may be expected to occur in the ultrathin range (here, according to our calculations, for the semiconductor thickness of about 3 nm), which has also been reported by other researchers [6, 8].

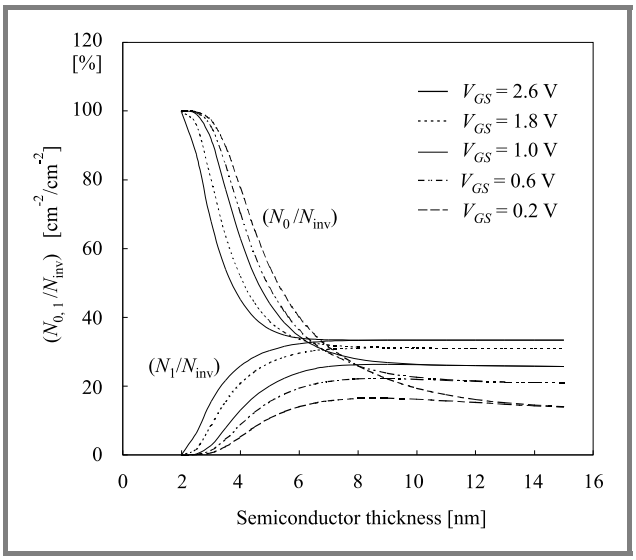

Fig. 19. Relative fraction of electrons in subbands E_0, E_1 (the nonprimed series) in the total inversion charge for DG SOI versus semiconductor thickness ($t_{ox} = 3$ nm).

The discussed "transport-facilitating" effect of the subband configuration plays an important role also in the case of Coulomb scattering, which suppresses the mobility more strongly in the conventional bulk MOSFET than in the DG SOI transistor, as analyzed here for the impurity-ion scattering. On the other hand, ultrathin DG SOI devices suffer much more from the interface roughness scattering than bulk MOSFETs due to the presence of another interface. This effect increases strongly when the semiconductor thickness is scaled down.

In this work we obtained results suggesting a possible increase of electron mobility in the symmetrical DG SOI transistor for the range of semiconductor layer thickness of about 3 nm. This effect is justified by theoretical postulates.

Furthermore, we have shown that conventional MOSFET dedicated models, particularly simplified ones, need to be reconsidered when applied to ultrathin SOI devices, although the modeling results may not be very sensitive to the model employed (as here in the case of image charge models), or, on the contrary, very sensitive (as for the interface roughness modeling).

Therefore, due to structural specificity, which allows for the semiconductor layer thickness variation and the corresponding change of the quantum structure across the channel area, ultrathin SOI and in particular DG SOI devices may be very efficient tools enabling verification of the carrier scattering theory.

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