Paper

Synthesis method for distributed amplifiers

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Abstract — New design method is presented for distributed amplifiers (DA). It is shown that by proper design of the applied transmission lines (TL) between the active devices the image impedance and the cut-off frequency (*COF*) of the input or output line of the DA can be independently tuned. As a consequence, the phase mismatch between the lines of the DA can be adjusted independently from the termination conditions and from the capacitances of the applied transistor and thus flat gain characteristic can be achieved. The method is well applicable for nearly unilateral devices like HBTs [1] and yields the highest gain-bandwidth product.

Keywords — distributed amplifier, gain-bandwidth products, phase synchronization, optical receivers.

1. Introduction

Distributed amplifiers have the widest bandwidth among the known gaining circuits. They are usually designed by computer optimization. However, in the presence of parasitics the error function has many local minima and thus it is difficult to find a global minimum. A better approach if the optimization is started from a simplified but almost perfect structure, which was generated by a systematic design procedure. However, huge amount of publications in the field [2] describes only analyses methods and just a very few gives direct synthesis methods.

An effective one was published by Beyer [3] for monolithic DAs comprised unilateral transistors. The method is valid if phase synchronization exists between the DA lines and if the applied TLs are short enough to be approximated by simple lumped Π network. Beside that, it manipulates the transistor losses to compensate the effect of the pole at the *COF*. However, as the input capacitance of the active device is usually much higher than the output one the phase synchronization can be difficult to achieve in a lumped element DA that works between fixed termination impedances. Other problem is that due to the required loss values, the other properties of the transistors (noise etc.) may be not optimal.

The method proposed by this paper tunes only the TLs between the active devices, thus the transistor's performance can be optimal. The design method is based on some important theoretical results, which were published in [4, 5]. They will be summarized as follows.

Considering the DA structure in Fig. 1 the closed formulas for the power-gain of a DA comprised TLs and unilateral active devices were derived. It was shown that the gain-bandwidth product (*GBP*) of the DA is proportional to the impedance-bandwidth product (*IBP*) of its input and output line. The *IBP* of a DA line is determined by the DA line impedance and by the *COF*.

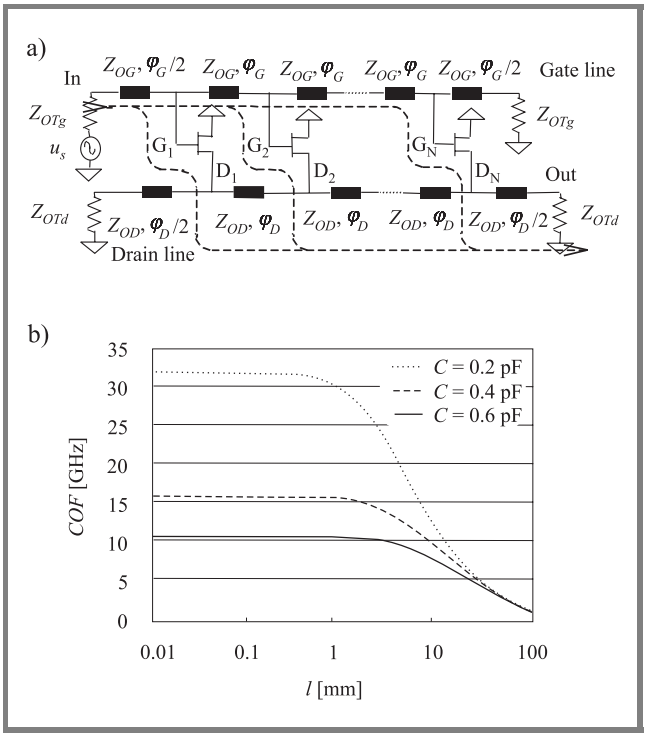

Fig. 1. (a) Model of an *N*-stage distributed element DA; (b) *COF* vs. TL's physical length *l* at different *C* values ($k = 50\ \Omega$, $v = c$).

In the case of a transistor which comprises only the input and output capacitances (C) and the transconductance the Z_{0T} and $Z_{0\Pi}$ image impedances of a line of the DA can be written as follows ($Y = j\omega C$):

$$Z_{0T} = Z_0\sqrt{\frac{2j\sin\varphi + Z_0 Y(\cos\varphi - 1)}{2j\sin\varphi + Z_0 Y(\cos\varphi + 1)}}, \quad Z_{0\Pi} = \frac{2Z_{0T}}{2 + jYZ_0\tan\frac{\varphi}{2}}. \tag{1}$$

The *COF* can be determined from the propagation factor per section, which is takes the form:

$$\theta = \operatorname{arcosh}\left(\cos\varphi + j\frac{YZ_0}{2}\sin\varphi\right); \quad \varphi = \omega\frac{l}{v}. \tag{2}$$

In the passband θ must be pure imaginary, i.e. the magnitude of the argument of the arcosh must be less than one. The *COF* can be calculated from this condition. However, it results a transcendental equation, which cannot be solved

in closed form, thus only approximate value for the *COF* (due to the TL, infinite number of upper passbands exists, but in this paper only the first one is applied) can be calculated. Conclusions are as follows:

- The *IBP* decreases as the capacitance increases.
- At a given capacitance and given TL characteristic impedance (Z_0) value, the image impedances are decreasing and the *COF* is increasing as the TL physical lengths (l) became shorter.

To maintain the image impedances on a k constant level the proper increase of the Z_0 value is necessary during the shortening of the TL lengths. The necessary Z_0 value can be computed from the DC limit of the image impedances:

$$Z_0(k, l, C) = \frac{1}{2l}\left(k^2 Cv + \sqrt{k^4 C^2 v^2 + 4l^2 k^2}\right). \qquad (3)$$

Substituting Eq. (3) into Eq. (2) and applying the condition mentioned there the *COF* can be calculated in the case of constant (k) low frequency image impedance (*LFI*) value at different TL lengths. The approximated *COF* are plotted in Fig. 1b as a function of the TL's physical length at different capacitance values. It can be seen, that the *COF* monotonically increases as the physical length of the TLs tends to zero. Because the image impedances are not changing we can conclude that the *IBP* is maximum at zero TL length. Simultaneously the characteristic impedance of the TLs must tend to infinity to satisfy Eq. (3). According to this it can be concluded that a DA line with lumped inductances has the highest *IBP*, i.e. a lumped element DA has the highest *GBP* with a given transistor and termination conditions.

The same behaviour was achieved in the presence of the series parasitic connection inductances (denoted by L_B) of the active device. It was also found that these inductances cause significant bandwidth degradation. In this case the formulas of image impedances and propagation factor remain valid if Y is replaced by Y^B ($Y^B = j\omega C/(1-\omega^2 C L_B)$). The required Z_0 value to get a constant line impedance can also be computed by Eq. (3). For this case the *COF* of a DA line vs. TL's physical length is plotted in Fig. 2a at different L_B values ($C = 0.4$ pF).

A third type of transistor connection is also proposed: the so-called V-shape connection which yields higher *COF* than the normal connection. The structure can be observed on the input line of he DA presented in Fig. 4a. The image impedances can be found in [5]. The propagation factor is given by Eq. (4). The necessary Z_0 value to maintain a constant (k) LFI can be computed by Eq. (5). The *COF* of a V-shape DA line vs. l is plotted in Fig. 2b ($L_B = 0.3$ nH).

An important conclusion of the above results is that in a DA applying TLs the *COF* as well as the θ of the DA lines can be varied independently from the line impedance value (usually it must be matched to the termination). Due to the variability of the phase mismatch between the gate and drain lines, this property gives an additional degree

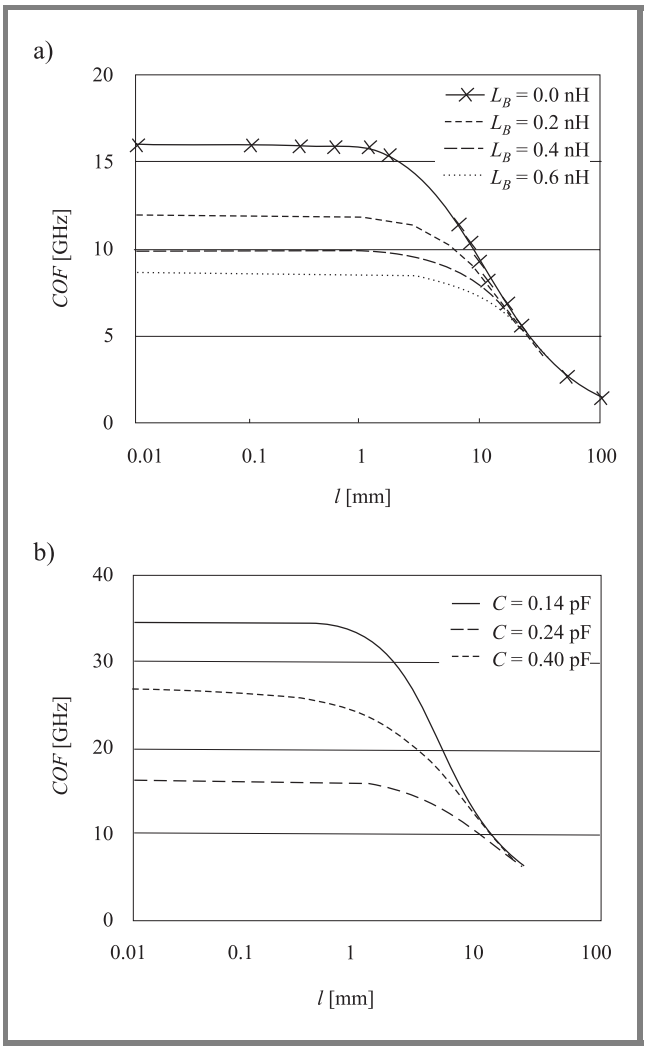

Fig. 2. (a) *COF* vs. l at different L_B values ($k = 50\ \Omega$, $v = c$); (b) *COF* vs. l at different C values ($k = 50\ \Omega$, $v = c$).

of freedom in the design. In contradiction, in a lumped element DA the θ yields from the capacitance and the image impedance value, hence cannot be varied [2]. In this paper the necessary phase mismatch between the DA lines are calculated to achieve a desired gain flatness. Next, a new hybrid structure is introduced for DAs using typical transistors. Finally, the design process is demonstrated on a design example, which gives the highest *GBP* with flat gain

$$\theta = \operatorname{arcosh}\left(\cos\theta(1 + YZ_B) + \right.$$
$$\left. + j\sin\theta\left(\left(2Z_B + Y\left(Z_0^2 + Z_B^2\right)\right)/2Z_0\right)\right); \qquad (4)$$
$$Z_B = j\omega L_B; \quad Y = j\omega C$$

$$Z_0(k, l, C, L_B) = \tfrac{1}{2l}\left(k^2 Cv - 2L_B v + \right.$$
$$\left. + \sqrt{k^4 C^2 v^2 + 4l^2 k^2 + 4L_B^2 v^2 - 4L_B v^2 k^2 C}\right). \qquad (5)$$

2. Effect of phase mismatch

The *GBP* is the highest if the physical lengths are minimal. Hence, during the design the TLs must keep as short as possible. Due to this reason, the effect of phase mismatch is analyzed only for lumped element DA. The phase mismatch can be described by the ratio of the drain and gate cut-off frequencies: $q = \omega_{CD}/\omega_{CG}$. The relative deviation of the power gain from its DC value as a function of the frequency is given by Eq. (6) for a DA comprised simplified transistors (only C_{GS}, C_{DS} and gm presents) the following equation:

$$\Delta P(\omega_{rel}) = \frac{1}{N^2} \frac{1}{\left(\sqrt{1-\omega_{rel}^2 \frac{1}{q^2}}\right)^* \sqrt{1-\omega_{rel}^2}} \left| \frac{\sin\left(\frac{N}{2}\Delta\theta\right)}{\sin\left(\frac{\Delta\theta}{2}\right)} \right|^2 . \tag{6}$$

In a real transistor the C_{GS} is bigger than C_{DS}, thus in Eq. (6) the frequency is related to the gate cut-off frequency, i.e. $\omega_{rel} = \omega/\omega_{CG}$.
As one can observe, at a given relative frequency the deviation depends on N (stage number) and q. By expanding the sin in Taylor series and neglecting the higher order parts an approximate analytical equation can be derived both of them. The N is given by Eq. (7) where ($\Delta\theta = \theta_D - \theta_G$)

$$N(\omega_{rel}, q, \Delta P) = \sqrt{\frac{40 - \sqrt{-320 + \left(1920 - 80\Delta\theta^2 + \Delta\theta^4\right)\left(1-\omega_{rel}^2\right)^{\frac{1}{4}}\left(1-\frac{\omega_{rel}^2}{q^2}\right)^{\frac{1}{4}}\sqrt{\Delta P}}}{\Delta\theta^2}} . \tag{7}$$

Similar equation can be derived for the presence of connection inductances:

$$N(\omega_{rel}, q, \Delta P) = \sqrt{\frac{40 - \sqrt{-320 + \left(1920 - 80\Delta\theta^2 + \Delta\theta^4\right)\left(1-\omega_{rel}^2\right)^{\frac{3}{4}}\left(1-\frac{\omega_{rel}^2}{q^2}\right)^{\frac{3}{4}}\frac{\sqrt{\Delta P}}{q}}}{\Delta\theta^2}} . \tag{8}$$

Due to the bigger gate capacitance, in real amplifiers the bandwidth of the drain line needs a significant reduction. According to this a DA with normal connection at the drain and V-shape connection at the gate may have practical importance. For this hybrid structure the N is described as follows

$$N(\omega_{rel}, q, \Delta P) = \sqrt{\frac{40 - \sqrt{-320 + \left(1920 - 80\Delta\theta^2 + \Delta\theta^4\right)\left(1-\omega_{rel}^2\right)^{\frac{1}{4}}\left(1-\frac{\omega_{rel}^2}{q^2}\right)^{\frac{3}{4}}\frac{\sqrt{\Delta P}}{q}}}{\Delta\theta^2}} \tag{9}$$

and is shown in Fig. 3a for $q = 1.55$. In the figure one can observe that at this q value a four stage DA has a flat gain response. If higher stage number is required, the value of the q should decrease. For lower stage numbers q must be increased.
If the flat response is required only up to 0.57 ω_{rel}, a six stage DA can produce a gain variation of less than 1 dB in the passband. It can be shown that up to 0.57 ω_{rel} the input and output matching of a DA is better than -20 dB,

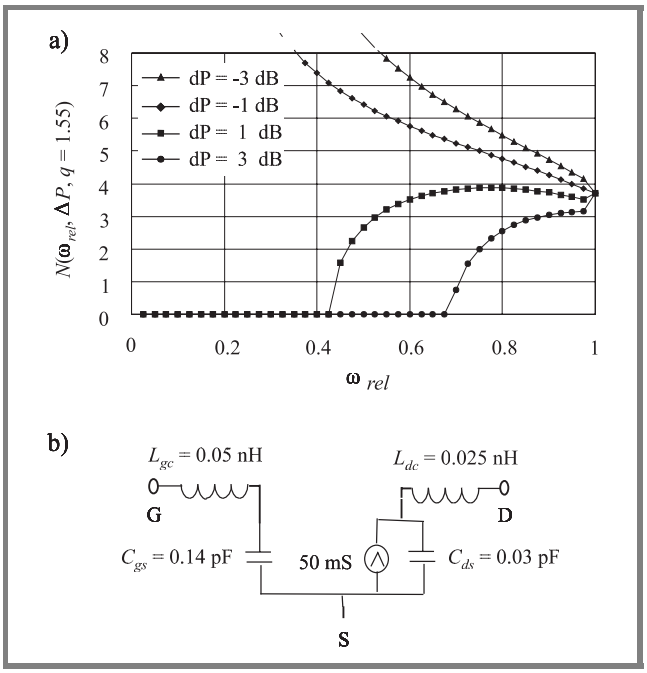

Fig. 3. (a) Number of stages to achieve a given gain deviation vs. relative frequency; (b) transistor model.

if the lines of the DA are ideal artificial transmission lines with *LFI* equal to the termination.

3. Design example

The method is demonstrated on a design example. The applied unilateral transistor model is shown in Fig. 3b. The inductances are the on-chip inductances. We assume that due to technological reasons the lowest value of the connection inductances (f.e. bonding inductance) is $L_B = 0.3$ nH. Due to the big difference between the transistor capacitances the application of the hybrid structure is practical. The gate is V-shape connected. If the only elements between the transistors are the two connection inductance ($2L_B$), the low frequency impedance (*LFI*) of the resulting gate artificial line is $LFI_G = (2L_B/C)^{0.5} = 65\ \Omega$ [4]. The cut-off frequency can be calculated by Eq. (10), due to the significant effect of the on-chip inductance on the bandwidth [4]

$$f_{cG} = \frac{1}{2\pi\sqrt{C_{gs}(L_{gc} + 2L_B/4)}} = 30.08\ \text{GHz}. \tag{10}$$

To achieve a matching better than -20 dB to 50 Ω, a *LFI* lower than 60 Ω is required. The gate line ends in a T-section, thus its characteristic impedance is monotonically decreased with frequency. Due to this property, a *LFI* level higher than the termination impedance results good matching in wider band. With 60 Ω *LFI* the matching is better than -20 dB up to 0.74 ω_{rel}. But to achieve 60 Ω *LFI* value, inserting of TLs is necessary. If we assume again that due to technological reasons at least $l = 0.5$ mm is needed, the resulting Z_0 is 38 Ω (from Eq. (5)). The degra-

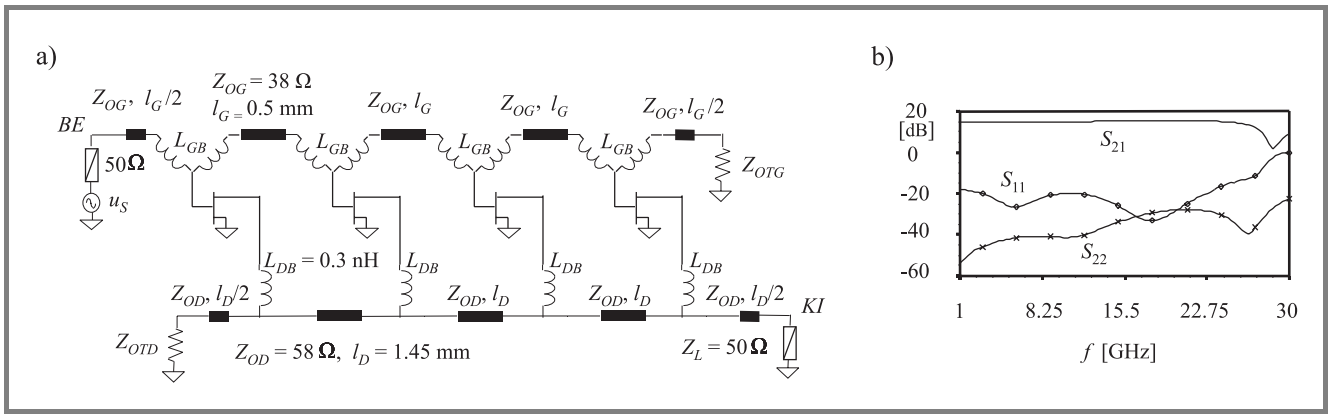

Fig. 4. (a) Hybrid DA structure with element values; (b) simulated results before optimization.

dation of the cut-off frequency is approx. 0.708 GHz (see Fig. 2b). Thus, up to $(30.08-0.708)*0.74=21.7$ GHz the matching of the gate line will be better than -20 dB.

In the drain line the transistors are connected by normal way, i.e the connection inductances are in series. If the line is designed for 50 Ω *LFI* the resulting interstage inductance value is $L_D = 0.075$ nH and the lumped element cut-off frequency is described as:

$$f_{cD} = \frac{1}{\pi\sqrt{C_{ds}\left(4(L_B+L_{dc})+L_D\right)}} = 49.56 \text{ GHz}. \quad (11)$$

However, in this case the q is 1.691, which is to big for a four stage amplifier. As it is shown in Fig. 3a the desired q value is 1.55, which corresponds to a drain cut-off frequency of 45.4 GHz. To achieve this, a proper TL must replace the L_D inductance. The necessary length can be read out from a figure similar to Fig. 2a, if a curve belong to $C = 0.03$ pF and $L_B = 0.3$ nH is drawn. The resulting l is 1.45 mm (in the case of $v = c$). The required drain TL Z_0 value to maintain a drain line *LFI* of 50 Ω is $Z_{0D} = 58$ Ω, which can be calculated from Eq. (3).

The final four stage amplifier structure is shown in Fig. 4a. The simulated results without optimization are shown in Fig. 4b (Aplac 7.5). They exactly follow the predicted properties. To a certain extent the effect of the losses and the source inductance can also be compensated by the decrease of q.

If the transistor is bilateral the value of the feedback capacitor (C_{GD}) is critical. If it is less than about 40% of C_{DS} its effect can be compensated by computer optimization applying the result of this method as a starting point.

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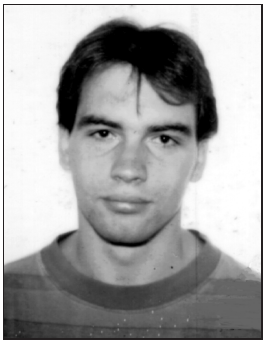

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