Regular paper

Efficient procedure for capacitance matrix calculation of multilayer VLSI interconnects using quasi-static analysis and Fourier series approach

Hasan Ymeri, Bart Nauwelaers, and Karen Maex

Abstract — In this paper, we present a new approach for capacitance matrix calculation of lossy multilayer VLSI interconnects based on quasi-static analysis and Fourier projection technique. The formulation is independent from the position of the interconnect conductors and number of layers in the structure, and is especially adequate to model 2D and 3D layered structures with planar boundaries. Thanks to the quasi-static algorithms considered for the capacitance analysis and the expansions in terms of convergent Fourier series the tool is reliable and very efficient; results can be obtained with relatively little programming effort. The validity of the technique is verified by comparing its results with on-surface MEI method, moment method for total charges in the structure, and CAD-oriented equivalent-circuit methodology, respectively.

Keywords* — *lossy IC interconnect, Fourier projection method, line capacitance.

1. Introduction

Calculation of the capacitance matrix in multilayer IC interconnects is a well-known problem that can be solved by many analytical and numerical techniques [1–9]. Often these procedures were based on the integral equation formulation, differential equation formulation, or have been the results of extensive numerical simulations using adequate empirical corrections.

This letter proposes a new and more general formulation for computation of capacitance matrix of the most common 2D interconnect structures using quasi-static analysis and Fourier projection approach.

2. Background of the method

In the formulation, 2D L-layered interconnect structures with planar boundaries are considered. Each layer is linear, homogeneous, and isotropic, and has permittivity $\varepsilon^{(l)}$ and conductivity $\sigma^{(l)}$, where $l = 1, \ldots, L$. For lossy medium the complex permittivity is $\underline{\varepsilon}^{(l)} = \varepsilon^{(l)} - j\sigma/\omega$. The point charge source is located along $y = 0$, $x = x_s$ and $z = z_s$, respectively (see Fig. 1).

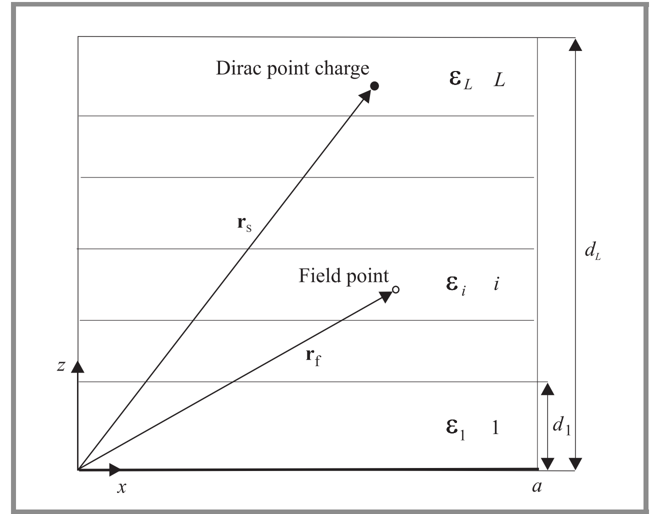


Fig. 1. Geometry of a layered structure for multilayer Green's function determination.

Inside each layer l and excluding the source point layer, the potential function $\varphi^{(l)}$ satisfies

$$\nabla^2 \varphi^{(l)} = 0 \tag{1}$$

and the induction vector $\mathbf{D}^{(l)}$ is obtained from

$$\mathbf{D}^{(l)} = -\underline{\varepsilon}^{(l)} \nabla \varphi^{(l)} . \tag{2}$$

Here, the problem is solved by developing each potential $\varphi^{(l)}$ as a Fourier series. In the source layer, the general solution to Eq. (1) can be written as

$$\varphi^{(s)}(x_f, y_f, z_f) = \varphi_P(x_f, y_f, z_f) + \varphi_H(x_f, y_f, z_f), \tag{3}$$

where φ_P is the source term given by

$$\varphi_P(x_f, y_f, z_f) = \frac{Q}{4\pi\underline{\varepsilon}^{(s)}} \left\{ \frac{1}{\left[(x_f - x_s)^2 + y_f^2 + (z_f - z_s)^2\right]^{\frac{1}{2}}} \right\} \tag{4}$$

and

$$\varphi_H(x_f,y_f,z_f)=\sum_{n,m\geq 0}\left[C_{nm}^{(s)}\exp(K_{nm}z_f)+\right.$$
$$\left.+D_{nm}^{(s)}\exp(-K_{nm}z_f)\right]\cos(k_nx_f)\cos(k_my_f)\,, \tag{5}$$

where $k_n=n\pi/a$, $k_m=m\pi/b$, $K_{nm}=(k_n^2+k_m^2)^{\frac{1}{2}}$, (x_f,y_f,z_f) are field point coordinates, and a and b are dimensions of the structures in x and y direction.
Considering Eq. (2), $\mathbf{D}^{(s)}$ is given by

$$\mathbf{D}^{(s)}(x_f,y_f,z_f)=\mathbf{D}_P(x_f,y_f,z_f)+\mathbf{D}_H(x_f,y_f,z_f) \tag{6}$$

with

$$\mathbf{D}_P(x_f,y_f,z_f)=\frac{Q}{4\pi}\left\{\frac{(x_f-x_s)\mathbf{1}_x+y_f\mathbf{1}_y+(z_f-z_s)\mathbf{1}_z}{\left[(x_f-x_s)^2+y_f^2+(z_f-z_s)^2\right]^{\frac{3}{2}}}\right\} \tag{7}$$

and

$$\mathbf{D}_H(x_f,y_f,z_f)=\underline{\varepsilon}^{(s)}\left\{\sum_{n,m\geq 0}k_n\left[C_{nm}^{(s)}\exp(K_{nm}z_f)+\right.\right.$$
$$\left.\left.+D_{nm}^{(s)}\exp(-K_{nm}z_f)\right]\sin(k_nx_f)\cos(k_my_f)\right\}\mathbf{1_x}+$$
$$+\underline{\varepsilon}^{(s)}\left\{\sum_{n,m\geq 0}k_m\left[C_{nm}^{(s)}\exp(K_{nm}z_f)+\right.\right.$$
$$\left.\left.+D_{nm}^{(s)}\exp(-K_{nm}z_f)\right]\cos(k_nx_f)\sin(k_my_f)\right\}\mathbf{1}_y+$$
$$-\underline{\varepsilon}^{(s)}\left\{\sum_{n,m\geq 0}K_{nm}\left[C_{nm}^{(s)}\exp(K_{nm}z_f)+\right.\right.$$
$$\left.\left.-D_{nm}^{(s)}\exp(-K_{nm}z_f)\right]\cos(k_nx_f)\cos(k_my_f)\right\}\mathbf{1}_z\,. \tag{8}$$

In the other layers, the solutions are

$$\varphi^{(l)}(x_f,y_f,z_f)=\sum_{n,m\geq 0}\left\lfloor C_{nm}^{(l)}\exp(K_{nm}z_f)+\right.$$
$$\left.+D_{nm}^{(l)}\exp(-K_{nm}z_f)\right\rfloor\cos(k_nx_f)\cos(k_my_f) \tag{9}$$

and

$$\mathbf{D}^{(l)}(x_f,y_f,z_f)=\underline{\varepsilon}^{(l)}\left\{\sum_{n,m\geq 0}k_n\left[C_{nm}^{(l)}\exp(K_{nm}z_f)+\right.\right.$$
$$\left.\left.+D_{nm}^{(l)}\exp(-K_{nm}z_f)\right]\sin(k_nx_f)\cos(k_my_f)\right\}\mathbf{1_x}+$$
$$+\underline{\varepsilon}^{(l)}\left\{\sum_{n,m\geq 0}k_m\left[C_{nm}^{(l)}\exp(K_{nm}z_f)+\right.\right.$$
$$\left.\left.+D_{nm}^{(l)}\exp(-K_{nm}z_f)\right]\cos(k_nx_f)\sin(k_my_f)\right\}\mathbf{1}_y+$$
$$-\underline{\varepsilon}^{(l)}\left\{\sum_{n,m\geq 0}K_{nm}\left[C_{nm}^{(l)}\exp(K_{nm}z_f)+\right.\right.$$
$$\left.\left.-D_{nm}^{(l)}\exp(-K_{nm}z_f)\right]\cos(k_nx_f)\cos(k_my_f)\right\}\mathbf{1}_z\,. \tag{10}$$

The potential function distribution $\varphi^{(l)}$ and the normal component of electric induction vector $\mathbf{D}^{(l)}$ are expressed by series expansions in terms of solutions of the Laplace Eq. (1). One such expansion is written down for each homogeneous region of the layered structure in Fig. 1. The expansion coefficients $C_{nm}^{(l)}$ and $D_{nm}^{(l)}$ of the different series are related to each other and to the charge density distribution on the interconnect conductors via boundary conditions. Then, coefficients $C_{nm}^{(l)}$ and $D_{nm}^{(l)}$ are determined recursively. In this way we have found the multilayer Green's function $G(\mathbf{r}_f;\,\mathbf{r}_s)$ of the problem. By deriving the Green's function over a multilayer dielectric region and allowing evaluation of potential distribution in any layer, we can place interconnect conductors anywhere in the multilayer structure, and therefore solve for the capacitance per unit length matrix for an arbitrary number of conductors.

3. Capacitance matrix calculation

In the following the complex capacitance calculation procedure will be treated in more detail. In an equivalent circuit, the value of a capacitance is the ratio of the free charge associated with a voltage difference between two interconnect conductors or between a interconnect conductor and the reference (e.g. the ground plane or the point at infinity), and that voltage difference. The values of these capacitances are known as network capacitances.
According to the equivalent source principle for the electromagnetic field, we can replace the rectangular conductor (c) (see Fig. 2a) with a piece of surface charge density distribution $\sigma_c(\mathbf{r}_s)$ around the surface S_c, as shown in Fig. 2b. Using a Green's function of the medium $G(\mathbf{r}_p;\,\mathbf{r}_s)$ that incorporates all boundary conditions in the structure in Fig. 2b (see Sec. 2), the voltage at any point $\mathbf{r}_p$ is generated by the charge density $\sigma_c(\mathbf{r}_s)$ on all conductors ($c=1,\ldots,N$)

$$V(\mathbf{r}_p)=\sum_{c=1}^{N}\oint_{(c)}\sigma_c(\mathbf{r}_s)G(\mathbf{r}_p;\,\mathbf{r}_s)dS_c\,. \tag{11}$$

Element C_{cj} of the capacitance matrix [C] may be calculated as the charge Q_c per unit length on conductor (c) when the voltage on conductor (j) is 1 and 0 V on all other conductors. The charge per unit length on conductor (c) is the integral of the surface charge density $\sigma_c(\mathbf{r}_s)$ over the circumference of conductor (c): $Q_c=\oint_{(c)}\sigma_c(\mathbf{r}_s)dS_c$. The charge distribution on every conductor (c) may be approximated by a number N_b of well-chosen basis functions $\sigma_{c,r=1,\ldots,N_b}(\mathbf{r}_s)$ along the contour of the conductor: $\sigma_c(\mathbf{r}_s=\sum_{r=1}^{N_b}W_{c,r}\sigma_{c,r}(\mathbf{r}_s)$. The problem has been reduced to the computation of the discrete charge constants $\{W_{c=1\ldots N,r=1\ldots N_b}\}$. As the result we obtain a series of simultaneous equations and represent them as follows:

$$\sum_{c=1}^{N}\sum_{r=1}^{N_b}W_{c,r}p_{j|c,r|t}=V_{j=1\ldots N}\,, \tag{12}$$

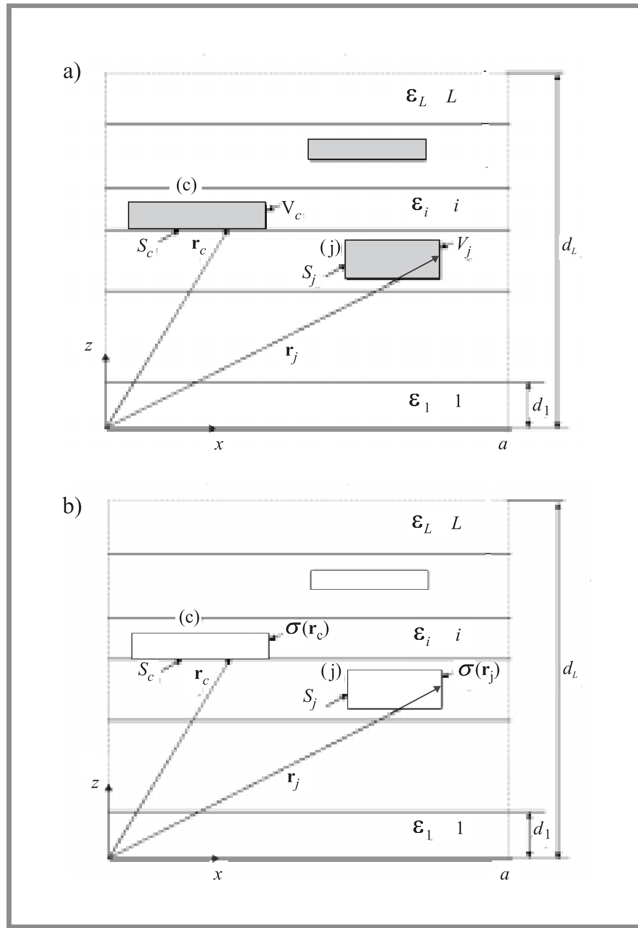


Fig. 2. Geometry of a layered structure with (a) embedded conductors, and (b) charge density distribution on the discretized surface of the conductors.

where $V_{j=1...N}$ is the voltage on any conductor (j), with

$$p_{j|c,r|t} = \frac{\oint_{(j)} \oint_{(c)} \sigma_{j,t}(\mathbf{r}_j) G(\mathbf{r}_j;\mathbf{r}_c) \sigma_{c,r}(\mathbf{r}_c) dS_c \, dS_j}{\oint_{(j)} \sigma_{j,t}(\mathbf{r}_j) dS_j} \tag{13}$$

as potential coefficients of the Galerkin matrix. Solving the matrix Eq. (12) on a computer, we can determine the constants $\{W_{c,r}\}$ and then the capacitance per unit length C_{cj} can be obtained in the form:

$$C_{cj} = Q_c(V_j = 1,\ V_{c \neq j} = 0) = \sum_{r=1}^{N_b} W_{c,r} \oint_{(c)} \sigma_{c,r}(\mathbf{r}_c) dS_c. \tag{14}$$

The lossy semiconducting substrate is taken into account by the complex permittivity

$$\varepsilon_{cs} = \varepsilon_s - j\frac{\sigma}{\omega}, \tag{15}$$

where ε_s is the permittivity and σ conductivity of the semiconducting substrate (silicon).

Due to the quasi-TEM character of the electromagnetic fields in the examined structure the frequency dependent distributed admittance per unit length Y can be calculated as

$$Y = G + j\omega C = j\omega \frac{Q}{\Delta V}, \tag{16}$$

where Q is the total charge per unit length, ΔV denote the voltage difference between the conductors, G is the conductance per unit length (losses) and C is the capacitance per unit length.

4. Discussion of the results

In this section we apply the new procedure to calculate some examples. In these examples we use multilayer IC interconnects whose strip conductors are infinitely thin (zero-thickness) or of rectangular cross-section and very thick (as usually in on-chip interconnets).

Example 1. Let us consider the system of four strip conductors embedded in a two-layered dielectric region with structure as shown in Fig. 3, where the conductors are numbered from left to right and upper to lower as 1, 2, 3 and 4, respectively. Numerical values for the ca-

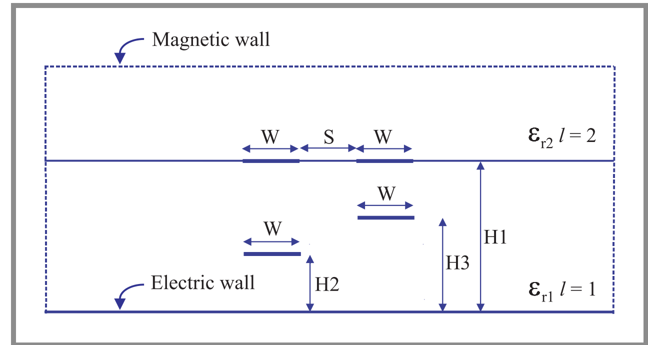


Fig. 3. Geometry of the structure from example with four strips (W/H1 = S/H1 = H2/H1 = 1/3, H3/H1 = 2/3, $\varepsilon_{r1} = 5$ and $\varepsilon_{r2} = 1$).

Table 1
Capacitance matrix of the structure of Fig. 3

Capacitance [pF/m]	MoM [5, 7]	MEI [1]	This letter
C_{11}	70.158	69.514	70.158
C_{12}	–12.842	–12.832	–12.839
C_{13}	–12.960	–13.110	–12.967
C_{14}	–22.240	–23.014	–22.230
C_{22}	87.327	87.028	87.227
C_{23}	–54.195	–55.462	–54.234
C_{24}	–4.052	–3.988	–4.049
C_{33}	133.935	128.86	128.50
C_{34}	–14.16	–14.93	–14.21
C_{44}	135.70	141.31	135.94

pacitance matrix elements, generated by the proposed approach (the moment method has been used) and by the on-surface MEI procedure [1] and the moment method with total charge in structure [5, 8], respectively, are given in Table 1. Note that the discrepancies between the values generated by our approach and one by [5, 8] are practically smaller than 0.2% over a wide range of physical dimensions and material parameters (all treated cases are not reported in this letter).

Example 2. In order to prove the validity of the given approach self and mutual shunt admittance per unit length (capacitance and conductance per unit length) calculated using our procedure are compared with the results of the full-wave analysis (spectral domain approach) in conjunction with equivalent circuit modeling technique [9]. In Fig. 4, an asymmetric coupled interconnect structure is depicted with the following electrical and geometrical parameters:

$$t_{Si} = 500\ \mu\text{m},\ t_{ox} = 2\ \mu\text{m},\ w_1 = 4\ \mu\text{m},\ w_2 = 1\ \mu\text{m},$$
$$T_1 = T_2 = 1\ \mu\text{m},\ \varepsilon_{si} = 11.8,$$
$$\rho_{Si} = 0.01\ \Omega\text{cm},\ \varepsilon_{ox} = 3.9\ \text{ and }\ \text{s} = 4\ \mu\text{m}.$$

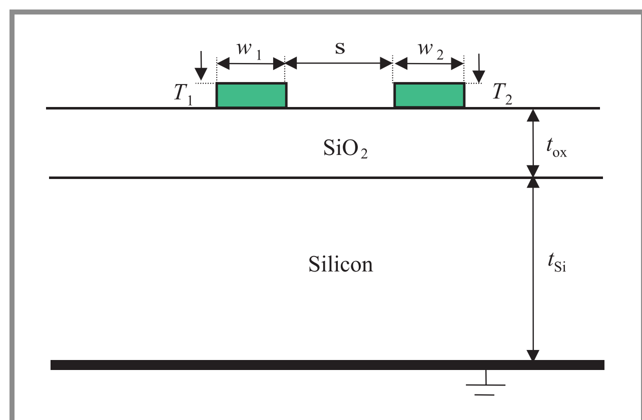


Fig. 4. Asymmetric coupled interconnects on lossy silicon substrate.

Figure 5a shows the variation in the distributed self and mutual capacitance per unit length $C_{11}(\omega)$, $C_{22}(\omega)$, and $C_{12}(\omega)$, as a function of frequency. Similarly, Fig. 5b shows the variation of the distributed self and mutual conductance per unit length $G_{11}(\omega)$, $G_{12}(\omega)$, and $G_{22}(\omega)$ as a function of frequency. The solid lines are computed using the new multilayer Green's function procedure and the dashed lines are the results from the equivalent-circuit model approach [9]. It is observed that the values of the self and mutual capacitance and conductance per unit length, respectively, are in good agreement with those of [9]. As expected, the lossy silicon semiconducting substrate has significant impact on the frequency-dependence of the capacitance and conductance per unit length as compared to the lossless or low loss dielectric substrate.

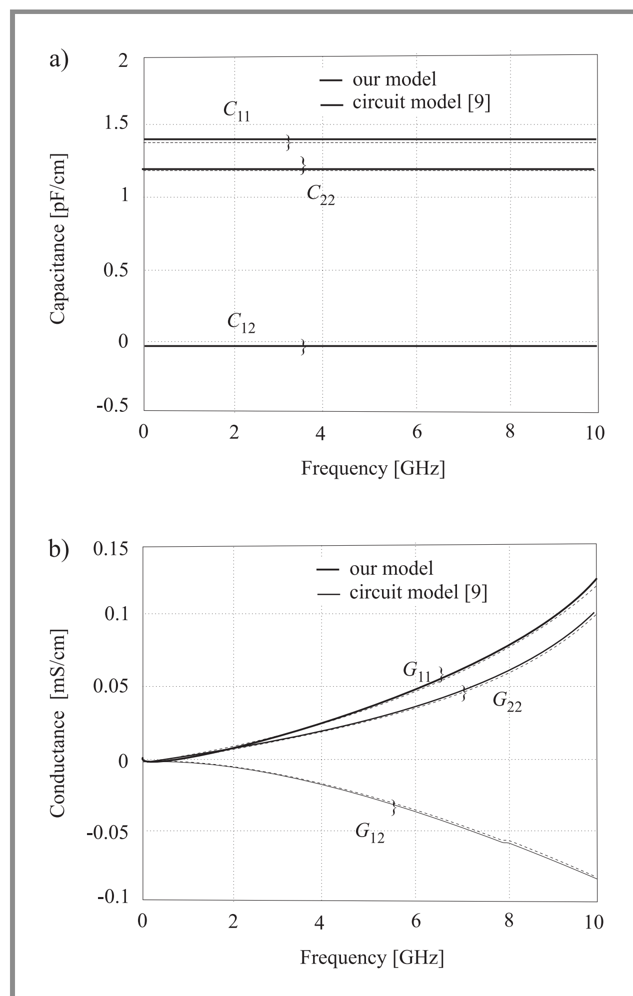


Fig. 5. (a) Self and mutual capacitance per unit length of asymmetric coupled interconnects on lossy silicon substrate; (b) self and mutual conductance per unit length of asymmetric coupled interconnects on lossy silicon substrate.

5. Conclusion

In this paper, we have discussed a technique for capacitance matrix extraction over a multilayer Si substrate. We derived the appropriate Green's function using quasi-static analysis and Fourier projection method. The potential function and electric induction vector components are defined as series expansions in terms of the Laplace equation which are periodic in the direction parallel to the plane of interconnect conductors. The proposed semi-analytical procedure allows us: first, to assess in an analytical and simple way the integral equations of the problem, and second, to obtain a fast convergence of the numerical results due to the averaging technique used in the Galerkin approach which leads to better accuracy in the numerical calculations. This method results in a very simple formulation of the problem that is well suited for computer solutions with relatively little programming effort.

References

[1] W. Y. Liu, K. Lan, and K. K. Mei, "Computation of capacitance matrix for integrated circuit interconnects using on-surface MEI method", *IEEE Trans. Microw. Guid. Wave Lett.*, vol. 9, pp. 303–304, 1999.

[2] Z. Zhu, W. Hong, Y. Chen, and Y. Wang, "Electromagnetic modeling and transient simulation of interconnects in high speed VLSI circuits", *IEEE Proc. Microw. Anten. Propag.*, vol. 143, pp. 373–378, 1996.

[3] E. Groteluschen, L. S. Dutta, and S. Zaage, "Full-wave analysis and analytical formulas for the line parameters of transmission lines on semiconductor substrates", *INTEGRATION, VLSI J.*, vol. 16, pp. 33–58, 1993.

[4] F. Stellari and A. L. Lacaita, "New formulas of interconnect capacitances based on results of conformal mapping method", *IEEE Trans. Electron. Dev.*, vol. ED-47, pp. 222–231, 2000.

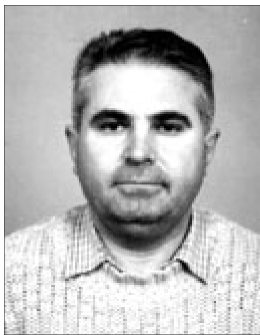
[5] C. Wei, R. F. Harrington, J. R. Mautz, and T. K. Sarkar, "Multiconductor transmission lines in multilayered dielectric media", *IEEE Trans. Microw. Theory Tech.*, vol. MTT-32, pp. 439–449, 1984.

[6] T. Sakurai, "Simple formulas for two- and three-dimensional capacitances", *IEEE Trans. Electron. Dev.*, vol. ED-40, pp. 118–124, 1993.

[7] C. P. Yan and T. N. Trick, "A simple formula for the estimation of the capacitance of two-dimensional interconnects in VLSI circuits", *IEEE Trans. Electron. Dev. Lett.*, vol. EDL-3, pp. 391–393, 1982.

[8] A. R. Djordjevic, M. B. Bazdar, T. K. Sarkar, and R. F. Harrington, *LINPAR: Matrix Parameters for Multiconductor Transmission Lines*. New York: Artech House, 1999.

[9] J. Zheng, Y.-C. Hahm, A. Weisshaar, and V. K. Tripathi, "CAD-oriented equivalent circuit modeling of on-chip interconnects for RF integrated circuits in CMOS technology", in *Proc. Int. Microw. Symp.*, Anaheim, USA, June 1999, pp. 35–38.



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