Invited paper

SiGe field effect transistors – performance and applications

Terrence E. Whall and Evan H. C. Parker

Abstract — Recent and encouraging developments in Schottky and MOS gated Si/SiGe field effect transistors are surveyed. Circuit applications are now beginning to be investigated. The authors discuss some of this work and consider future prospects for the role of SiGe field effect devices in mobile communications.

Keywords — SiGe, FETs, epitaxy, circuits.

1. Introduction

SiGe heterostructures are now firmly established in bipolar technologies, with a current market value of £30M per annum rising to £1.83B by 2005, driven by the wireless and optical communications sector [1]. SiGe also offers the exciting prospect of similar or even bigger commercial benefits in Si field effect transistors. The reasons for this optimism are based on the substantial gains in room temperature effective mobilities, shown in Figs. 1, 2 and 3, which accrue from strain-induced band structure modifications [2–4] in silicon, SiGe alloy and germanium epilayers. In this article, we examine the resulting performance gains in a number of devices based on these heterostructures, discuss some other potential benefits of a SiGe technology, and briefly survey some circuit applications.

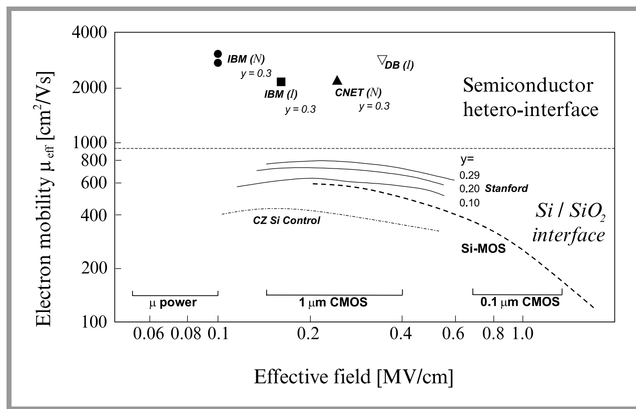

Fig. 1. Available experimental data on 300 K electron mobilities in strained Si grown on virtual substrates with terminating composition $Si_{1-x}Ge_y$ versus the effective field E_{eff} [2, 3]. $E_{eff} = \frac{e}{\varepsilon_s}\left[N_{depl} + \frac{1}{\beta}n_s\right]$ where ε_s is the absolute permittivity of Si, N_{depl} is the depletion charge density, and n_s is the carrier density. The upper section shows mobilities at remote doped hetero-interfaces and the lower section refers to oxide-gate/(tensile strained) Si interfaces. I denotes „inverted" modulation-doped structure (doping supply layer below strained silicon) and N denotes „normal" interface case (doping above silicon). The oxide-gated structures are operated in the inversion mode. Here $\beta = 2$.

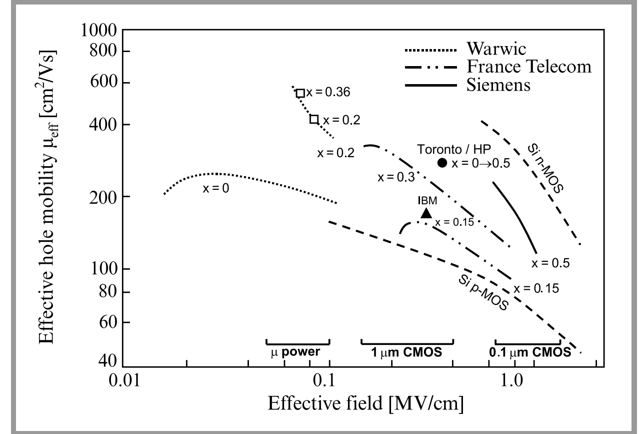

Fig. 2. Available experimental data on 300 K hole effective mobilities obtained in pseudomorphic $Si/Si_{1-x}Ge_y/Si$ structures plotted against effective field (E_{eff}), all data refer to buried SiGe channels except for the IBM sample where the gate dielectric was produced by plasma oxidation. The alloy composition in the Toronto/HP sample was graded. The squares refer to modulation-doped structures. The bars indicate the range of E_{eff} values present in micropower, 1 and 0.1 μm CMOS technologies. β is usually taken as 3 for holes [6], in order to obtain an universal curve independent of doping specifications. That practice is followed here, but we note that this tends to over-emphasise the superiority of the electron channel where β is chosen as 2.

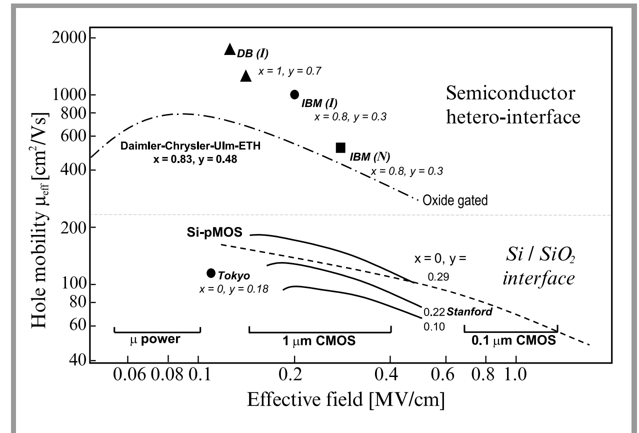

Fig. 3. Available experimental data on 300 K hole mobilities obtained in compressively strained $Si_{1-x}Ge_y$ and tensile strained Si grown on virtual substrates with terminating composition structures $Si_{1-x}Ge_y$. The upper section shows mobilities for remote doped hetero-interfaces and the lower section refers to oxide-gate/(tensile strained) Si interfaces. I denotes „inverted" and N denotes „normal" interface. The oxide-gated data refer to inversion layers. $\beta = 3$.

2. Strained silicon n-channel devices

Ismail et al [5] have fabricated an 0.4 μm gate length Schottky gated modulation doped FET or n-MODFET with a peak transconductance of 420 mSmm^{-1}, an f_T of 40 GHz and an f_{max} of 56 GHz, comparable to GaAs/AlGaAs HEMTs of the same gate length. Figure 4 shows a typical Si/SiGe n-MODFET, designed and fabricated by the Daimler-Chrysler group [6]. The strained Si is supplied

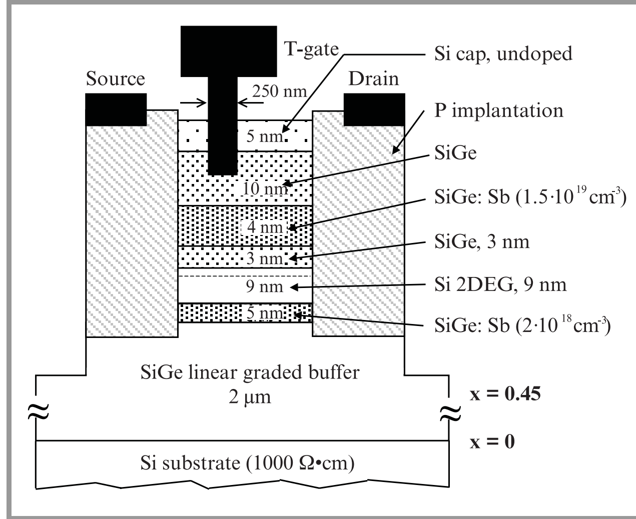

Fig. 4. Schottky gated modulation doped n-channel FET (n-MODFET). The conduction band offset in the strained Si layer confines electrons. The T gate recess determines the threshold voltage, allowing either d-mode or e-mode operation (*after Glück et al. [6]*).

with carriers by SiGe:Sb doped layers above and below the quantum well. The device can operate in either depletion or enhancement mode depending on the depth of the Pt/Au Schottky gate recess, with a deeper recess in the latter case. An 0.25 μm d-mode device gives a measured f_T of 70 GHz and an f_{max} of 120 GHz (*U. König, private communication*). Simulations [7] suggest transconductances up to 1000 mSmm^{-1} and transit frequencies f_T above 200 GHz in self aligned layouts with gate lengths < 0.1 μm. Figure 5 shows the simulations of f_T. It is apparent that velocity overshoot plays an important role at gate lengths of 0.1 μm and below, particularly in the heterostructure.

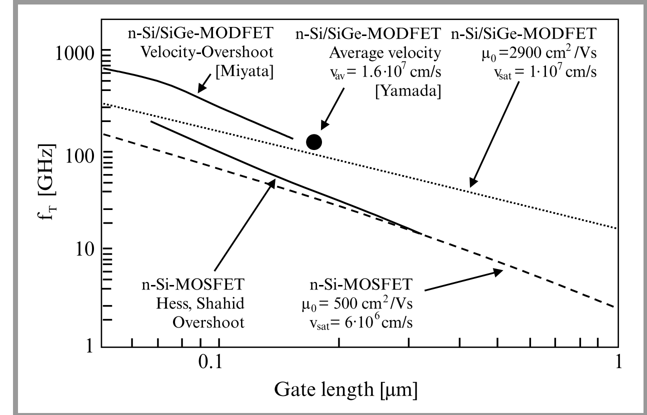

Fig. 5. Simulated transit frequencies of SiGe n-MODFETs compared to ordinary SiGe n-MOS (*after König et al. [7]*).

The Stanford group have used CVD at 750°C to grow a strained Si channel on a relaxed $Si_{0.8}Ge_{0.2}$ strain-tuning virtual substrate (VS), and have fabricated an n-MOSFET of channel length 0.1 μm [8]. This is illustrated in Fig. 6a. The VS is in-situ boron-doped to create a punchthrough stopper doping profile surrounded by $Si_{0.8}Ge_{0.2}$ of lower doping. A very steep profile is possible because the boron diffusivity in both strained and relaxed $Si_{0.8}Ge_{0.2}$ is 8 times lower than in bulk Si. In the unstrained Si control sample SiGe boron diffusion barriers are placed either side of the p-layer, as shown in Fig. 6b. The doping profiles obtained

give comparable short channel behaviour in heterostructure and control with a DIBL value of approx 0.8, threshold voltage shift of approx 0.1 V and subthreshold slope of $103 \div 110$ mV per decade. Transconductance enhancement in the heterostructure device is 60%, and average velocity (a measure of f_T) 67% as shown in Fig. 7. This improved performance [9] corresponds to a mobility enhancement of 70% at an effective field as high as 1 MV/cm and substantial velocity overshoot associated with a 100% increase in the energy relaxation time.

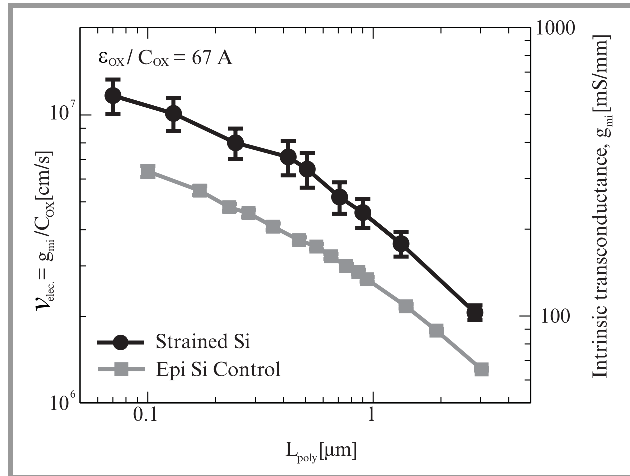

Fig. 7. Average channel velocities and intrinsic transconductances of the devices shown in Fig. 6 (*after Rim et al. [8]*).

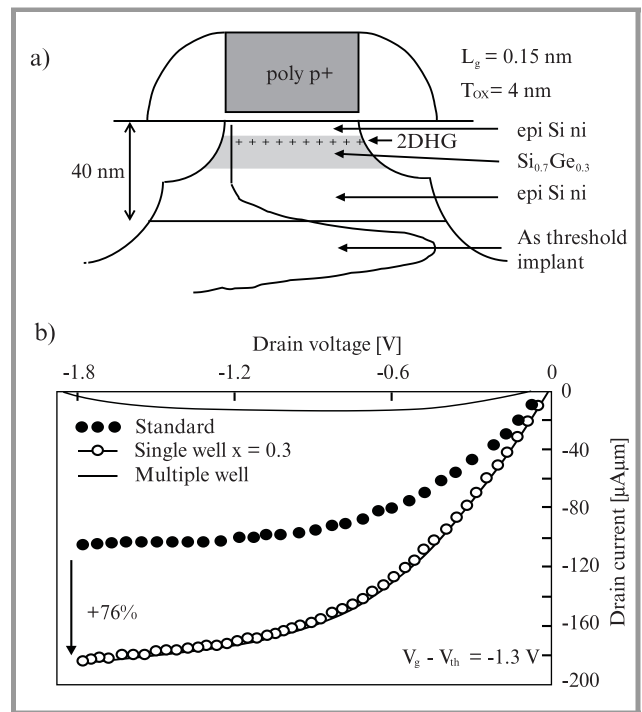

Fig. 8. Device architecture (a) and current drive capability (b) of fully pseudomorphic $Si/Si_{0.7}Ge_{0.3}/Si$ p-MOSFET. The valence band offset relative to silicon confines the carriers in the alloy. Also shown is the current drive enhancement as compared to silicon for a Si/SiGe multi quantum well structure (*after Alieu et al. [11]*).

3. Strained $Si_{1-x}Ge_x$ ($0 \leq$ and ≤ 1) p-channel devices

Modern circuits for analogue and digital performance demand both n- and p-channel devices but the poor performance of the latter is an impediment to even better circuitry. Indeed, a major theme at the recent (December 1999) *International Electronic Devices Meeting (IEDM)* concerned the Si p-MOS device, which is the Achilles heel of Si CMOS. Factors of two or more reduction in current drive or transconductance as compared to Si n-MOS were reported in about a dozen papers concerned with deep submicron devices (50 nm $< L_{eff} \lesssim$ 100 nm) and theoretical work [10] indicated that the factor of two represented a lower limit. SiGe offers a unique opportunity to obtain matching n- and p-channel performance for the first time.

The fully pseudomorphic Si/SiGe/Si sandwich structure, because of its simplicity, has received a lot of attention for enhanced p-channel performance. It is a relatively defect-free structure which avoids the problems associated with the $Si_{1-y}Ge_y$ virtual substrate of long growth times and comparatively poor thermal conductivity. The CNET group have fabricated [11] such a device within an 0.15 μm CMOS process and this is sketched in Fig. 8a. It uses a p^+ poly-gate with a 4 nm gate oxide, and In or As implants for threshold voltage adjustment. They obtain a 76% improvement in current drive compared to a bulk silicon standard, as shown in Fig. 8b. The Cornell group report an f_T of 23 GHz and an f_{max} of 35 GHz in $Si/Si_{0.6}Ge_{0.4}/Si$ 0.2 μm gate length p-MOS device [12]. They compare their f_T value with measurements on a bulk Si n-MOSFET of similar geometry, which gave 32 GHz. A novel solid-phase epitaxy process has been used [13] to form an ultra thin body SOI p-channel $Si/Si_{0.7}Ge_{0.3}$ MOSFET, which is shown in Fig. 9a. Negligible threshold voltage roll-off and a subthreshold slope of 100 mV/dec is obtained for a channel length of 50 nm. The incorporation of SiGe in the channel (graded from 0 at the bottom to 30% at the top) results in a 70% enhancement in drive current, Fig. 9b. The authors note that further increases in drain current can be expected if the series resistance is reduced by process optimisation.

A Glasgow/Loughborough/Warwick team have been investigating the factors which limit current drive and transconductance in SiGe p-MOS devices. Measurements on an $x = 0.5$ structure of uniform composition, fabricated at Infineon (Munich), Fig. 10, have been compared with theory by Kearney et al. [14] and it is concluded that interface roughness rather than alloy scattering dominates the mobility at both 4 K and 300 K. Further arguments in favour of this viewpoint are given by Whall and Parker [15]. Figure 11 shows measurements of effective mobility by Palmer

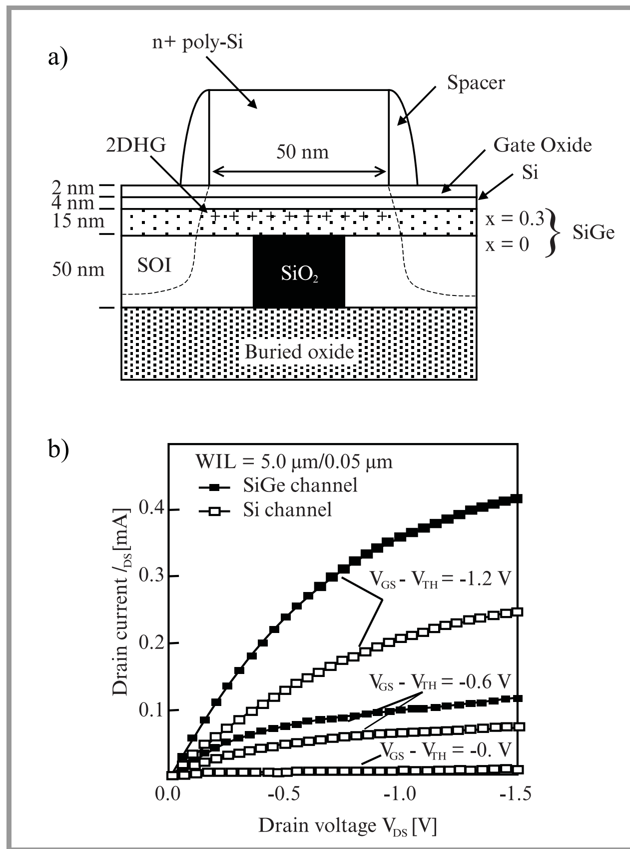

Fig. 9. (a) Ultra-thin-body silicon on insulator MOSFET incorporating SiGe strained layer. A trench is formed in the SOI wafer, $Si0_2$ is deposited by low-pressure CVD and then SiGe is deposited and crystallised by solid-phase epitaxy. The broken lines indicate the boundaries of the source and drain islands. (b) Showing 70% enhancement in current drive as compared to silicon (*after Yee Chia Yeo et al. [13]*).

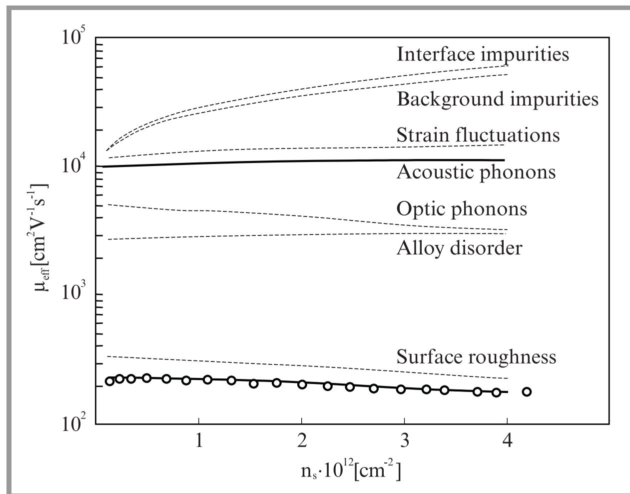

Fig. 10. Room temperature effective mobility of a $Si/Si_{0.5}Ge_{0.5}/Si$ p-MOSFET versus carrier density. O experiment: broken lines theory, continuous line resultant theoretical mobility (*after Kearney et al. [14]*).

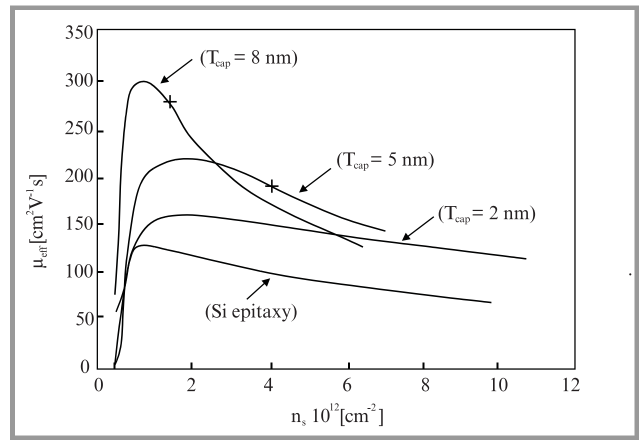

Fig. 11. Measurements of effective mobility versus carrier density in $Si/Si_{0.64}Ge_{0.36}/Si$ p-MOSFETs of various Si cap thicknesses, compared with a Si control. The crosses indicate the onset of parasitic conduction in the Si cap (*after Palmer et al. [16]*).

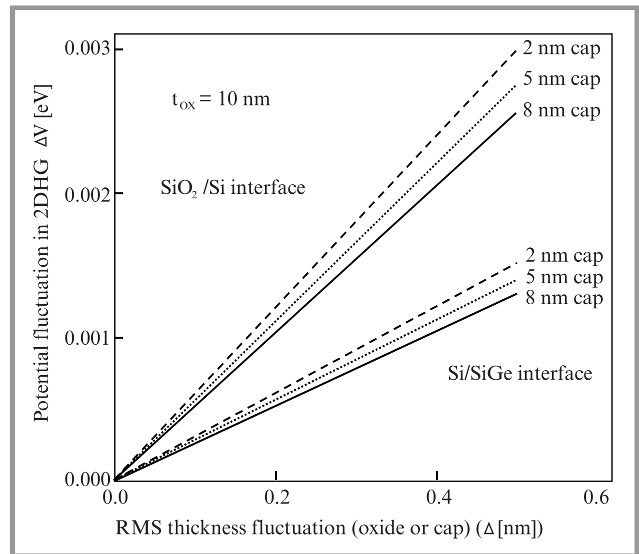

Fig. 12. Coulomb potential fluctuations in the $Si_{0.64}Ge_{0.36}$ quantum well due to random thickness variations in the oxide and Si cap layers, giving rise to interface roughness scattering. A carrier density of $1 \cdot 10^{12}$ cm^{-2} is chosen to avoid the complication of parasitic conduction in the silicon cap (*after Palmer et al. [16]*).

et al. [16] on $x = 0.36$ devices of various Silicon cap thicknesses. They argue that, for the devices in question, the potential fluctuations in the SiGe channel which limit the mobility, Fig. 12, are associated mainly with $Si0_2$/Si as opposed to Si/SiGe interface roughness, in contrast to what is usually claimed. Ge segregation during growth and/or diffusion during processing degrades the Si/$Si0_2$ interface, presumably because of snowploughing of the Ge during oxidation, leading to increased roughness scattering. Thicker silicon caps lead to better $Si0_2$/Si interfaces and higher peak mobilities. At high carrier densities, however, the thicker Si caps are populated, leading to a fall in effective mobility. A device configuration which has merit, is shown in Fig. 13. It uses an n$^+$ poly-Si gate and a B doping layer beneath the SiGe channel to suppress parallel conduction

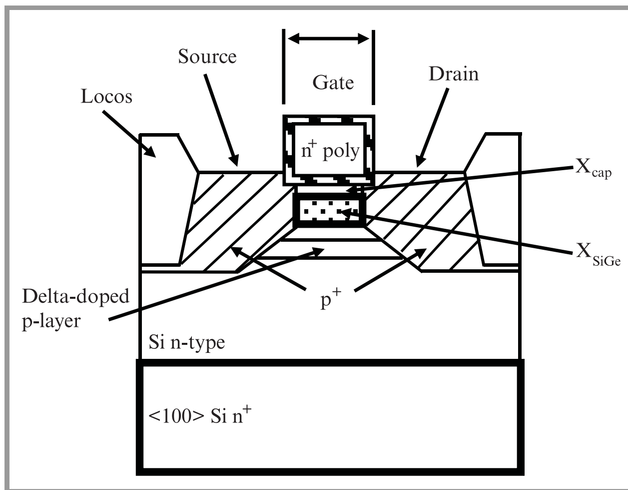

Fig. 13. p-channel Si/SiGe/Si e-mode MOSFET with n^+ poly Si gate and Si:B doping layer to reduce effective (vertical) field and allow thicker Si cap.

in the cap while maintaining a low threshold voltage for enhancement mode operation. Because a thicker silicon cap becomes possible, it should be more tolerant of any Ge segregation. The B doping layer reduces the vertical effective field E_{eff}, which should give higher mobilities. Co-evaporation of C is being used by the Warwick group to stabilise the B against segregation and also diffusion. The velocity field characteristics reported by Kaya et al. [17] on an $x = 0.2$ SiGe p-MOS device, and reproduced in Fig. 14, are consistent with the view that, although the bulk saturation velocity in SiGe is less than that in Si, velocity overshoot affects dominate at short channel lengths and are responsible for the enhanced device performances discussed above. Zhao et al. [18] confirm this behaviour and also report that the observed velocity overshoot effects increase with mobility. Further improvements in device performance should be possible by engineering the doping

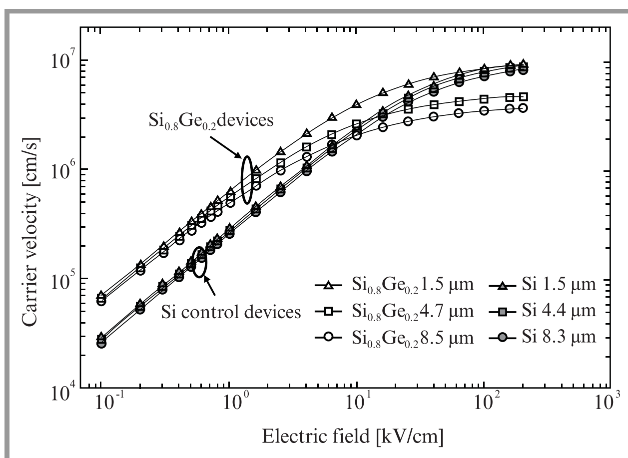

Fig. 14. Carrier velocity versus horizontal field, extracted from measurements on thick oxide (140 nm) $Si_{0.8}Ge_{0.2}$ p-MOSFETs and by comparison with a drift diffusion model (*after Kaya et al. [17]*).

distributions to increase the velocity at the source end of the channel.

A number of other factors could tip the scales in favour of SiGe. The increased solid solubility and low diffusivity of B in SiGe promises shallow low resistance source and drain contacts [19]. SiGe sources have been demonstrated to suppress parasitic bipolar action and punchthrough [20, 21]. Poly SiGe gates [22] exhibit reduced gate-depletion, reduced boron penetration and give increased current through reduction of E_{eff}. Measurements by the Warwick group on a Siemens Si/$Si_{0.5}Ge_{0.5}$/Si p-MOSFET give two orders of magnitude improvement in the relative $1/f$ noise, as shown in Fig. 15, which may be associated with the displacement of the Fermi level in the heterostructure [23].

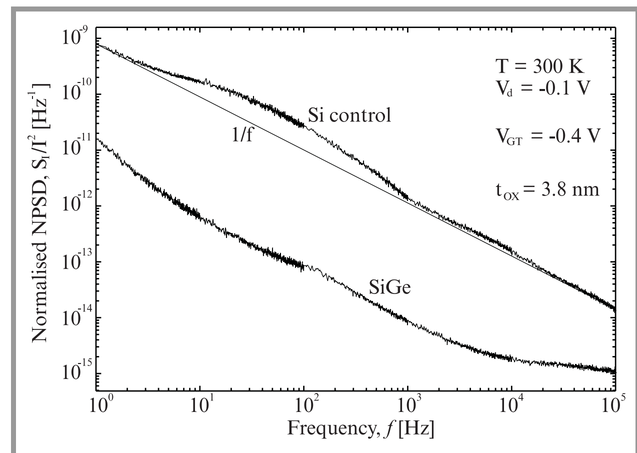

Fig. 15. Showing two orders of magnitude improvement in relative noise power spectral density (NPSD) in a Si/$Si_{0.5}Ge_{0.5}$/Si MOSFET as compared to a Si control (*after Prest et al. [23]*).

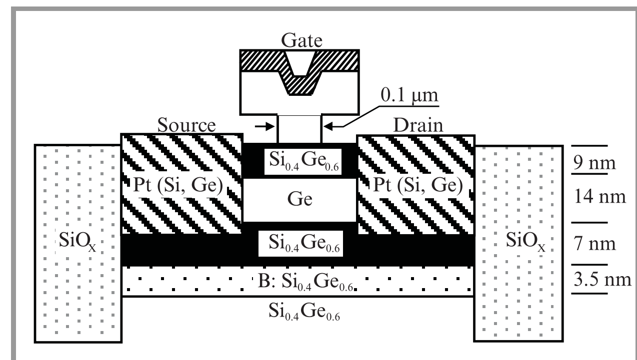

Fig. 16. 0.1 μm gate length strained Ge p-MODFET. Contact pad metallisation not shown (*after Hammond et al. [26]*).

Even more dramatic performance enhancements might be expected in high Ge content and pure Ge strained layers on VS. The Daimler-Chrysler group et al. [24] have fabricated strained $Si_{0.3}Ge_{0.7}$ and Ge p-MOS and p-MODFETs on VS. A novel Ge p-MOS device yielded an f_T of 59 GHz and an f_{max} of 126 GHz at a gate length of 0.1 μm (*U. König, private communication*). The f_T value is close to that in ordinary Si n-MOS [25]. A recent IBM 0.1 μm Ge p-MODFET is shown in Fig. 16. Transconductances of up

to 488 mS/mm at a drain source voltage as low 0.6 V were obtained [26]. For comparison ordinary 0.1 μm Si p-MOS exhibits a transconductance of 320 mS/mm at 1.5 V [25]. An 0.15 μm self aligned $Si_{0.2}Ge_{0.8}$ p-MOS structure, using SiN for the gate dielectric [27], displayed a maximum transconductance of 305 mS/mm an f_T of 62 GHz at low drain source voltage of 0.75 V (compared to approximately 30 GHz at 1.5 V in Si [25]) and an f_{max} of 68 GHz.
We have omitted to mention strained p-channel FETs in this article, which have also shown promise. The reader is referred to the review of Maiti and co-workers [29].

4. Some potential circuit applications

n-type Si/SiGe MODFETs promise improved performances comparable to III-V based circuits in analogue RF circuits and could play an important role in communication systems where they might be used as, for example, front and photoreceivers or low noise amplifiers. Saxarra et al. [29] have fabricated a transimpedance amplifier, based on the n-MODFET described in Section 2, the circuit of which is shown in Fig. 17. It consists of two stages, the input common-source stage having drain to gate feedback to

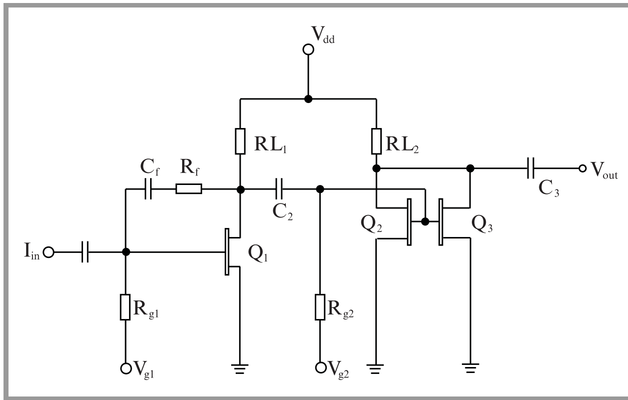

Fig. 17. Two stage transimpedance amplifier using n-MODFETs sketched in Fig. 4.

transform current to voltage. The second stage amplifiers the output voltage of the first stage and uses two transistors to increase the gain. Spice simulations suggest a 3 dB Ω bandwidth of 4.84 GHz with a gain of 64.7 dB Ω for a power supply voltage of 5 V and for a feedback resistor of 1.5 kΩ, assuming ideal impedance matching. On the other hand, using a feedback resistor of 540 Ω, the maximum bandwidth measured is 1.8 GHz and the gain is 56 dB Ω. The performance shortfall is attributed in part to non-optimum oxide passivation and non-ideal impedance matching. A similar device has been used by Ostermann et al. [30] to fabricate an inverter circuit, Fig. 18. Q_1 is a common source amplifier which feeds on active load Q_2. The gate delay is 28 ps for 180 nm gate length, 100 μm gate width, and power supply voltage $V_{DD} = 2$ V.
SiGe CMOS offers for the first time the possibility of speeds to approach and match that of GaAs technology while at

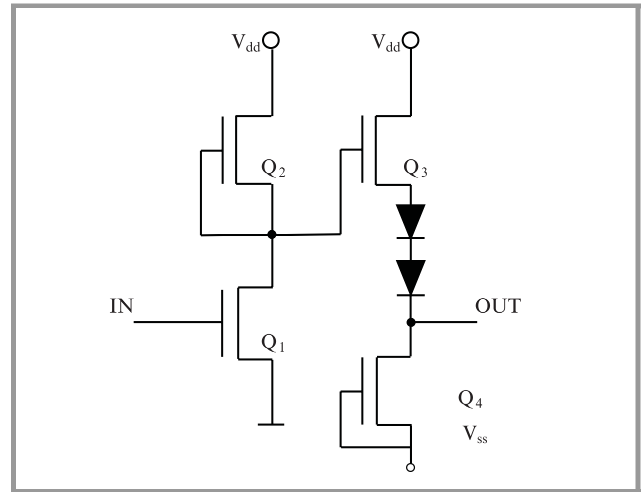

Fig. 18. Inverter circuit with source follower, using n-MODFETs sketched in Fig. 4. Q_2 and Q_4 are active loads.

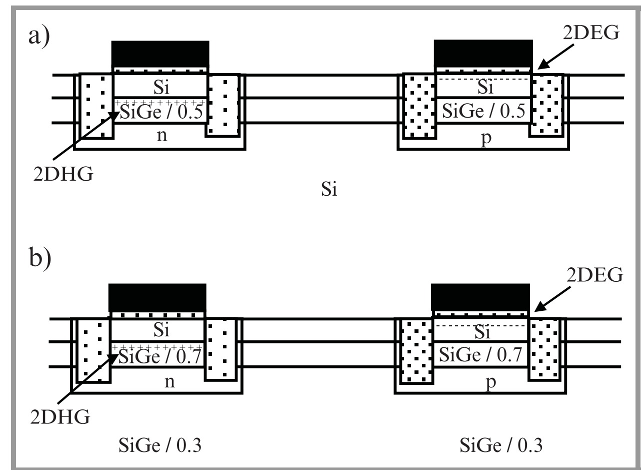

Fig. 19. Si/SiGe CMOS process options: (a) giving enhanced p-channel performance, (b) giving enhanced n-channel performance and further enhancement of p-channel performance.

the same time offering p-channel and enhancement mode devices, not available in GaAs, simplifying circuit design. Figures 19a and 19b show, respectively, two process options for (a) a fully pseudomorphic CMOS technology of enhanced p-channel performance and (b) a VS one having both improved n and p-channel performance. A CNET group [11] and a Southampton/Warwick Group [32] have independently attempted the fabrication of a CMOS configuration of type (a). Whereas enhanced p-channel performance was demonstrated in the CNET device, Ge segregation and/or diffusion degraded the performance of the surface n-channel. Similarly, the Southampton p-channel showed enhanced transconductance but the n-channel device properties were poor due to unsuccessful attempts to find a low thermal budget oxide. Nevertheless, these are first attempts and the outlook is promising. As far as we are aware no work has yet been carried out on configuration (b).

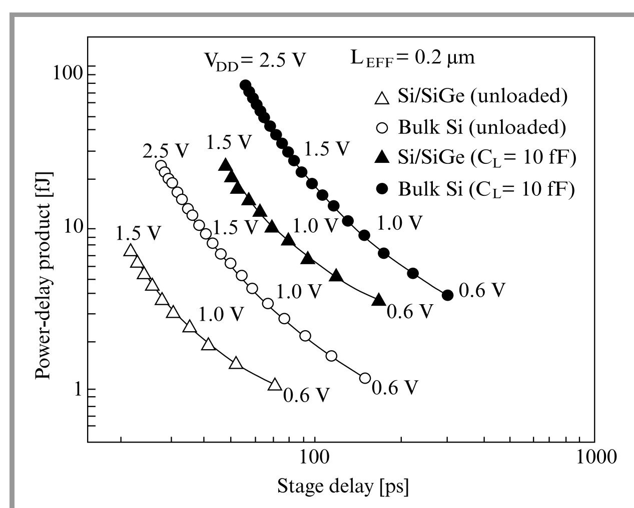

Fig. 20. Simulated power delay product versus stage delay for a Si/SiGe CMOS configuration, based on strained silicon and strained SiGe alloy layers, given enhancements in both n- and p-channel current drive (*after Armstrong et al. [34]*).

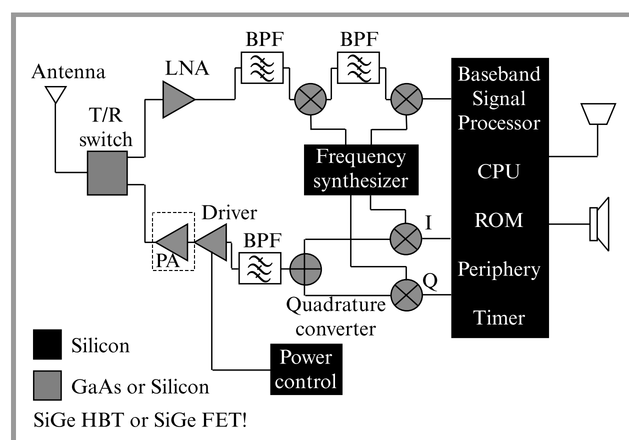

Fig. 21. Building blocks of a digital handset (*after Costa [35]*). The areas where SiGe FETs could compete are shown shaded.

Voinigescu et al. [33] have calculated the 3-stage ring oscillator delay for a fully pseudomorphic Si/SiGe 0.25 μm CMOS technology, and for a supply voltage of 2.5 V. Their calculations are based on a fully graded SiGe channel, the Ge fraction varying from 0 at the bottom to 0.5 at the top of the structure, the effective mobility [34] of which is shown in Fig. 2. They obtain a delay of 33 ps per stage compared to 50 ps for the Si CMOS circuit. The power delay products have been calculated by Armstrong et al. [35] for a VS based Si/SiGe CMOS configuration similar to that shown in Fig. 19b and for bulk Si CMOS, and are compared in Fig. 20. The authors assume channel lengths of 0.2 μm, gate oxide thicknesses of 5 nm and low field mobilities of 2500 $cm^2V^{-1}s^{-1}$ and 800 $cm^2V^{-1}s^{-1}$ for SiGe n-MOS and p-MOS. Factors of 1.23 and 2.25 increases are predicted for n-MOS and p-MOS current drive respectively. The drain current saturates at a low drain bias of 0.4 V for SiGe n-MOS and 0.8 V for SiGe p-MOS. This cuts down the power consumption by up to a factor of 3 or 4! The high carrier mobilities result in a factor of 6.4 improvement in power delay product for the unloaded case and a factor of 4.6 improvement at a delay of 55 ps for the loaded case compared to bulk Si. It is noted that the performance advantage derives largely from the increased current drive of the SiGe p-MOS channel.

The huge and wide ranging markets in wireless and optical communications offer plenty of opportunities for a SiGe FET technology. The digital wireless handset [36] shown in Fig. 21 may be used to illustrate the potential advantages of SiGe MOS technology, since it contains numerous important building blocks in mobile communications. GaAs currently predominates in the RF section containing the power amplifier (PA), driver amplifier, low noise amplifier (LNA) and transmit/receive (T/R) switch, and competes with silicon in the mixer sections. It is currently being challenged by the SiGe HBT in all these areas. A preferred solution, capable of giving higher levels of integration and lower power consumption is Si CMOS [37]. The incorporation of SiGe into CMOS may be what is needed for this to happen. As the technology matures we might expect that SiGe will bring the high f_T, f_{max}, better linearity and HF noise needed by the LNA. Switched capacitor circuits are promising candidates for band pass filters (BPF). Here the faster switching speed and low power consumption of SiGe CMOS could be of benefit. The good $1/f$ noise properties referred to in Section 3 could lead the development of low-phase noise local oscillators for the frequency synthesiser. The transmitter power amplifier places particularly onerous demands on Si CMOS. However, good progress is being made in this respect with ordinary Si. For example, an 0.4 μm Si n-MOS 2 GHz amplifier has been demonstrated with 1 W output power, 50% PAE at 3.6 V, with satisfactory linearity and a breakdown voltage of 15 V [38]. SiGe should, in principle, be able to significantly improve on these figures.

5. Conclusions

The current performance indicators for Si/Ge are such that it offers serious prospects of making significant inroads into, or even displacing, the more mature bulk silicon technology. An example of an early application would be in mobile telephony. Much work is still needed on design, growth and processing before this can happen.

Acknowledgements

The authors have had stimulating and valuable discussions with A. Asenov, J. Barker, A. Evans, K. Fobelets, M. J. Kearney, U. König, A. O'Neill and C. Pappavasilou.

References

[1] R. Dixon, „Silicon germanium", *Compound Semicond.*, vol. 7(1), p. 72, 2000.

[2] E. H. C. Parker and T. E. Whall, „SiGe heterostructure CMOS circuits and applications", *Solid State Electron.*, vol. 43, p. 1497, 1999.

[3] T. E. Whall and E. H. C. Parker, „SiGe heterostructures for FET applications", *J. Phys. D. Appl. Phys.*, vol. 31, p. 1397, 1998.

[4] G. Hock, E. Kohn, C. Rosenblad, H. von Känel, H.-J. Herzog, and U. König, „High hole mobility in $Si_{0.17}Ge_{0.83}$ channel metal-oxide-semiconductor field-effect transistors grown by plasma-enhanced chemical vapour deposition", *Appl. Phys. Lett.*, vol. 76(26), p. 3920, 2000.

[5] K. Ismail, „Si/SiGe high speed field-effect transistors", *IEDM Tech. Dig.*, vol. 95, p. 509.

[6] M. Glück, T. Hackbarth, M. Birk, A. Haas, E. Kohn, and U. König, „Design and fabrication of SiGe n-type MODFETs Physica E: Low Dimensional Systems and Nanostructures", vol. 763, 1998.

[7] U. König, M. Glück, A. Grable, G. Hock, E. Kohn, B. Bozon, D. Nuernbergk, T. Ostermann, and R. Hagelauer, „Design rules for n-type SiGe hetero FETs", *Solid State Electron.*, vol. 41(10), p. 1541, 1997.

[8] K. Rim, J. L. Hoyt, and J. F. Gibbons, „Transconductance enhancement in deep submicron strained Si n-MOSFETs", *IEDM Tech. Dig.*, vol. 98, p. 707.

[9] K. Rim, J. L. Hoyt, and J. F. Gibbons, „Fabrication and analysis of deep submicron strained Si n-MOSFETs", *IEEE Trans. Electron Dev.*, vol. 47(7), pp. 1406–1415, 2000.

[10] F. Assad, Z. Ren, S. Datta, and M. Lundstrom, „Performance limits of silicon MOSFETs", *IEDM Tech. Dig., 1999* (to be published).

[11] J. Alieu, T. Skotnikii, J. L. Regolini, and G. Bremond, „Multiple SiGe quantum, wells – novel channel architecture for 0.12 μm CMOS", in *Proc. 29th Eur. Solid State Dev. Res. Conf.*, Leuven, Belgium, Sept. 1999, p. 292.

[12] K. Bhaumik, Y. Shacham-Diamand, J. P. Noel, J. Bevk, and L. C. Feldman, „23 GHz f_T room temperature SiGe quantum well p-MOSFETs", in *Proc. NRC IMS Epit. Meet.*, Ottawa, March 1994, p. 349.

[13] Yee Chia Yeo, Vivek Sabramanian, J. Kedzierski, Peiqi Xuan, Tsu-Jae King, Jeffrey Bokor, and Chenning Hu, „Nanoscale ultra-thin-body silicon-on-insulator p-MOSFET with SiGe/Si heterostructure channel", *IEEE Electron Dev. Lett.*, vol. 21, p. 161, 2000.

[14] M. J. Kearney, A. I. Horrell, H. Fischer, L. Risch, E. H. C. Parker, and T. E. Whall, „Improved room temperature mobility in a coherently strained $Si/Si_{0.5}/Ge_{0.5}/Si$ p-channel field effect structure", *Appl. Phys. Lett.* (submitted, Sept. 2000).

[15] T. E. Whall and E. H. C. Parker, „Si/SiGe/Si pMOS performance – alloy scattering and other considerations", *Thin Solid Films*, vol. 368, pp. 297–305, 2000.

[16] M. J. Palmer, G. Braithwaite, T. Grasby, P. J. Phillips, M. J. Prest, E. H. C. Parker, T. E. Whall, C. P. Parry, A. M. Waite, A. G. R. Evans, S. Roy, J. R. Watling, S. Kaya, and A. Asenov, „Effective mobilities in pseudomorphic SiGe p-channel MOSFETs with thin silicon capping layers", *Appl. Phys. Lett.* (submitted, Sept. 2000).

[17] S. Kaya, Y.-P. Zhao, J. R. Watling, A. Asenov, J. R. Barker, G. Ansaripour, G. Braithwaite, E. H. C. Parker, and T. E. Whall, „Indication of velocity overshoot in strained $Si_{0.8}Ge_{0.2}$ p-channel MOSFETs", *Semicond. Sci. Technol.*, vol. 15, p. 573, 2000.

[18] Y.-P. Zhao, S. Kaya, J. R. Watling, A. Asenov, J. R. Barker, M. Palmer, G. Braithwaite, E. H. C. Parker, T. E. Whall, A. Waite, and A. G. R. Evans, „Indication of non-equilibrium transport in SiGe p-MOSFETs", in *Proc. 30th Eur. Solid State Dev. Res. Conf. (ESSDERC),* Cork, 2000, pp. 224–227.

[19] Hideki Takeuchi, Wen-Chin Lee, Pushkar Ranade, and Tsu-Jae King, „Improved pMOSFET short-channel performance using ultra-shallow $Si_{0.8}Ge_{0.2}$ source/drain extensions", *IEDM Tech. Dig.*, 1999 (to be published).

[20] Z. Y. Wu, S. Hall, and W. Eccleston, „Suppression of parasitic bipolar action in deep submicron MOSFETs by the use of a narrow band gap source", in *Proc. 25th ESSDERC*, Sept. 1995.

[21] R. M. Sidek, A. G. R. Evans, and R. A. Kubiak, „Reduction of parasitic bipolar action and punchthrough in MOSFETs using Si/SiGe sources and drains", *Electron Lett.*, vol. 32, p. 269, 1996.

[22] Wen-Chin Lee, B. Watson, Tsu-Jae King, and Chenning-Hu, „Enhancement of pMOS device performance with poly-SiGe gate", *IEEE Electron Dev. Lett.*, vol. 20, p. 232, 1999.

[23] M. Prest, C. Brown, H. Fischer, L. Risch, B. Jones, E. H. C. Parker, and T. E. Whall, „Low 1/f noise in a $Si/Si_{0.5}Ge_{0.5}/Si$ pMOSFET", *Electron Dev. Lett.* (submitted, Sept. 2000).

[24] M. Glück, T. Hackbarth, U. König, A. Haas, G. Hock, and E. Kohn, „High f_{max} n-type Si/SiGe MODFETs", *IEEE Electron. Lett.*, vol. 33(4), p. 355, 1997.

[25] Yuan Taur, A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, S.-H. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H.-J. C. Wann, S. J. Wind, and H.-S. Wong, „CMOS scaling into the nanometre regime", *Proc. IEEE*, vol. 85(4), p. 486, 1997.

[26] R. Hammond, S. J. Koester, and J. O. Chu, „Extremely high transconductance $Ge/Si_{0.4}Ge_{0.6}$ pMOSFETs grown by UHV-CVD", *IEEE Electron Dev. Lett.* (to be published).

[27] W. Lu, R. Hammond, S. J. Koester, X. W. Wang, J. D. Chu, T. P. Na, and I. Adesida, „High performance 0.15 self aligned SiGe p-MOS-MODFETs with SiN gate dielectric", *IEDM Tech. Dig.*, 1999 (to be published).

[28] C. K. Maiti, L. K. Bera, and S. Chattopadhyay, „Strained-Si heterostructure field-effect transistors", *Semicond. Sci.Tech.*, vol. 13, p. 1225, 1998.

[29] M. Saxarra, M. Glück, J. N. Albers, D. Behammer, U. Langmann, and U. König, „Transimpedance amplifiers based on Si/SiGe MODFETs", *Electron Lett.*, vol. 34(5), p. 49, 1998.

[30] T. Ostermann, M. Glück, R. Hagelauer, U. König, M. Dobersberger, M. Birk, and F. Vehler, „Inverter circuits with Si/SiGe n-type MODFETs", in *Proc. Int. Semi. Dev. Res. Symp.*, Charlottesville, Va, 1997.

[31] R. M. Sidek, U. N. Straube, A. M. Waite, A. G. R. Evans, C. Parry, P. Philips, T. E. Whall, and E. H. C. Parker, „SiGe CMOS fabrication using SiGe MBE and an anodic/LTO gate oxide", *Semicond. Sci. Tech.*, vol. 15, p. 135, 2000.

[32] S. Voinigescu, P. Rabkin, C. A. T. Salama, A. Tcherniaev, R. Cottle, and P. Blakey, „Submicron Si/SiGe CMOS circuit potential determined using mixed-mode device-circuit simulation", *Simulat. Standard*, vol. 4(5), 1993.

[33] S. Voinigescu, C. A. T. Salama, J. P. Noel, and T. I. Kamins, „Si/SiGe heterostructure pMOSFET with triangular Ge channel profiles", *IEDM Tech. Dig.*, vol. 94, p. 369.

[34] M. A. Armstrong, D. A. Antoniadis, A. Sadek, K. Ismail, and F. Stern, „Design of Si/SiGe heterostructure complementary metal-oxide-semiconductor transistors", *IEDM Tech. Dig.*, vol. 95, p. 7861.

[35] J. C. Costa, „Heterostructure FETs for digital wireless communications", *Compound Semicond.*, vol. 5(4), p. 42, 1999.

[36] B. Razavi, „Challenges in portable RF transceiver design", *IEEE Trans. Circ. Dev.*, vol. 2, p. 12, 1996.

[37] Isao Yoshida, „2 GHz Si power MOSFET technology", *IEDM Tech. Dig.*, vol. 97, p. 51.

Terrence E. Whall – BSc(Hons), City University 1964, D Phil, University of Sussex 1969; Research Fellow London University 1969–71, Lecturer/Senior Lecturer Portsmouth University 1971–87, Lecturer 1987–89, Senior Lecturer 1989–95, Reader 1995–98, Personal Chair 1998-, Department of Physics, University of Warwick. Research Profile:

Research career devoted to experimental investigations of the synthesis and electrical properties of a wide range of materials. Since 1987 has lead the electrical characterisation and device physics work in the Semiconductor Group at Warwick. Along with Professor Parker spearheaded the UK consortium research activity (involving seven universities, UK/German industry) evaluating the prospects for SiGe MOS technologies. Has given numerous invited talks and has produced over 200 publications.
e-mail: T.E.Whall@warwick.ac.uk
Department of Physics
University of Warwick
Coventry CV4 7AL, UK

Evan H. C. Parker – Dip. Tech(Hons), City University 1964, D Phil University of Sussex 1968; Research Scientist – Zenith Radio Research Corporation 1968–1971; Lecturer (1971, Senior Lecturer 1976), Sir John Cass Reader 1984–86, Sir John Cass College of Science and Technology, London. Professor of Semiconductor Physics 1986-present, Department of Physics, University of Warwick. Leader: Semiconductor Research Group (currently 20 personnel). Research Profile: Since 1978 have worked on thin semiconducting layers – PbTe, InGa, GaAs, and since 1980 Si, SiGe and SiGeC. The work of the semiconductor group is concerned with the study of MBE growth and the physics and device properties of Si-SiGe-SiGeC heterostructures. Along with Professor Whall he spearheaded a consortium research activity (involving nine universities, UK/German industry) evaluating the prospects for SiGe MOS technologies. AVS Prize 1983. Chaired/co-chaired several of the international symposia on Si-MBE, given numerous invited talks, produced over 250 publications (including two books and several Editorships) and has acted as a consultant for UK, German and Japanese industry.
e-mail: E.H.C.Parker@warwick.ac.uk
Department of Physics
University of Warwick
Coventry CV4 7AL, UK

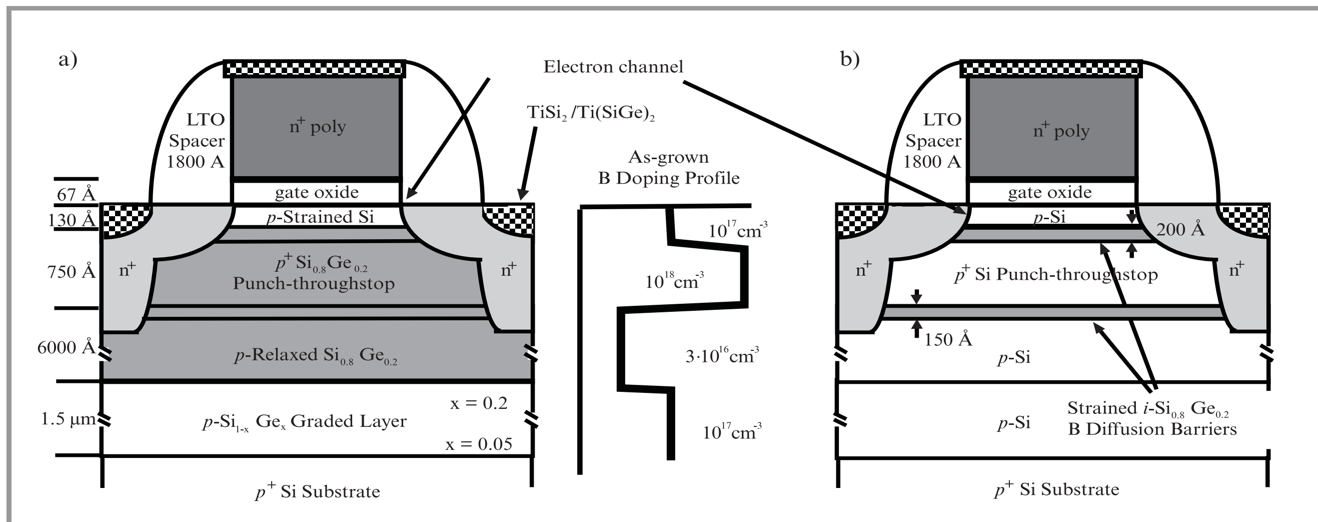

Fig. 6. Showing (a) strained Si n-MOSFET and (b) unstrained Si control device structures. Boron profile control is aided by $Si_{0.8}Ge_{0.2}$ diffusion barriers in each case (*after Rim et al. [8]*).