Paper

Comparison of gate leakage current components in metal-insulator-semiconductor structures with high-k gate dielectrics

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Abstract — Numerical simulations of the gate leakage current in metal-insulator-semiconductor (MIS) structures based on the transfer matrix approach were carried out. They show contribution of different components of this current in MIS structures with best known high-*k* dielectrics such as Ta_2O_5 and TiO_2. The comparison of the gate leakage current in MIS structures with SiO_2 layer as well Ta_2O_5 and TiO_2 layers is presented as well. Additionally, the minimum Si electron affinity to a gate dielectric which allows to preserve given level of the gate leakage current is proposed.

Keywords* — *MIS structures, ultrathin dielectrics, high-k dielectrics.

1. Introduction

High-k dielectrics are attractive for microelectronics as they allow to avoid problems with extremely thin SiO_2 layer as a gate dielectric in MIS structures. Although some of these dielectrics, e.g. Ta_2O_5 and TiO_2, have experienced intensive technological exploration, basic physical constants of these materials have not been completely recognized yet. However, as far as best known high-k dielectrics are considered, its energy gaps manifest apparently smaller values than the SiO_2 band gap [1, 2]. Similarly, Si electron affinity to those dielectrics appears to be significantly smaller than its affinity to SiO_2. Consequently, the significant increase of over barrier current flowing through a such dielectric layer becomes possible. Contrary to that, since high-k dielectric layers can be fabricated as relatively thick layers in comparison with SiO_2 layers, their direct tunneling component is decreased. As a result, the relation between different components of the gate leakage current is changed in comparison to the SiO_2 case which finally may affect the gate voltage dependence of this current as well as breakdown and reliability properties of the gate dielectric.

In this work contribution of different current components to the gate leakage current in best known high-k dielectrics in MIS structures is analysed. Additionally, the minimum Si electron affinity to a gate dielectric which allows to preserve given level of this current is proposed.

2. Gate current components description

Electrostatic properties of a gate dielectric are defined by its electric permittivity ε_x and thickness t_x. In further analysis the same capacitance per unit area of both high-k dielectric and SiO_2 layer is assumed

$$C_x = C_{ox} \,, \tag{1}$$

where $C_x = \varepsilon_x / t_x$ and $C_{ox} = \varepsilon_{ox} / t_{ox}$ (indexes „x" and „ox" refer to a high-k dielectric and SiO_2 layer, respectively). Then

$$t_x = R t_{ox} \,, \tag{2}$$

where $R = \varepsilon_x / \varepsilon_{ox}$ denotes a high-k dielectric electric permittivity normalized to the SiO_2 electric permittivity.

The quality of the dielectric layer as well as the state of its both surfaces are not addressed in this work. Then, the gate leakage current can be considered as a current of carriers tunneling from the semiconductor substrate to the gate or from the gate to the semiconductor substrate. This current depends on the height and shape of the potential barrier that corresponds to the dielectric layer. The height and shape of the barrier depend in turn on dielectric energy gap E_{gx}, the Si-dielectric electron affinity χ_{cx} and the electric field in the dielectric F_x. The energy diagram of the metal-dielectric-semiconductor system is shown in Fig. 1. In further analysis only the electron current flowing from the semiconductor conduction band to the gate is considered. It consists of three components, denoted in Fig. 1: direct tunneling current J_d, Fowler-Nordheim tunneling current J_{FN} and over-barrier current J_{ob}.

To check a contribution of different components of the gate leakage current flowing through best known high-k dielectrics, a numerical simulation of the gate leakage current was carried out. The components of the gate leakage current were calculated with the following formula:

$$J = q \int_{E_0}^{E_1} \left[N_m(E_x) - N_s(E_x) \right] P(E_x) \, dE_x \tag{3}$$

proper when the transverse electron mass change during the electron move from the semiconductor substrate to the gate is neglected. In Eq. (3) E_x is the electron kinetic energy in

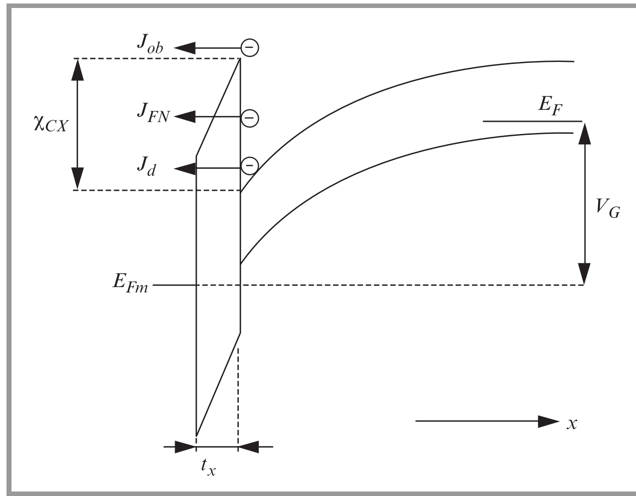

Fig. 1. The energy diagram of the metal-insulator-semiconductor system.

the x direction perpendicular to the semiconductor surface, $P(E_x)$ is the probability of an electron with a given energy E_x transmission from the semiconductor to the gate, and $N_m(E_x) - N_s(E_x)$ is the „supply function" where

$$N_{m,s}(E_x) = \frac{4\pi m^*}{h^3} k_B T \ \ln\left[1 + \exp\left(\frac{E_{Fm,s} - E_x}{K_B T}\right)\right] \quad (4)$$

with E_F as the Fermi potential and indexes m and s refering to the gate and to the semiconductor, respectively [3].

To calculate the probability $P(E_x)$ one needs to know the wavefunction amplitude F_s of an electron which enters the dielectric from the semiconductor-dielectric surface and the wavefunction amplitude F_m of an electron which leaves the dielectric while entering the gate

$$P = \frac{k_m/m_m^*}{k_s/m_s^*} \left|\frac{F_m}{F_s}\right|^2 . \quad (5)$$

Here m_m^* and m_s^* are electron effective masses, and k_m and k_s are electron wavevectors, in the gate and the semiconductor, respectively.

The probability $P(E_x)$ was calculated with the transfer matrix approach. Using this approach, the potential barrier created by a gate dielectric was approximated by the step-like potential barrier. Then, the amplitude of the electron wavefunction F_{i-1} entering the x_i plane between the $(i-1)$-th and i-th potential steps is related to the electron wavefunction F_i leaving this plane by the following relation

$$\begin{bmatrix} F_{i-1} \\ R_{i-1} \end{bmatrix} = \begin{bmatrix} \frac{k_{i-1}+k_i}{2k_{i-1}} \exp[i(-k_{i-1}+k_i)x_i] & \frac{k_{i-1}-k_i}{2k_{i-1}} \exp[i(-k_{i-1}-k_i)x_i] \\ \frac{k_{i-1}-k_i}{2k_{i-1}} \exp[i(k_{i-1}+k_i)x_i] & \frac{k_{i-1}+k_i}{2k_{i-1}} \exp[i(k_{i-1}-k_i)x_i] \end{bmatrix} \begin{bmatrix} F_i \\ R_i \end{bmatrix}, \quad (6)$$

where R_{i-1} and R_i are amplitudes of the electron wavefunctions propagating in opposite direction than the wavefunctions described by F_{i-1} and F_i, k_i is the x-direction component of the electron wavevector in the i-th potential step. The wavevector k_i is calculated using the two band model of the dielectric's potential barrier.

In Eq. (3) the ends of the integration depend on a calculated gate tunnel component. In case of the direct tunneling $E_0 = 0$ and $E_1 = \chi_{cx} - qV_x$, in case of the Fowler-Nordheim tunneling $E_0 = \chi_{cx} - qV_x$ and $E_1 = \chi_{cx}$ and in case of the over barrier component $E_0 = \chi_{cx}$ and $E_1 = \infty$. However, for larger gate voltages, when $qV_x > \chi_{cx}$ there is no direct tunneling component and then $E_0 = 0$ for the Fowler-Nordheim tunneling component.

In simulations the 1 nm equivalent oxide thickness (t_{eq}) of high-k dielectrics was assumed, leading, according to Eq. (2), to

$$t_x = R \ \ [\text{nm}] . \quad (7)$$

The following dielectrics were considered: SiO_2, Ta_2O_5 and TiO_2, with its electric permittivity ε_x, energy gap E_{gx} and electron affinity χ_{cx} according to Table 1. For the TiO_2 layer two cases of different electric permittivity were considered: the thin layer permittivity 30 and thick layer permittivity 80. Since the poor availability of published data of electron effective mass values in high-k dielectrics we assumed their value same as in SiO_2 layer, i.e., half the free electron mass. For comparison we carried out simulations for a larger value of the electron effective mass in a dielectric which led us to the conclusion that larger the electron mass smaller the Fowler-Nordheim current, significantly smaller the direct tunneling current, practically unchanged the over-barrier current and, consequently, smaller the total gate leakage current.

Table 1
Parameters of the considered dielectrics applied in simulations (parameters of high-k dielectrics after [1])

Dielectric	E_{gx} [eV]	χ_{cx} [eV]	ε_x
SiO_2	9	3.15	3.9
Ta_2O_5	4	1.45	25
TiO_2	3.3	1.1	30, 80, (30 ÷ 80)

3. Results

In simulations n^+-polysilicon gate was assumed. Figures 2÷5 show dependence of the gate leakage current and its components on the gate voltage for the all considered gate dielectrics. In case of SiO_2 the direct tunneling component dominates in the total current in a wide range of the gate voltage, up to 3 V. Then, the Fowler-Nordheim tunneling component becomes to dominate and determine the total gate current. In SiO_2 case contribution of the over-barrier current in the total gate leakage current is extremely small due to a high potential barrier (3.15 eV) that electrons encounter at the border between the silicon substrate and the SiO_2 layer. In case of Ta_2O_5 layer the direct tunneling

and Fowler-Nordheim tunneling components dominate in the total current, similarly as in the previous case, but the latter component becomes to dominate for the gate voltage equal to 1.5 V. In case of TiO_2 layers the total gate current is determined by the Fowler-Nordheim component in the whole gate voltage range. Additionally, one can see significant reduction of the direct tunneling component. Here, in spite of the fact that the over-barrier current level remains almost unchanged, one can see significant increase of the over-barrier component contribution to the total gate current in comparison with previous cases. This is due to a low potential barrier (1.1 eV) that electrons encounter at the border between the silicon substrate and the TiO_2 layer.

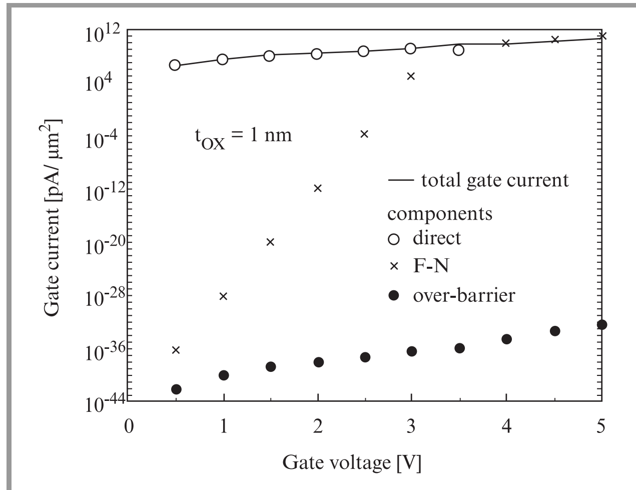

Fig. 2. Dependence of the gate leakage current and its components on the gate voltage in case of MIS structure with SiO_2 as a gate dielectric.

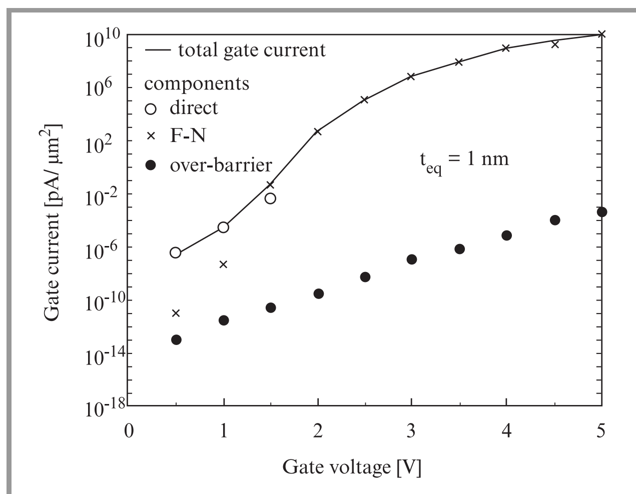

Fig. 3. Dependence of the gate leakage current and its components on the gate voltage in case of MIS structure with Ta_2O_5 as a gate dielectric.

The gate leakage current normalized to the SiO_2 layer current for structures with different dielectrics is shown in Fig. 6. One can see significant dominance of the SiO_2 layer current within the range of small and moderate voltages up to 3 V. The leakage current of the TiO_2 layer with the electric permittivity 30 exceeds the SiO_2 layer current if the gate voltage is increased above 3 V. However, one must remember that in 1 nm thick SiO_2 layer the breakdown will occur for the gate voltage larger than the flat-band voltage by about 1.5 V, which in the case of the assumed n+-polysilicon gate gives the gate voltage approximately equal to 0.5 V.

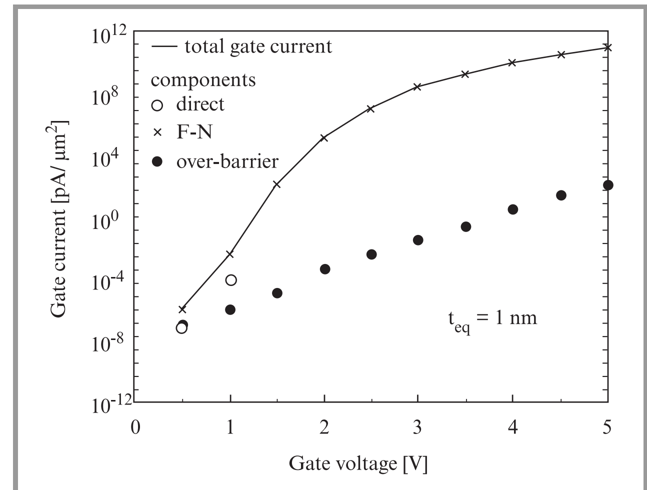

Fig. 4. Dependence of the gate leakage current and its components on the gate voltage in case of MIS structure with TiO_2 with electric permittivity 30 as a gate dielectric.

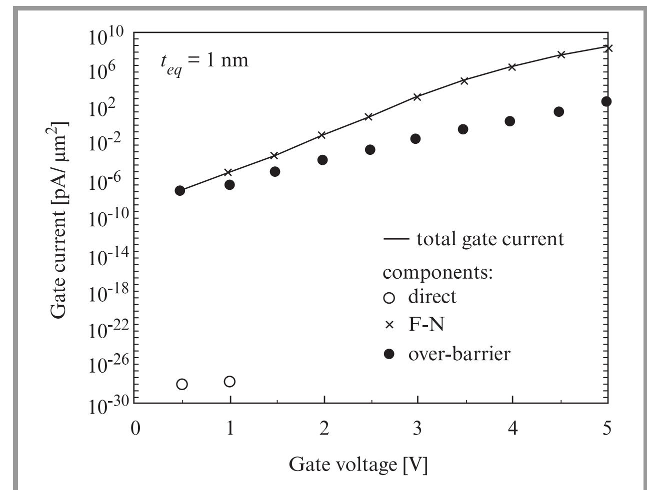

Fig. 5. Dependence of the gate leakage current and its components on the gate voltage in case of MIS structure with TiO_2 with electric permittivity 80 as a gate dielectric.

The minimum Si-dielectric electron affinity which ensures the flow of the same electron leakage current as the current flowing through the SiO_2 layer is shown in Fig. 7. One can see results of a numerical simulation for the 1 V gate voltage (the curve denoted as „total current limit"), tending to be a standard supply voltage in future IC generations.

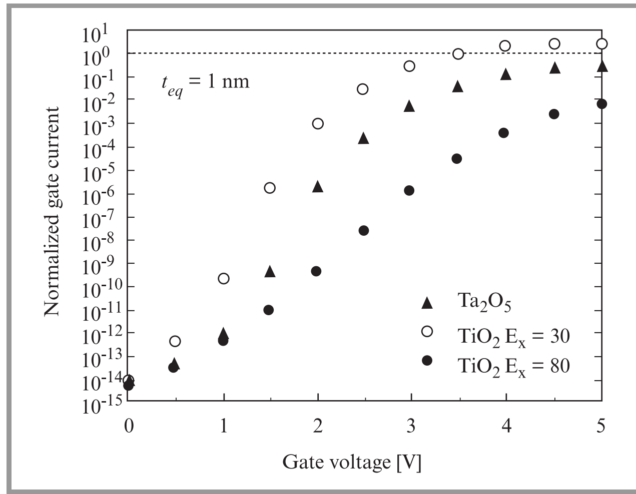

Fig. 6. Gate voltage dependence of the gate leakage current normalized to the SiO_2 layer current for MIS structures with different dielectrics.

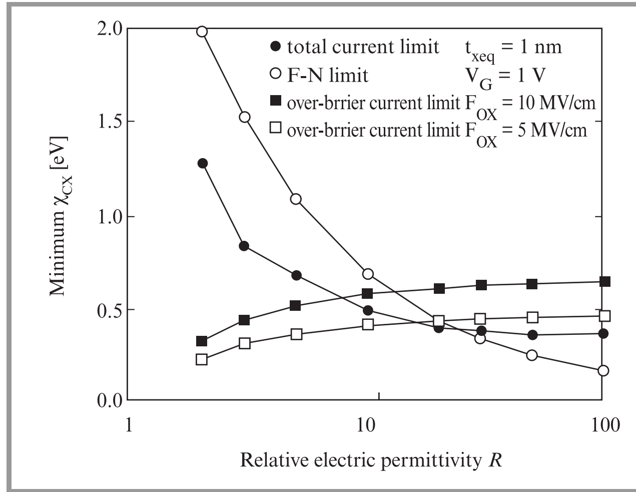

Fig. 7. The minimum Si-dielectric electron affinity that ensures the flow of the same electron leakage current as in the case of SiO_2 layer.

Since, as was shown in the previous figures, in case of TiO_2 layers Fowler-Nordheim current dominates for this voltage, results obtained with analytical approximated condition for the Fowler-Nordheim current level conservation (see Appendix 1) are also presented. For comparison, results of analogous condition for the over-barrier current level conservation (see Appendix 2) are presented in the figure as well. As seen in Fig. 5, this component becomes significant in the case of the TiO_2 layer with electric permittivity 80 for gate voltages smaller than 1 V.

4. Conclusions

The analysis presented in the work shows the contribution of different current components to the gate leakage current in best known high-k dielectrics. In case of Ta_2O_5 layer the structure of this current is similar to the SiO_2 case with the Fowler-Nordheim component dominance for large gate voltages and direct tunneling component dominance for small gate voltages. Contrary to that, in TiO_2 case the direct tunneling component has practically no impact on the total current which is now determined by the Fowler-Nordheim component. Here, the over-barrier current component becomes significant for low gate voltages. Although the total current level is significantly lower than in SiO_2 case, the difference in the structure of this current may result in the breakdown and reliability behavior different than in SiO_2 case.

A minimum value of Si-dielectric electron affinity is limited to 0.4 eV for dielectrics with their electric permittivity as large as tens of SiO_2 electric permittivity. This limit results from the Fowler-Nordheim and over-barrier components of the gate current.

Finally, we wish to underline that there is still a need for more complex exploration of basic physical parameters of high-k dielectrics. There is especially large uncertainty about Si electron affinity to those dielectrics as well as their electron effective masses. In the gate leakage current analyses these parameters are as important as the electron permittivity. Their better knowledge will help to eliminate some materials, or to propose new ones, before spending a lot of money and time on technological experiments.

Appendix 1. Fowler-Nordheim tunneling

Fowler-Nordheim tunneling is given by the following formula

$$J_x = A_x F_x^2 \exp\left(-C_x \frac{\chi_{cx}^{3/2}}{F_x}\right), \qquad (8)$$

where A_x and C_x are constants depending on an electron effective mass in a given insulator and A_x depends additionally on the Si-insulator electron affinity χ_{cx}. If we consider only the exponential factor, the following condition must be fulfilled to preserve the constant value of the F-N current

$$C_x \frac{\chi_{cx}^{3/2}}{F_x} = C_{ox} \frac{\chi_{cox}^{3/2}}{F_{ox}}. \qquad (9)$$

Under assumption that both the gate voltage and the semiconductor voltage drop remain unchanged

$$V_x = F_x t_x = V_{ox} = F_{ox} t_{ox}, \qquad (10)$$

where V_{ox} is the voltage drop on the SiO_2 layer.
Then

$$F_x = \frac{F_{ox}}{R}. \qquad (11)$$

Taking advantage of Eqs. (1), (9) and (11) we get

$$\chi_{cx}^{3/2} = \frac{\chi_{cox}^{3/2}}{R} \qquad (12)$$

and consequently

$$\chi_{cox} - \chi_{cx} \leq \left(1 - R^{-2/3}\right) \chi_{cox}. \qquad (13)$$

Appendix 2. The over-barrier current

The over-barrier current is given by the following formula

$$J_x = A_x T^2 \exp\left(-q\,\frac{\chi_{cx} - \sqrt{\frac{qF_x}{4\pi\varepsilon_x}}}{k_B T}\right), \qquad (14)$$

where T is the absolute temperature, k_B is the Boltzmann constant and A_x is the Richardson constant. Similarly to the F-N case we consider only the exponential factor

$$\chi_{cx} - \sqrt{\frac{qF_x}{4\pi\varepsilon_x}} = \chi_{cox} - \sqrt{\frac{qF_{ox}}{4\pi\varepsilon_{ox}}}. \qquad (15)$$

Then, according to Eqs. (2) and (11)

$$\chi_{cox} - \chi_{cx} = \sqrt{\frac{qF_{ox}}{4\pi\varepsilon_{ox}}} - \sqrt{\frac{qF_{ox}}{4\pi R^2\varepsilon_{ox}}} \qquad (16)$$

and finally

$$\chi_{cox} - \chi_{cx} = \sqrt{\frac{qF_{ox}}{4\pi\varepsilon_{ox}}}\left(1 - \frac{1}{R}\right). \qquad (17)$$

Since ε_{ox} = $3.45 \cdot 10^{-13}$ F/cm:

$$\chi_{cox} - \chi_{cx} \leq 0.2\sqrt{F_{ox}[\mathrm{MV/cm}]}\left(1 - \frac{1}{R}\right) \quad [\mathrm{eV}], \qquad (18)$$

which for $R > 10$ gives

$$\chi_{cox} - \chi_{cx} \leq 0.2\,\sqrt{F_{ox}[\mathrm{MV/cm}]}\,[\mathrm{eV}]. \qquad (19)$$

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Andrzej Jakubowski – for biography, see this issue, p. 33.