Paper

From modelling of a CDMA transceiver in indoor environment to an ASIC circuit synthesis

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Abstract — This paper presents the study, design and simulation of a multi-flow radio frequency transceiver based on a direct sequence spread-spectrum with a 2.4 GHz carrier. First, the functional model of differential QPSK modulation for digital transmission, and the different parts making up spread spectrum function (spreader, despreader, tracking and synchronising devices) have been studied, implemented, simulated and validated in noisy multi-users and multi-path environment by using a unified language. The results obtained by taking into account the home automation running constraints have allowed to determine some critical parameter values and so to integrate the digital functions in an ASIC circuit.

Keywords — indoor radiocommunications, wireless transceiver modelling, CDMA, DS-SS systems.

1. Introduction

The wireless communication needs are increasing for a few years in many application domains as home automation, automobile, aeronautic or telephony. The full expansion of telephony, for example, leads to the emergence of new communication techniques due to the need of higher data rate link. Thus, in 10 years we've passed from GSM-1 G (9.6 kbits) to UMTS-3 G (2 Mbits) [1] entailing a higher system complexity, and so a higher conception difficulty. From that, the telecommunication system conception is the more difficult since many different techniques (RF, numeric, analogic) must coexist in the same chip. Moreover, low cost integration and reduction of the conception time are a priority.

A good way to proceed is to start the conception by studying and analysing the system in its integrity and environment. Such approach allows the designer to choose the system architecture and optimise the parameters with the knowledge of the sub-system interactions (between them or with their environment). If this analysis is done with functional modelling and simulations under an appropriated software environment, it will entail a feedback between the integration stage and the conception as shown in Fig. 1. This top-down approach is retained for the realisation of our system. From the specifications a virtual prototype which allowed us to integrate the system on chip (SoC) has been realised.

The aim of this paper is to expose our solution for the conception of complex system based on a global approach. Here after, a system including its environment is described in a unified language. We will show how the system architecture can be chosen, how some system constraints can be highlighted thanks to such model and how the key parameters can be determined. This analysis allows us to define the optimum architecture for our system considering its physical and technological constraints. Once defined, it can be integrated on an ASIC circuit, performing thus the global conception of the SoC.

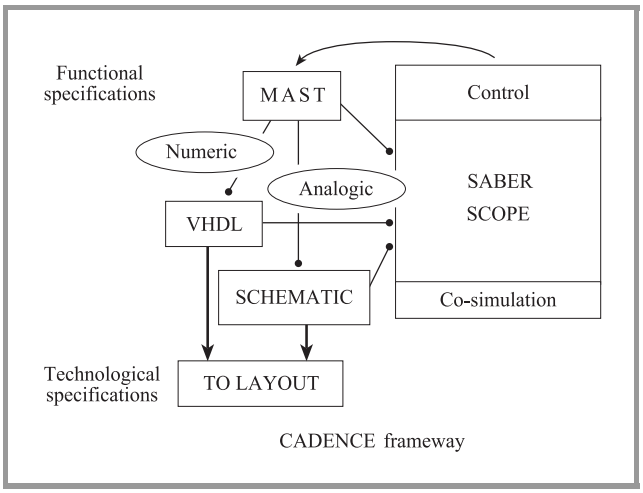

Fig. 1. Top-down conception platform using a unified language.

Based on this approach, the complete design of a 2.4 GHz CDMA transceiver for indoor communications will be presented from the functional simulation (with MAST language under SABER software) to the integration of the baseband processing functions on an ASIC with CADENCE tools. The direct sequence spread spectrum (DS-SS) technique is chosen because of its high indoor constraints immunity (fading, jamming...) [2]. Thanks to our global approach, the conception time is about 6 men/year for the design of the first ASIC.

In the first part, we present the global model of the transceiver. In the second part, we will present some simulation results, which allow us to validate our model, to choose architecture considering the system performances, to optimise some parameters and to highlight some system constraints. At last, a third part will present the integration of the baseband digital processing functions on an ASIC circuit. The conclusion will summarise the important results and the methodology used.

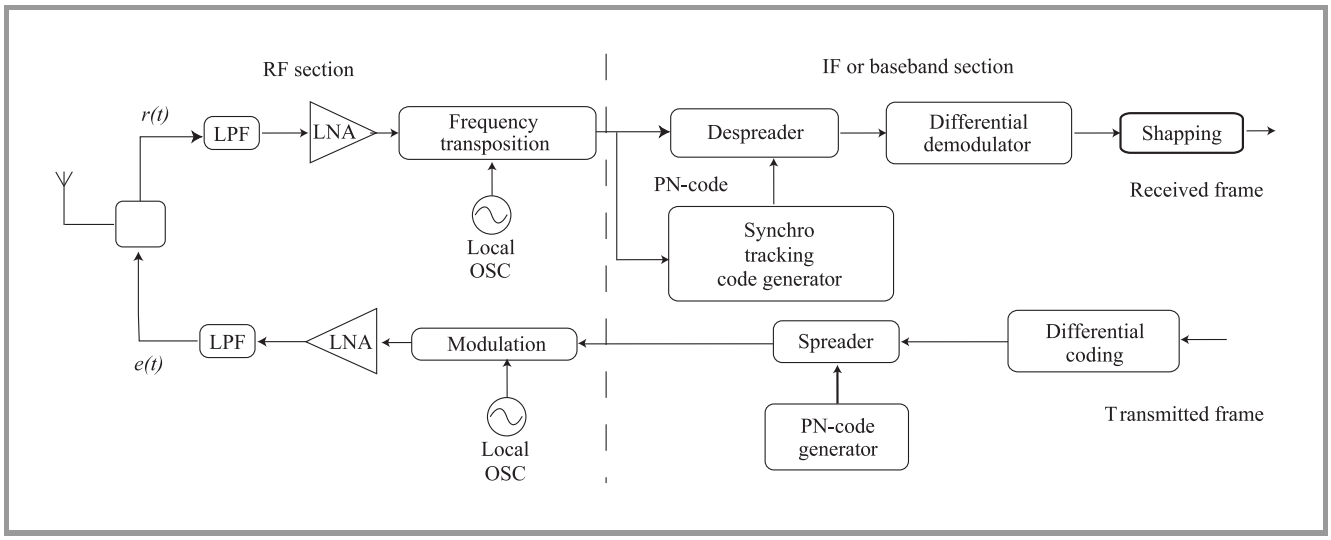

Fig. 2. Global principle scheme.

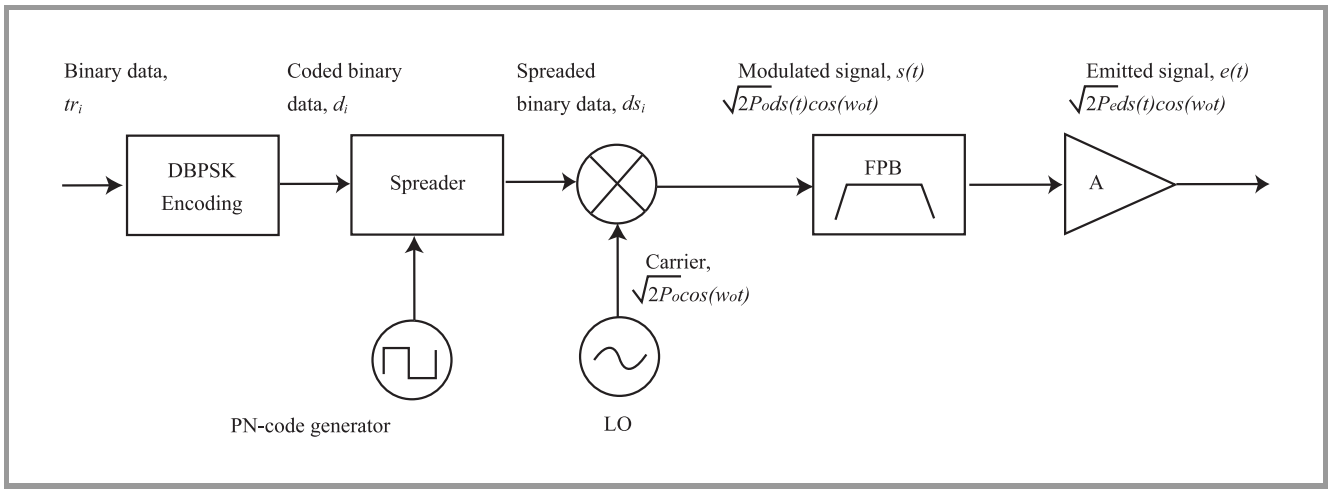

Fig. 3. DBPSK modulator model performed under SABER.

2. Modelisation of the complete transceiver with SABER

2.1. Principle

The system principle is shown in Fig. 2. All functions are described in MAST language which allows to simulate the RF stage and the transmission channels (AWGN, Rayleigh, Multiusers) in a simple way.

Several architectures have been studied and modelled, specially a baseband (BB) and an intermediate frequency (IF) one's. Also different synchronisation architectures (RASE and serial search) have been modelled in order to choose the most appropriated. The signal processing functions of the system can be divided into two groups: direct link and synchronisation. The following notation are used to describe the models: $d(t)$ – the transmitted information; d_i – the expression of the sampled sequence transmitted; $c(t)$ – the PN-code; $ds(t)$ – spread binary data; w_o – the carrier radian frequency; P_r – the power of the received signal; P_e – the power of the emitted signal; P_o – the power of the local oscillator (LO); Td – a time varying delay caused by the channel; T – the symbol time and Tc – the chip time.

2.2. Direct link elements

The modulation technique chosen is the differential phase shift keying (DPSK) for the following reasons [3]:

– an easiest realisation (because this modulation is non-coherent, that is to say there is no carrier tracking);

– the TEB $= 10^{-6}$ when $E_b/N_o = 11$ dB (at the demodulator input); the coherent modulation reaches the same TEB with $E_b/N_o = 12$ dB (see Fig. 8); this performance amelioration is not very significant in regard of the higher system complexity;

– the spectral efficiency can be increased ($\times 2$) just by using a QPSK modulation, which is easy to realise starting from a BPSK modulation [4].

The modulator model realised is presented in Fig. 3. The differential coding equation is [5]: $d_i = tr_i \oplus d_{i-1}$. In DS-SS, the correlation between the transmitted sequence $d(t)$ and the pseudo noise sequence $c(t)$, involving the signal frequency spreading, is assumed by their product $\big(ds(t) = c(t) \cdot d(t)\big)$. It can be digitally realised by an inclusive-AND ($ds_i = d_i \oplus c_i$). The spreading factor (Ns) is therefore the ratio of the code rate with the symbol rate (Tc/T).

A sequential generator generates the PN-code. These sequences are used because of their particular autocorrelation functions: the correlation between two PN-codes is one if they are equal and aligned and is zero elsewhere [6]:

$$Rc(0) = \int_{-\infty}^{+\infty} c(t)c(t)dt = 1\,,$$

$$Rc_i c_j(\tau) = \int_{-\infty}^{+\infty} c_i(t)c_j(t-\tau)dt = 0\,,$$

$$Rc(\tau) = \int_{-\infty}^{+\infty} c(t)c(t-\tau)dt = 0 \quad \text{for} \quad \tau \neq 0\,.$$

Thanks to that property, the correlation between the received signal and the local PN-code allows the system synchronisation and also realises the processing gain (Gp). The processing gain increases the SNR at the input of the demodulator. There are several PN-code families. We chose the M-sequences because they are easily generated with linear feedback shift-registers. Moreover, they are used in many actual norms (especially UMTS) [7]. We have modelled two different types of generator as shown in Fig. 4; g_i represents some switches which are closed or opened according to the primitive polynomial $g(D)$. For example, the polynomial [2, 3] (010011 in octal) is written $g(D) = 1 + D + D^4$, and only the switches g_1 and g_4 are closed (g_0 being always closed).

The Galois generator is potentially faster, but the Fibonacci one's can be initialised with the PN-code loaded serially. This property is used in the RASE synchronisation.

At the receiver, one conception problem is to choose between intermediate frequency or baseband architecture. In a simple way, the BB is interesting because the signal processing is easier to implement (simple digital processing) and also because the signal (and system) bandwidth is two times smaller than IF one's. In the other way, the RF front/end is harder to realise because the frequency transposition goes to zero. This transposition to the baseband leads to conception problems as IIP2, LO leakage, self-mixing, components BF noise [8, 9]. Using IF architecture allows ignoring those problems. The drawback of this technique is the larger bandwidth, which leads to the realisation of chips with bigger size. This is a conception constraint because the power consumption and the price

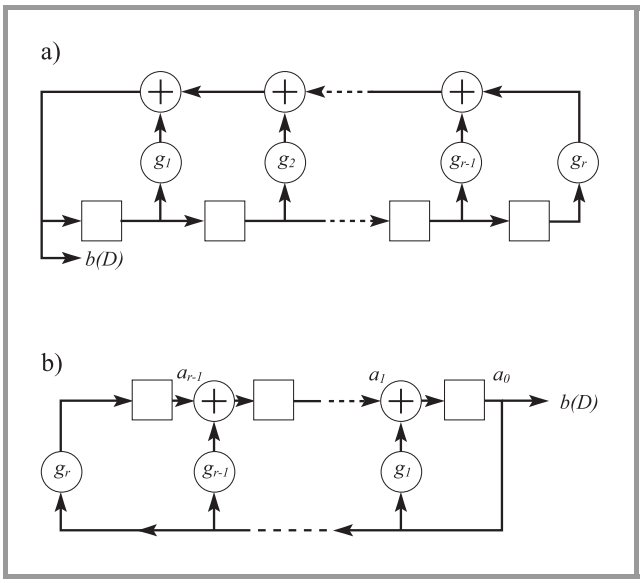

Fig. 4. PN-code generator models: (a) Fibonacci generator; (b) Galois generator.

increase with the chip size. The two types of architectures considered (Fig. 5) have been modelled (for the direct link elements), under SABER, in order to compare their performances. Also, because it uses the receiving signal, the tracking element has been also modelled for a BB and an IF architecture [10].

We can describe the three main elements as followed:

The I/Q demodulator [11] represents the RF front/end. Because the present study is focused on the conception of the signal processing stage, this I/Q demodulator does not take into account all the imperfections of this stage (as non-linearity or BF noise) but allows to consider the carrier impact on the system (filtering, harmonic imbalance...).

The despreader assumes the decorrelation of the PN-code from the received signal. As it despreads the signal, it realises the processing gain (Gp), that is to say the output despreader SNR is the input SNR plus Gp ($S/N_{out} = S/N_{in} + 10 \log Ns$) [12]. In the BB implementation, this function is assumed by a simple logic gate followed by an integrate and dump filter (I&D). The I&D filter sums all the chips in a symbol and dumps the value at the end of the integration. As shown in Fig. 5, for the IF architecture, the integration must be assumed by a filter (because of the carrier) and the product must be done by a multiplier (for which the digital implantation is heavy).

The differential demodulator is assumed by the product of the received symbol with the previous one [13]. Again this function is made by a logic gate and a latch in BB, and by a multiplier in IF.

2.3. Synchronisation elements

The synchronisation principle is shown in Fig. 6a. First, it is necessary to find the PN-code phase (origin) in the re-

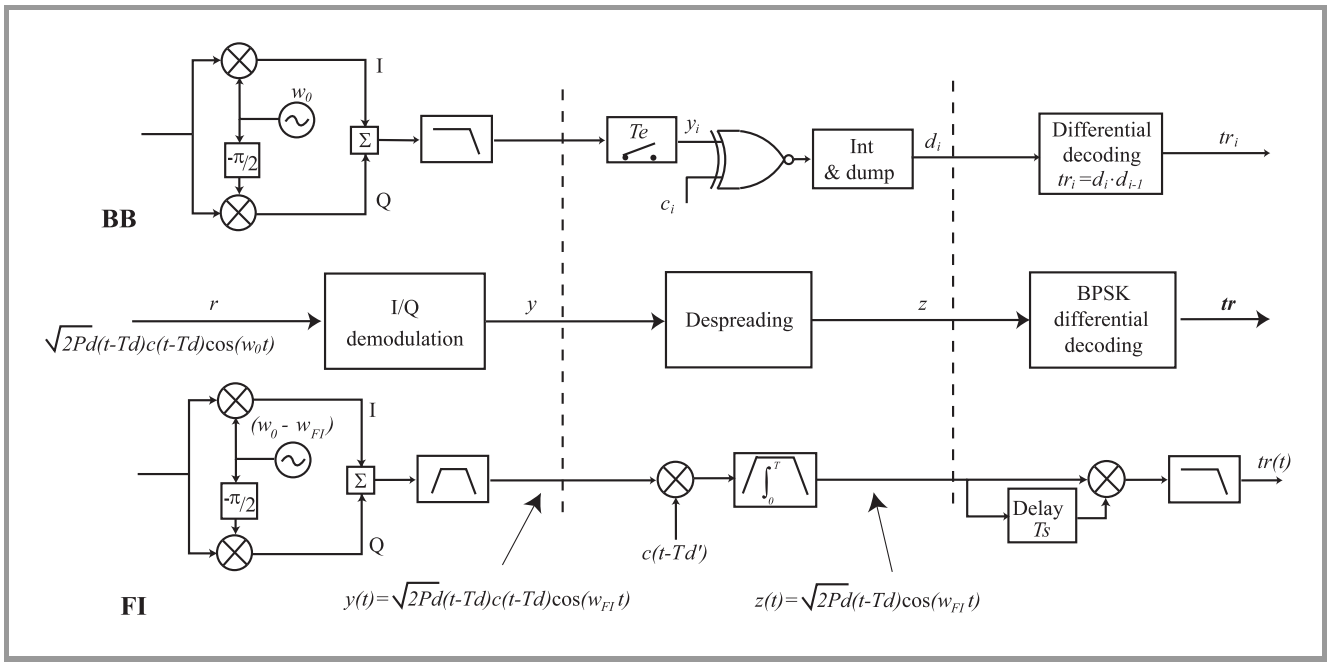

Fig. 5. Principle and models of IF and BB DBPSK receivers.

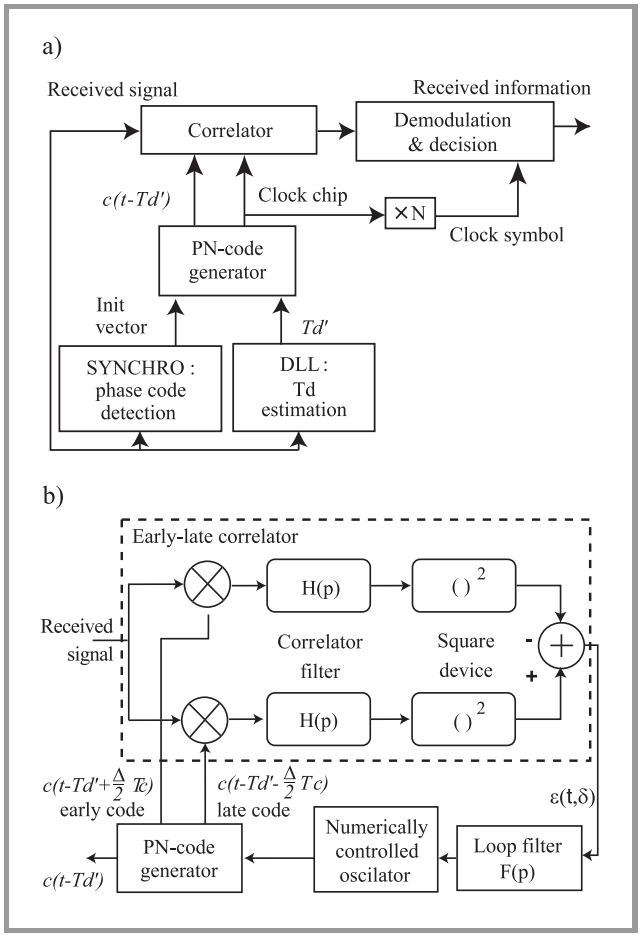

Fig. 6. (a) Synchronisation and acquisition principle; (b) DLL model.

ceived sequence. This function is the acquisition (or initial synchronisation). Next, because the delay in the physical channel is time-variant, it is necessary to evaluate continuously this delay. This function is the tracking.

The tracking is achieved by the DLL [14]. Its model is shown in Fig. 6b. The DLL evaluates the channel delay ($Td(t)$ being the delay in the channel and $Td'(t)$ its estimation) and generates a PN-code slaved by the delay error ($\delta = Td(t) - Td'(t)$). The early-late correlator output signal ε varies with δ thanks to the correlation between the received signal and the PN-code. In the BB architecture, the filter $H(p)$ and the square-low device $()^2$ are replaced by an I&D for the implementation of the early-late correlator [15].

The first acquisition system modelled on SABER is the rapid acquisition based on sequential estimation (RASE) [16], presented in Fig. 7a. Here the local PN-code is built in phase thanks to the estimation of the PN-code received.

Initially, the switch is on position 1. The estimation is achieved by sampling (in BB) or by an I/Q demodulation (in IF). Then, the PN-code estimated is used to load (serially) the $\log_2(N+1)$ shift registers of a Fibonacci generator. This load allows the generation of a PN-code synchronised with the one received. When the shift registers are loaded (after $Tc \log_2(N+1)$ second), the switch is put on position 2 and the generator operates normally.

Then the correlation between the received signal and the local PN-code is estimated. If the correlation occurs, the switch stays on position 2, in the other way round it means that a wrong estimation has been made and the switch is put again on position 1. The interest of this technique is the short acquisition time ($Tc \log_2(N+1)$ in the ideal case), but its drawback is its high noise sensitivity.

The other code acquisition technique implemented with the MAST language is the serial search presented in Fig. 7b.

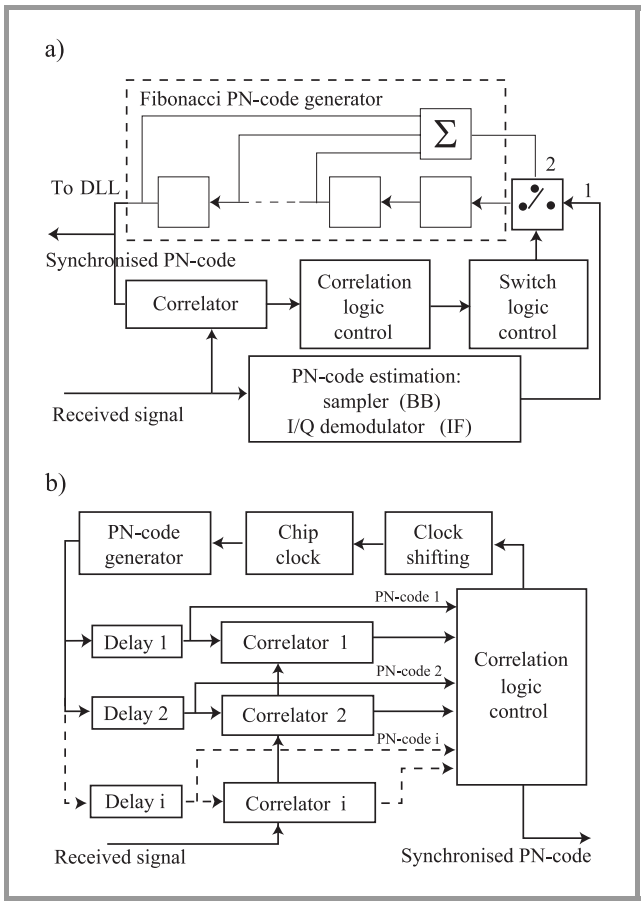

Fig. 7. (a) Rapid acquisition based on sequential estimation model; (b) serial search model.

It was developed by Sage [17]. The principle lies on the estimation of the synchronisation by the correlation of the received signal with the local PN-code. A control device measures the correlation. If the correlation does not occur, the local PN-code is one chip shifted until the correlation occurs [18]. This technique drawback is the maximum acquisition time, which is $N \cdot Tcor$ (where $Tcor$ is the correlation time that is around T) in the noiseless case. This time is reduced by addition of multiple dwells as shown in Fig. 7b. On the other hand, this technique is more immune from noise because it uses the code correlation instead of using the code estimation.

3. Simulations results

3.1. Modulation/demodulation

In Fig. 8a, the different architectures performances in an AWGN channel are plotted. The TEB estimator and the AWGN channel are modelled in MAST language. The despreader is suppressed in order to compare with theory. In Fig. 8a, the model 1 represents the IF architecture, the model 2, the BB one's and the model 3 is the same as model 2 with a matched filter (which is an I&D when the signal is BB) before the demodulator. It appears that model 3 matches with the theory. The divergence observed for the other models is due to the lake of matched-filter, which is necessary to insure the maximum likelihood criterion [DC]. This consideration is important because such filter is quite difficult to make when the signal is IF.

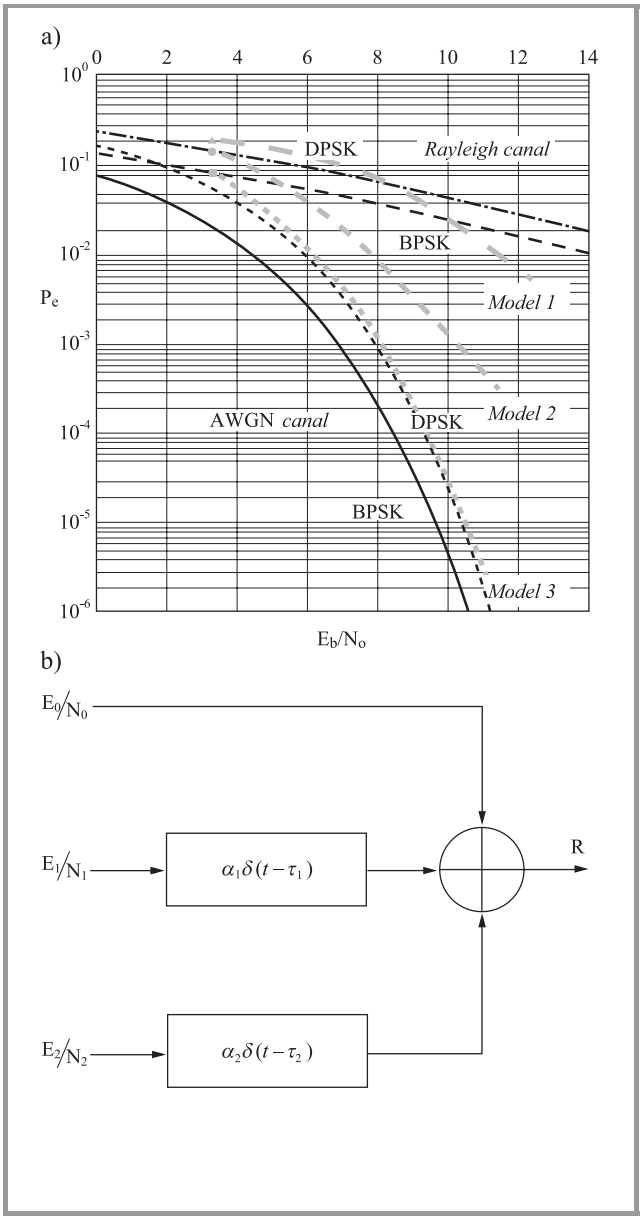

Fig. 8. (a) TEB of the 3 models implanted; (b) multi-path model.

3.2. Despreader

Several studies have been made. First, our virtual prototypes allow us to compare the Gp for the two architectures considered. For a PN-code length equal to 15, the BB processing gain obtained is 12.3 dB (in the ideal case where the sampling is done on an infinite bit number, which is the case the closest to the IF case). For the IF architecture, the processing gain is about 10.8 dB. This highlights the BB for the realisation of this function.

Next, two key parameters associated with the digital implantation are considered [15]. The first one is the sampling frequency, a key parameter when it comes to engineering a good performance-consumption trade-off during reception, and the second one is the number of bits needed at the analog to digital converter during reception that significantly impacts the circuit size. To perform this simulations, we studied the evolution of the signal to noise ratio at the correlator output versus signal to noise ratio at input for different values of sample frequency and number of bits of the analog to digital converter. We also read the process gain value for each simulation. The results are summarised in Table 1.

Table 1
Simulated process gain value for typical sample frequencies and receiver ADC bits number ($N = 15$)

Sampling frequency [MHz]	Process gain [dB]	Number of bits (DAC)	Process gain [dB]
80	8.1	3	11
120	10.54	4	14.3
160	11.2	6	12.8
		8	14.1
		infinite	12.3

A sampling frequency of 80 MHz is markedly inadequate to maintain a significant process gain. Conversely, a frequency higher than or equal to 120 MHz warrants a gain at least equal to 11 dB, close to the maximum theoretical value of 11.8 dB.
The number of bits of the DAC affects the size of the buses in the ASIC circuit and therefore the size and final consumption of the global chip. The study shows that 4 bits is a sufficient value to maintain an amply adequate process gain in the order of 14 dB. Conversely, for a number of bits equal to 3, one notes an important drop of 3 dB on the process gain relative to the maximum theoretical value.

Table 2
Additional SNR due to multi-path

Topology	Characteristics ($Tc = 25$ ns)	S/N out
One user: $E_0 = E_1 = E_2 = U$	$N_0 = N_1 = N_2 = 15$, $\tau_1 = 12.5$ ns, $\tau_2 = 40$ ns, $\alpha_1 = \alpha_2 = 1.1$	+13.5 dB
Two user: $E_0 = E_1 = U_1$, $E_2 = U_2$ (R is on U_1)	$N_0 = N_1 = 256$, $N_2 = 15$, $\tau_1 = 10$ ns, $\tau_2 = 40$ ns, $\alpha_1 = 0.75$, $\alpha_2 = 1$	+48 dB
Two user: $E_0 = E_1 = U_1$, $E_2 = U_2$ (R is on U_1)	$N_0 = N_1 = 15$, $N_2 = 256$, $\tau_1 = \tau_2 = 40$ ns, $\alpha_1 = 0.75$, $\alpha_2 = 1$	+8.5 dB

At last, we have studied the multi-path channel impact on the correlation thanks to the model shown in Fig. 8b which allows simulating real topologies.

The perturbations due to the different paths are measured in term of additional SNR (at the output despreader) comparatively to the case of a single path. The results are summarised in Table 2.
More than the trivial observation which is to say: long codes prevent from multi-path, this simulation shows that the paths arriving during the time chip ($\tau < Tc$) increase the SNR. In other terms, to take advantage of time diversity and DS-SS, the signal bandwidth must be around the coherence bandwidth. In the other way, especially if $1/Tc$ is bigger than the coherence bandwidth (which is around 10 MHz in our indoor application), a RAKE receiver is needed to use time diversity and so prevent from multi-path fading.

3.3. DLL

The DLL performance analysis is done thanks to tracking jitters variance σ_s [18]. The Fig. 9a shows a comparison between the theoretical and measured variance of the BB and IF model. First, it validates our MAST model, since the measure is close to the theory. Next, it shows that the BB is more immune to the white Gaussian noise thanks to its correlation filter. Indeed, thanks to our virtual prototype, we highlight the fact that the early-late correlator filter bandwidth can be set to $1/T$ in the BB case whereas it must be around $1/Tc$ in the IF architecture. In IF, a smaller bandwidth results in a loss of energy that degrades the DLL performance.
The Fig. 9b compares a DLL architecture where the tracking is done on a entire chip ($\Delta = 1$) with one where the tracking is done on a half chip ($\Delta = 0.5$). Here, the simulation result is quite interesting because the measure gives the $\Delta = 0.5$ architecture to be the best when the theory gives the $\Delta = 1$ architecture. However, the $\Delta = 0.5$ architecture is said to be better in practice [20], and this contradiction is explained by the divergence of the theoretical model when $\Delta \neq 1$. This shows how such virtual prototyping is helpful in system conception, especially to choose architecture.

3.4. RASE vs serial

Because the simulation of the code acquisition mean time is too long, (there are too many random parameters), we have studied the noise limit for which this time increases exponentially. The results presented in Fig. 10 compare the RASE and the serial search techniques for a BB signal. It appears that the serial search (even if it is slower than RASE) is more immune to the noise since its limit is around -8 dB against -4 dB for the RASE.

3.5. Simulation summary

This unified description with the MAST language was helpful for the conception and the design of our system. The previous study highlights the BB architectures for their simplicity and most of the time for their better performances (despreader, demodulator, DLL). For the synchronisation

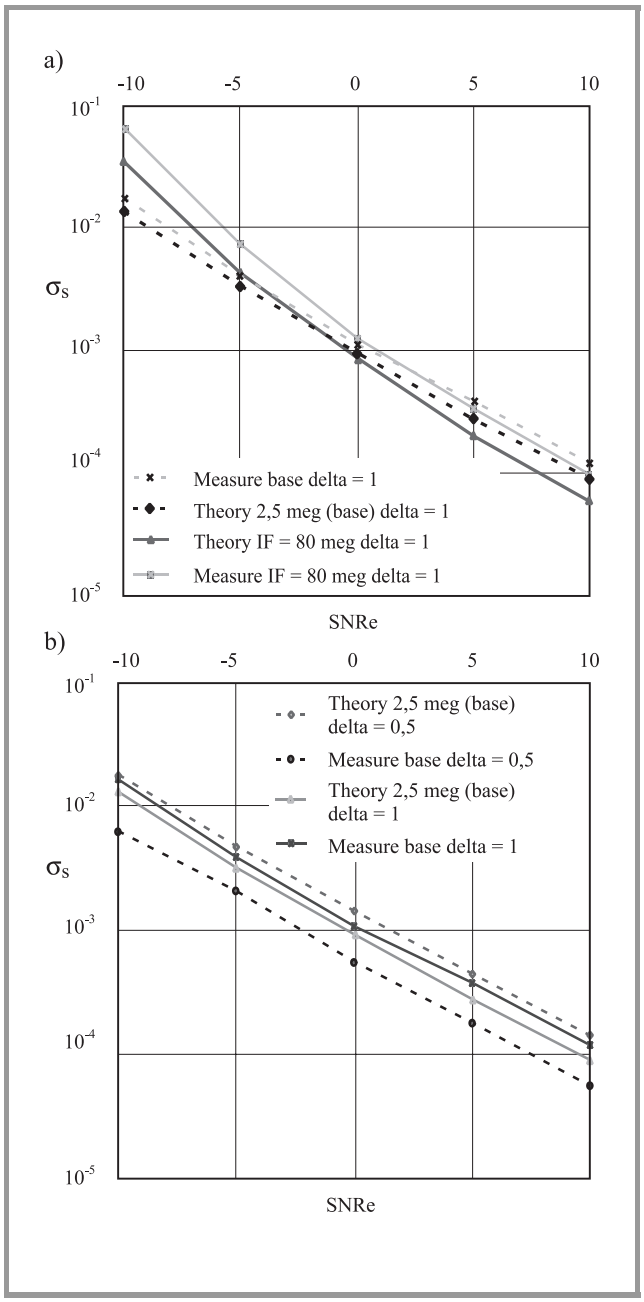

Fig. 9. DLL performance analysis: (a) δ_S for BB and IF architecture; (b) δ_S for different Δ architecture.

sub-system, the $\Delta = 0.5$ DLL and the serial search are retained according to there performances in noisy environment. In term of system constraints, our virtual prototype shows that a double integrator is needed in serial search. Moreover, the multi-path analysis shows that the system bandwidth must be < 10 MHz to take advantage of time diversity. At least a matched-filter is needed in receiver. In the BB architecture, the matched filtering is assumed by the correlator I&D filter placed just before the demodulator. In terms of parameters, the simulation shows that the BB DLL correlator integration time can be set to *Tc*. Also, for a digital implementation, the simulation shows that a frequency sampling of 160 MHz and a 4 bits DAC is needed to achieve the processing gain.

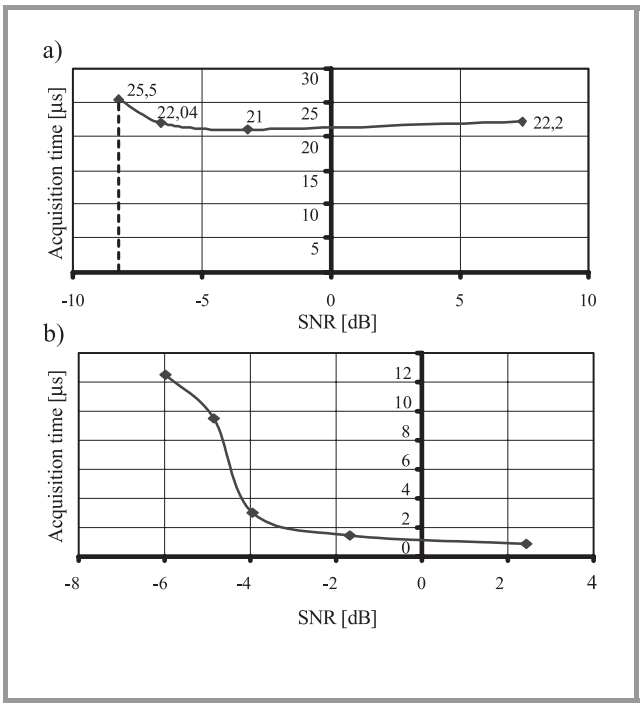

Fig. 10. (a) Serial search; (b) RASE.

4. ASIC conception

Since the architecture and the key parameters are defined and studied in the previous part, the integration of the digital signal processing functions on an ASIC circuit is now presented. First, the methodology and the baseband digital stage are presented. Next, some simulation results derived from the VHDL encoding of the main digital functions and the corresponding circuits are presented using CADENCE software. These simulations will allow us to quantify the performances reached (in terms of costs, consumption and surface area) of the ASIC circuit as a function of the technologies put forward (CMOS and BiCMOS).

According to the global functional system presented in Fig. 2, we present in the Table 3 the different numerical stages that we decided to implement on the ASIC for the complete transceiver. As seen in the Table 3, a particularity of our circuit is the possibility of transmitting and receiving at different rates from 19 kbps ($N = 2047$) to 5.71 Mbps ($N = 7$). So, a low rate corresponds to a high process gain, and therefore the channel noise perturbation can be reduced. Likewise, a higher rate induces a low process gain and the demodulation is more difficult to achieve.

4.1. Methodology

Our aim is to produce a low consumption and a low cost circuit. One of the original features of our study lies in the

Table 3
Numerical functions implanted in ASIC circuit

Transmitter		Receiver	
Differential encoder	yes	Differential decoder	yes
PN code generator	yes	PN code generator	yes
Multi-rate command ($N = 7$ to 2047)	yes	Multi-rate command ($N = 7$ to 2047)	yes
Spreading correlator	yes	Despreading correlator (integrate & dump)	yes
Nyquist filter	no	Nyquist filter	no
		DLL	no
		Serial search	no

development of a source code using a VHDL portable onto different technologies.

After validation of our system, we now investigate the implementation of main transmitter and receiver digital functions. To perform the simplest ASIC tests, we integrated a state machine type module in order to synchronise and adequately track the received signal.

The available technologies in our laboratory are A.M.S. type (Austrian Mikro Systeme), as indicated in Table 4. Under CADENCE environment, functional simulations are carried out with Affirma and placement-routing with silicon ensemble. Under SYNOPSYS, we perform the synthesis with design analyser. The overall design chart given in Fig. 11 describes the top-down approach starting from the VHDL specification.

Table 4
Available technologies (X)

AMS technologies	0.8 μm	0.6 μm	0.35 μm
CMOS	X	X	X
BiCMOS	X	–	–

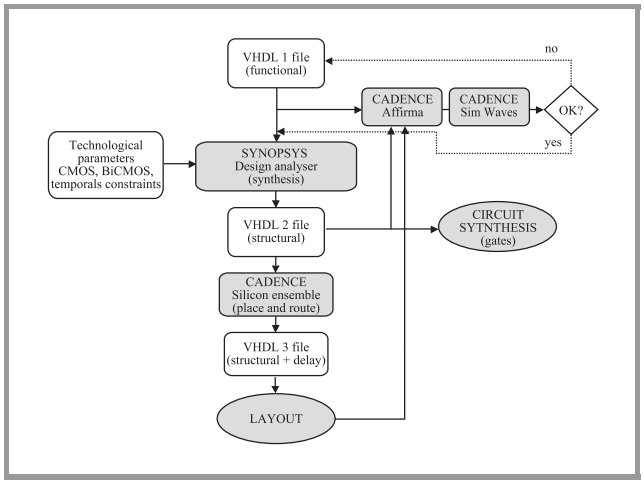

Fig. 11. Top-down ASIC circuit design under CADENCE and SYNOPSYS.

4.2. Transmitting and receiving circuits synthesis

Figure 12 shows the synthesised functions of the global transceiver, including the main digital functions as indicated in Table 1.

Concerning the transmitter, a Galois type PN code generator adjustable in length by means of a 4 bits word ($N_{\max} = 2047$) has been implemented. In the same way, a drive module allowing to generate the clock frequencies corresponding to the different possible data rates (19 kbps to 5.71 Mbps) and to synchronise the digital frame to be transmitted with the local PN code, has been implemented.

For the receiver, we chose an 8 bits word size for the analog-to-digital converter output in order to facilitate the first functional tests of the ASIC. Then, before the final production of the complete ASIC (including the synchronisation and tracking units of the PN code received), we will synthesise a 4 bits architecture (generic VHDL code).

First, we synthesised the transceiver using various technologies (see Table 5) and compared the area, power consumption and production cost of the ASIC using the AMS technology available in the lab.

The CMOS 0.8 μm technology is the least expensive. Nonetheless, for an equal cost, the 0.6 μm technology occupies twice as less surface and causes a 30 percent drop of the power consumption. With regard to the currently embedded functions, and in spite of a very important area and power consumption fall, a 0.35 μm technology seems too onerous for our application.

Finally, we choose a 0.6 μm CMOS technology, which is a good trade-off in terms of cost and performances. We can notice that interconnections use 60% of the total area of the transmitter chip. The circuit is actually in course of realisation and the first tests will be performed in few months.

5. Conclusion

Using a unified specification approach, we realised a virtual prototype of a complete DS-SS DBPSK transceiver under SABER software (using the MAST language). This stage conception allowed us to specify the optimum architecture taking into account the environment and the subsystems interactions. Baseband architecture is chosen in regard of its performances. Also a $\Delta = 0.5$ DLL and the serial search is chosen for the realisation of the synchronisation elements. Moreover, the functional models allow us to determine important parameters as the DLL correlator integration time ($1/T$ in BB and $1/Tc$ in IF) or the system bandwidth (< 10 MHz). Also, the impact of three key parameters related to the digital stages, i.e., sampling frequency ($f = 160$ MHz) and converter bus size (4 bits), is analysed.

Portable VHDL encoding the basic digital functions enabled us to quantify the system performances under CADENCE and SYNOPSYS software. Simulation results shown that interconnections and drive circuits oc-

Table 5
Sensitivity to various AMS technologies ($V_{DD} = 4.5$ V; $T = 350$ K)

Technologies	Area [mm^2]	Power consumption [mW]	Price/mm^2 [euro]	Total price [euro]	Minimal area [mm^2]
0.8 μm CMOS	2.16	55	220	475	4
0.8 μm BiCMOS	2.7	68	440	1188	3
0.6 μm CMOS	0.97	42	300	291	4
0.35 μm CMOS	0.32	4	490	156.8	12

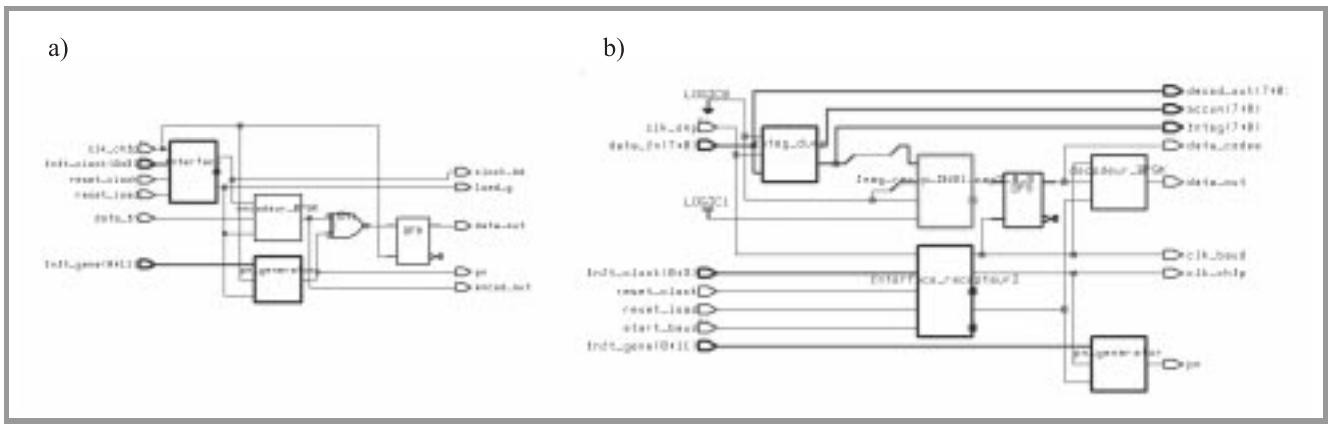

Fig. 12. Synthesised transmitter (a) and receiver (b) under design analyser.

cupy a substantial area compared to elementary functions. Finally, we have investigated the impact of CMOS and BiCMOS technologies and found a good trade-off in terms of cost and performance with a 0.6 μm CMOS technology.

All digital functions have not been embedded yet. The DLL and the Nyquist filter are being developed and precedent results could be perceptibly affected.

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