Paper

Novel Method of Improving Electrical Properties of Thin PECVD Oxide Films by Fluorination of Silicon Surface Region by RIE in RF CF_4 Plasma

Małgorzata Kalisz, Grzegorz Głuszko, and Romuald B. Beck

Abstract—This study describes a novel technique to form good quality low temperature oxide ($< 350^\circ$C). Low temperature oxide was formed by N_2O + SiH_4:N_2 plasma in a plasma enhanced chemical vapour deposition (PECVD) system on the silicon surface reactively etched in CF_4 plasma (RIE – reactive ion etching). The fabricated oxide demonstrated excellent (for low temperature dielectric formation process) current-voltage (I–V) characteristics, such as: low leakage current, high breakdown voltage and good reliability. Experimental results indicate that the proposed method of fluorine incorporation into the SiO_2/Si inteface improves electrical parameters of MOS structures.

Keywords—capacitance-voltage characteristics, current-voltage characteristics, fluorine plasma, radio frequency reactive ion etching.

1. Introduction

As semiconductor devices are scaled down to obtain higher-performance ultra-large-scale integration (ULSI) devices, the realibility of gate-oxide films is one of the most important issues. The downscaling of gate oxide thickness improves current driving capability and reduces short-chanel effects. However, ultrathin oxide films exhibit many serious reliability problems, such as, time-dependent dielectric beakdown, interface-state generation and charge trapping (e.g., [1]). Fluorination of the gate oxide structures has been investigated as a possible candidate for solution of these problems [2]–[8]. Many aspects of the properties of fluorinated oxides have already been studied. Such oxides have been found, for example, to be more resistant to ionizing radiation [2], Fowel-Nordheim (F-N) tunneling injection stress [1]–[3] and channel hot electron stress [4]. Dramatic reduction of both hole-trapping probability and interface-trap generation under avalanche hole injection conditions of the fluorinated samples has also been reported [6]. In [7] it has been found that the degree of improvement is a function of fluorine concentration, which has created a pressure to obtain high concentrations of fluorine in silicon oxide.

A number of methods of fluorinated gate oxide fabrication has been proposed, e.g., by immersing Si wafer in HF solution with D.I. water rinse prior to oxidation [8], by ion implantation of fluorine atoms into poly-Si gate followed by a high temperature drive-in [2], or by rapid thermal processing in O_2 with diluted NF_3 [7].

An attractive method to fabricate high quality thin fluorinated gate oxides is conventional plasma enhanced chemical vapour deposition (PECVD) oxide on silicon substrate pretreated with CF_4 plasma without subsequent annealing [8]. As it has already been established in [8] application of CF_4 plasma pretreatment to the silicon surface before the PECVD gate oxide formation improved largely almost all electrical parameters, e.g., the Q_{bd} distribution, the V_{th} value.

In our recent study, it has been reported that reactive ion etching (RIE) in CF_4 plasma is a good method to incorporate high concentrations of fluorine ions into silicon surface, thus it may be considered as yet another serious candidate for fluorination process [9].

This study, in turn, investigates the structural and electrical characteristics of metal-oxide-semiconductor (MOS) structures with thin fluorinated gate oxide prepared by means of silicon dioxide RIE in CF_4 plasma prior to the deposition of gate oxide.

2. Experiments

In this work, two types of gate oxide fabrication methods were compared and investigated: PECVD deposited oxide (control – sample 4 in Table 1) and oxide deposited in a conventional PECVD tool on a surface etched in CF_4 plasma (samples 1, 2, and 3 in Table 1).

The p-type, boron-doped (100)-oriented silicon wafers with resistivity of 4–10 Ωcm were cleaned using standard procedures (SC1+SC2+HF).

Both, PECVD and RIE processes were performed in conventional RF Oxford PlasmaLab Systems. First, 13 nm thick initial PECVD oxide was deposited by at 300°C for 30 s with RF power of 10 W. The SiO_2 film was then reactively etched for 2 min in a RIE tool at room temperature by CF_4 flowing at the rate of 50 ml/min. In the experiments the RF power was set to: 80 W, 120 W and 160 W.

The complete set of experiments performed in this study is shown in Table 1.

For all samples except of the control one, fluorine distribution profiles and their concentration in the dielectric

Table 1
Matrix of experiment and process parameters

Type of sample	PECVD initial oxide reactive ion etching in RF CF_4 plasma				Final SiO_2 deposition using PECVD				
	flow of CF_4 [ml/min]	pressure [mTr]	time [min]	RF power [W]	temperature [°C]	RF power [W]	pressure [mTr]	gas flow rates [ml/min]	time [s]
1	50	200	2	80	350	10	600	$N_2O = 120$ SiH_4:$N_2 = 70$	30
2	50	200	2	120					
3	50	200	2	160					
4	–	–	–	–					

layer have been measured by ultra low energy-secondary ion mass spectroscopy (ULE-SIMS).

In order to use electrical characterization methods, MOS test structures were fabricated with the layers under investigation as gate dielectrics. Aluminium was used as gate metal and bottom electrode, allowing reliable electrical measurements.

3. Results and Discussion

3.1. SIMS Characterization of Fluorine Content

It has already been established in [9] that reactive ion etching in fluorine plasma is a good method of fabricating layers containing fluorine atoms in the silicon substrate surface region. These layers are thin (about 1.5 nm) and the concentration of fluorine incorporated into them is very high, with the maximum values exceeding 10^{19} cm^{-3}. What is important – the fluorine incorporation in the substrate may be controlled by RIE parameters, e.g., RF power or reactive gas pressure.

As it has been shown in [10], the PECVD gate oxide deposition (at 300°C) following RIE does not change the position of this profile but affects the maximum of fluorine concentration only. As a result of the deposition of silicon dioxide on the etched surface, the maximum of fluorine concentration decreases for all characterized samples fabricated within this study to about 10^{18} cm^{-3}. This suggests that due to the elevated temperature of deposition (300°C) some of the fluorine atoms can escape from the fluorinated film. Interestingly, the fluorine concentration is still significantly higher (by several orders of magnitude) than that obtained with other methods. In this way a structure consisting of silicon dioxide/oxide fluorine rich thin film/silicon (Fig. 1) is formed.

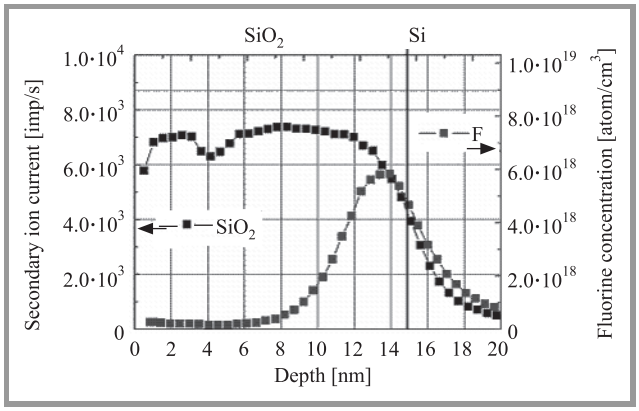

Fig. 1. SIMS profiles for structure consisting of silicon dioxide/thin fluorine-rich/silicon obtained as a result of initial oxide etching by RIE in CF_4 followed by PECVD oxide formation.

It should be stressed that although the fluorine concentration decreases after the final silicon oxide layer depositon, the RIE process still makes it possible to control (to a certain extent) the position of the fluorine profile and the value of its maximum concentration (Fig. 2). For electrical characterization discussed below we used the sample with the highest fluorine concentration at the dielectric/silicon interface of a MOS structure fabricated with RF power equal to 160 W (sample 3).

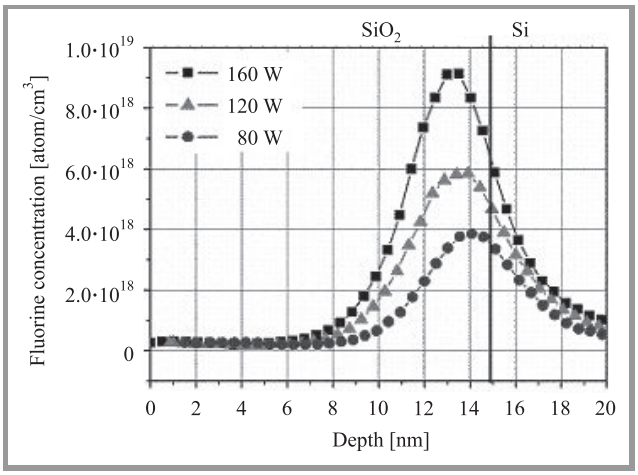

Fig. 2. Fluorine distribution profile in samples fluorinated in RIE with different RF plasma power prior to PECVD oxide deposition.

3.2. Electrical Characterization

The effect of fluorine incorporation into the gate oxide was clearly noticeable in the electrical characteristics: capacitance-voltage (*C–V*) and current-voltage (*I–V*) of MOS test capacitors.

3.2.1. Analysis of *C–V* Characteristics

As expected, the control samples with PECVD gate oxide only are characterized by very high shift of *C–V* curves towards negative voltages. *C–V* characteristics of these samples exhibit also a strong frequency dependence in the strong inversion region – see Fig. 3(a).

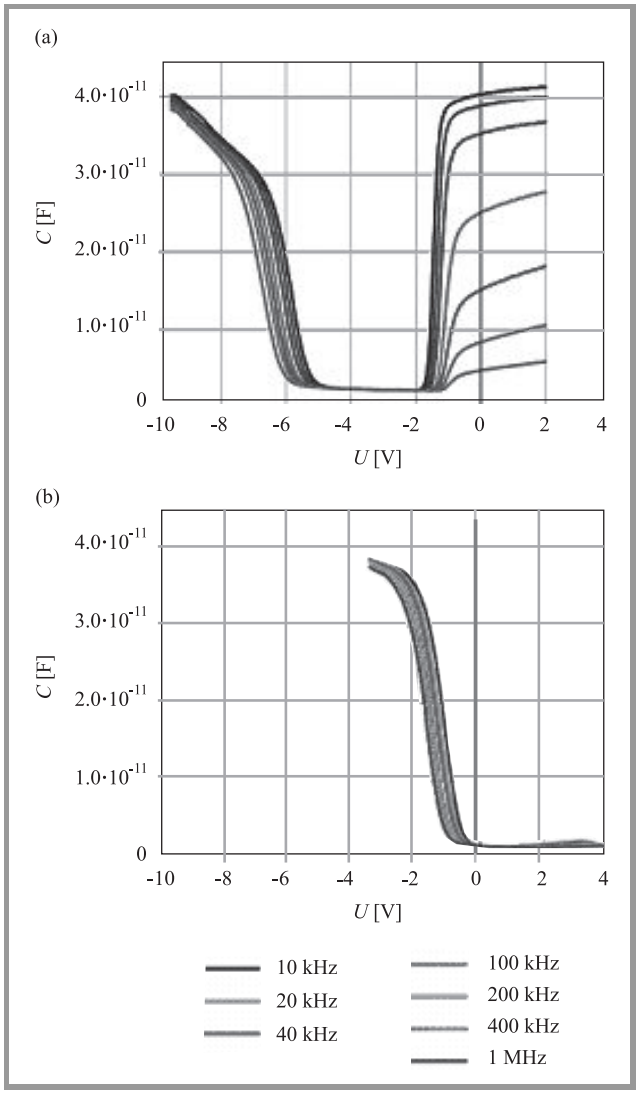

Fig. 3. The $C-V$ characteristics for MOS test structures with gate oxide prepared in different ways: (a) control sample (PECVD only) and (b) fluorinated by RIE process (RF power 160 W) + PECVD oxide.

The incorporation of fluorine by means of RIE reduces the voltage shift significantly (compare Fig. 3(a) with Fig. 3(b)). Another effect of fluorine incorporation into the interface of a MOS structure is the disappearance of frequency dispersion in *C–V* curves – see Fig. 3(b).

In Table 2 electro-physical parameters evaluated from *C–V* characteristics of the MOS test devices formed during experiment are presented.

It can be seen there, that all the measured samples have negative flat band voltage (V_{fb}) values. For the control oxide sample, the negative (V_{fb}) is very high. The possible reason is that after RIE in CF_4 plasma, we can expect poorer quality of the substrate surface due to the damage of the initial oxide layer. The very low temperature of the gate dielectric PECVD deposition (300°C) does not allow for significant improvement of the oxide quality due to thermally related effects – the temperature is simply too low. Consequently, for these samples, we can expect high effective densities of the total non-compensated charge in the oxide-silicon system (Q_{eff}) and interface traps density (e.g., D_{itmb}).

Table 2
Electrical parameters evaluated from *C–V* characteristics of the fabricated test structures

Method of fluorination	Control	RIE
C–V curves analysis at $\varepsilon = 3.9$		
N_A [cm^{-3}]	$1.7 \cdot 10^{15}$	$0.43 \cdot 10^{15}$
V_{fb} [V]	−4.15	−1.42
V_{mb} [V]	−3.4	−0.95
D_{itmb} [1/eV cm^2]	$10.3 \cdot 10^{11}$	$5.7 \cdot 10^{11}$
Q_{eff}/q [cm^{-2}]	$35.8 \cdot 10^{11}$	$7.7 \cdot 10^{11}$

In the studied samples substrate fluorination has improved the properties of both, the oxide/silicon interface and the oxide bulk (see Table 2), showing that curing mechanisms resulting form the presence of fluorine prevailed over the effects resulting from the damage created during the fluorination (RIE).

During fluorination, high energy fluorine ions break O-Si-O bonds and form two types of dangling bonds: Si and Si-O. In the mean time, fluorine ions react with dangling Si bonds and Si-O bonds and form SiF and SiOF films, which passivate the modifited surface.

The same type of dependence on fluorine concentration is observed for Q_{eff}.

As it has already been established in [10], for the sample prepared by means of RIE, the maximum of fluorine concentration is located in the oxide. Fluorine ions located in the silicon dioxide layer not only passivate SiO_2/Si interface but also react with the structural defects and damages of silicon dioxide. Therefore, the value of Q_{eff} is lower for the sample with fluorine incorporated into the interface of MOS structure than for the control sample.

3.2.2. Analysis of *I–V* Characteristics

As it can be seen from Fig. 4 fluorinated PECVD gate oxide exhibits much better properties than the control one. The very bad breakdown statistics indicate that the uniformity of the PECVD oxide is poor. On the other hand, relatively low leakage currents (until breakdown) prove, that the control PECVD oxide does not contain many structural defects that would contribute to the leakage currents.

The observed changes can be considered in terms of breakdown statistics and leakage current.

For RIE fluorination, we have observed very significant rise in the mean breakdown voltage value and very good

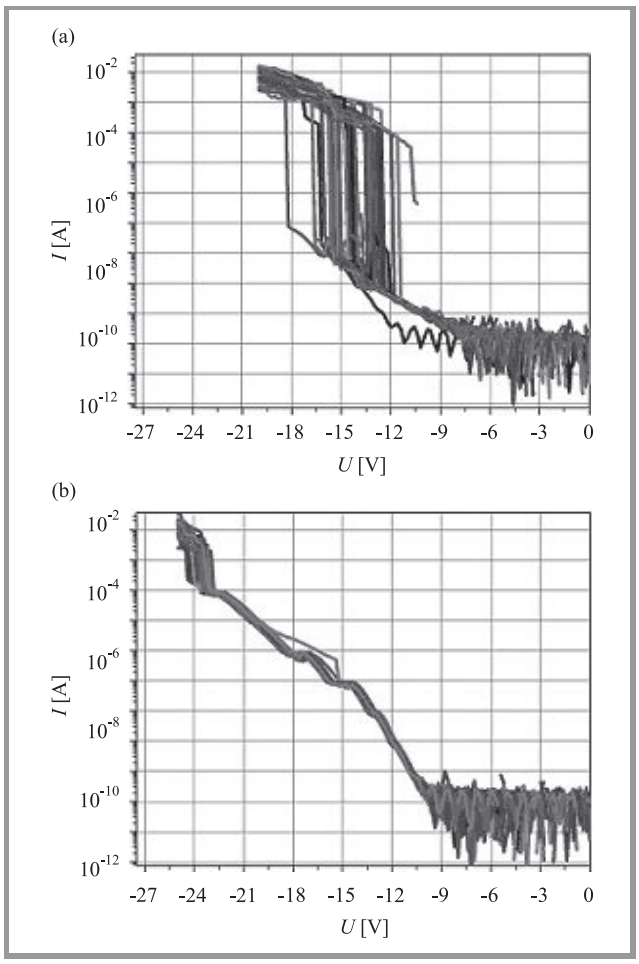

Fig. 4. The $I-V$ characteristics measured on MOS test structures with gate oxide prepared in different ways: (a) control sample (PECVD only) and (b) fluorinated by RIE process (RF power 160 W) + PECVD oxide.

statistics of breakdowns, while the leakage currents were still comparable with those of the control samples. All these parameters are very important for the feasibility of manufacturing real devices, as the requirements resulting from international technology for semiconductors (ITRS) have been challenging in this area for many years already.

4. Conclusions

The results obtained in this study show that the examined method of fluorination (RIE in CF_4 plasma of initial oxide) allows achieving very high concentrations of fluorine at the silicon surface region (of the order of $10^{19} - 10^{20}$ cm^{-3}) and the following gate oxide deposition by means of PECVD at 300°C does not reduce this concentration by more than one order of magnitude.
It is also clear from the presented results, that the presence of fluorine in such quantities at the oxide-silicon interface results in significant improvement of the electrical properties of otherwise poor-quality PECVD oxide.

The obvious results of silicon surface fluorination by means of RIE in CF_4 plasma prior to gate oxide deposition by PECVD are:

- significant reduction of both, Q_{eff} and D_{itmb};
- removal of the frequency dispersion in the inversion region of $C-V$ curves;
- increased breakdown voltage;
- significantly improved breakdown statistics.

References

[1] Y. Mitani, H. Satake, Y. Nakasaki, and A. Toriumi, "Improvement of charge-to-breakdown distribution by fluorine incorporation into thin gate oxides", *IEEE Trans. Electron Dev.*, vol. 50, no. 11, pp. 2221–2226, 2003.

[2] Y. Nishioka, K. Ohyu, Y. Ohji, N. Natuaki, K. Mukai, and T. P. Ma, "Hot-electron hardened Si-gate MOSFET utilizing F implantation", *IEEE Electron Device Lett.*, vol. 10, no. 4, pp. 141–143, 1989.

[3] P. Wrigh, N. Kasai, S. Inoue, and K. C. Saraswat, "Hot electron immunity of SiO_2 dielectrics with fluorine incorporation", *IEEE Electron Dev. Lett.*, vol. 10, no. 8, pp. 347–348, 1989.

[4] X. W. Wang, A. Balasinski, T. P. Ma, and Y. Nishioka, "Pre-oxidation fluorine implantation in Si process-related MOS characteristics", *J. Electrochem. Soc.*, vol. 139, no. 1, pp. 238–241, 1992.

[5] H. H. Tseng, P. J. Topin, F. K. Baker, J. R. Pfiester, K. Evans, and P. L. Fejes, "The effect of silicon gate microstructure and gate oxide process on threshold voltage instabilities in P+ gate chanel MOSFET's with fluorine incorporation", *IEEE Trans. Electron Dev.*, vol. 39, no. 7, pp. 1687–1693, 1992.

[6] E. F. da Silva Jr., Y. Nishioka, and T. P. Ma, "Radiation response of MOS capacitors containing fluorinated oxide", *IEEE Trans. Electron Dev.*, vol. 34, no. 6, pp. 1190–1195, 1987.

[7] J. Ahn, G. Q. Lo, W. Ting, D. L. Kwong, J. Kuehne, and C. W. Magee, "Radiation hardered metal-oxide-semiconductor devices with gate dielectrics grown by rapid thermal processing in O_2 with diluted NF_3", *Appl. Phys. Lett.*, vol. 58, no. 4, pp. 425–427, 1991.

[8] J-W. Lee, Y. Li, and S. M. Sze, "Highly reliable low temperature ultrathin oxides grown using N_2O plasma", *WSEAS Trans. Electron.*, vol. 1, no. 1, pp. 72–76, 2004.

[9] M. Kalisz, R. B. Beck, and M. Ćwil, "Reactive ion etching process (RIE) in CF_4 plasma as a method of fluorine implantation", *Vaccum*, vol. 82, no. 10, pp. 1046–1050, 2008.

[10] S. K. Lai and D. R. Young, "Effects of avalanche injection of electrons into silicon-dioxide – generation of fast and slow interface states", *J. Appl. Phys.*, vol. 52, no. 10, pp. 6231–6240, 1981.

Małgorzata Kalisz was born in Żarów, Poland, in 1977. She received the M.Sc. degree in electronics and optoelectronics material science in 2003 from the Department of Fundamental Problems of Technology, Wrocław University of Technology, Poland. She received the Ph.D. degree in microelectronics in 2009 from the Faculty of Elec-

tronics and Information Technology, Warsaw University of Technology. Since 2003, she has been with the Motor Transport Institute (ITS), Warsaw. Her research interests include the role of fluorine-containing ultrathin layer, formed on the surface during silicon and silicon dioxide reactive ion etching on the depth of boron thermal diffusion into silicon and electrical parameters of MOS structures.

e-mail: mkalisz1@mion.elka.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland

e-mail: malgorzata.kalisz@its.waw.pl
Motor Transport Institute
Jagiellońska st 80
03-301 Warsaw, Poland

Grzegorz Głuszko was born in Biłgoraj, Poland, in 1976. He received the B.Sc. and M.Sc. degrees in microelectronics from Warsaw University of Technology in 2002 and 2004, respectively. Since then he has been working on a Ph.D. thesis concerning characterization of novel MOS devices. His research interests include charge pumping studies of the quality of silicon-silicon dioxide interface, as well as modeling of MOS devices.

e-mail: ggluszko@poczta.onet.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa 75
00-662 Warsaw, Poland

Romuald B. Beck received the M.Sc. degree in electronics from the Faculty of Electronics, Warsaw University of Technology, Poland, in 1976. From the same university, he received the Ph.D. and D.Sc. degrees in 1982 and 1996, respectively. Since 2000 he has taken the post of a Professor. Since 2005 he has been heading Microelectronic and Nanoelectronic Devices Division. His research activities have been concentrated in the area of modeling, diagnostics and technology of the metal-insulator-semiconductor devices, especially – with very thin and ultrathin oxides. In particular he is concerned with theoretical and experimental studies on different dielectric layers formation methods (including methods involving d.c. and a.c. plasmas), their kinetics and the relations between the process kinetics and the electrophysical properties of the devices, their yield and their reliability. The area of his research interest covers also dry etching methods and their implementation to modern ICs technology. In case of plasma processing he has been actively engaged in the research work on negative consequences of the use of plasma (radiation damage and contamination) and experiments aiming at curing the structural and electrophysical damage related to plasma ambient and e-beam bombardment. His research interest covers also design of novel test structure design and new diagnostics methods.

e-mail: r.beck@elka.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa 75
00-662 Warsaw, Poland