Paper

The Effect of High Temperature Annealing on Fluorine Distribution Profile and Electro-Physical Properties of Thin Gate Oxide Fluorinated by Silicon Dioxide RIE in CF_4 Plasma

Małgorzata Kalisz, Grzegorz Głuszko, and Romuald B. Beck

Abstract—This study describes the effects of high temperature annealing performed on structures fluorinated during initial silicon dioxide reactive ion etching (RIE) process in CF_4 plasma prior to the plasma enhanced chemical vapour deposition (PECVD) of the final oxide. The obtained results show that fluorine incorporated at the PECVD oxide/Si interface during RIE is very stable even at high temperatures. Application of fluorination and high temperature annealing during oxide layer fabrication significantly improved the properties of the interface (D_{itmb} decreased), as well as those of the bulk of the oxide layer (Q_{eff} decreased). The integrity of the oxide (higher V_{bd}) and its uniformity (V_{bd} distribution) are also improved.

Keywords—capacitance-voltage characteristics, current-voltage characteristics, fluorine plasma, high temperature annealing process, radio frequency reactive ion etching.

1. Introduction

A key issue of ultra-large-scale-intergation technology (ULSI) is the quality of thin silicon dioxide layer used in the devices. Today, oxide thickness less than 80 Å and oxidation temperatures at about 800–900°C are required as the semiconductor industry pushes toward 1 Gbit memory chips and beyond. However, good electrical properties generally require high temperature conditions either during oxidation or as postoxidation annealing (POA) [1]. At low temperatures, ultrathin SiO_2 films prepared by the conventional plasma enhanced vapour deposition (PEVD) process do not represent satisfactory properties, e.g., they are characterized by high leakage currents and high fixed charge density. It has been demonstrated, e.g., in [1]–[6] that incorporation of small amounts of fluorine into SiO_2 can be an efficient way to improve the electrical parameters of SiO_2/Si interface.

Several ways of fluorine introduction into gate oxide, including among others: in-situ NF_3 oxidation [4] and ion implantation [5], have been tried so far.

Another useful technique to improve the quality of low temperatrure SiO_2 is high thermal annealing process.

It, thus, seems tempting to apply both of these techniques in order to get the best results possible. The problem with such an approach is that high temperature annealing of fluorinated oxides fabricated by means of the above mentioned processes seriously affects the F concentration in the oxides – as fluorine atoms escape from fluorinated gate oxides during high temperature annealing [7].

In our previous work, it has been reported that fluorination by means of reactive ion etching (RIE) in CF_4 plasma is an efficient method of manufacturing quite good quality oxides [8].

In this work, we study the effects of high temperature annealing on structures fluorinated during initial silicon dioxide reactive ion etching in CF_4 plasma prior to the plasma enhanced chemical vapour deposition (PECVD) of the final oxide.

2. Experiments

The p-type, boron-doped (100)-oriented silicon wafers with the resistivity of 4–10 Ωcm were cleaned using standard procedures prior to oxidation.

The PECVD and RIE processes were performed in conventional RF Oxford PlasmaLab systems.

The 13 nm thick initial oxide was deposited by means of PECVD at 300°C for 30 s with RF power equal to 10 W. The obtained SiO_2 film was then reactively etched for 2 min in a RIE tool at room temperature in CF_4 (50 ml/min) plasma generated with 160 W RF signal. Afterwards, the final oxide layer was deposited during PECVD at 300°C. Then, in split experiment, some of the samples were annealed in Ar at 1100°C for 30 min. The complete matrix of experiments is shown in Table 1.

For all samples, except of the control one, the fluorine distribution profiles and their concentration in the dielectric layer have been measured by ultra low energy-secondary ion mass spectroscopy (ULE-SIMS).

In order to use electrical characterization methods for evaluation of electro-physical properties, metal-oxide-semiconductor (MOS) test structures were fabricated with

Table 1
Parameters of all processes used during experiments

Type of sample	Reactive ion etching (RIE) in RF CF_4 plasma				Final SiO_2 deposition in PECVD					Thermal annealing	
	flow of CF_4 [ml/min]	pressure [mTr]	time [min]	RF power [W]	temperature [°C]	RF power [W]	pressure [mTr]	gas flow [ml/min]	time [s]	temperature [°C]	time [min]
1	50	200	2	160	300	10	600	$N_2O = 120$ $SiH_4 = 70$	30	–	–
2	50	200	2	160						1100	30
3	–	–	–	–						–	–
4	–	–	–	–						1100	30

the layers under investigation as gate dielectrics. For the purposes of comparison, the reference samples, without fluorination of the SiO_2/Si interface, were also made.

3. Results and Discussion

3.1. SIMS Characterization of Fluorine Content

It has already been established before (e.g., in [9]) that reactive ion etching in fluorine plasma can be effectively used for fabricating layers containing high concentrations of fluorine atoms. Direct application of high temperature to such a layer causes fluorine atoms to escape from the fluorinated film. Thin film of silicon oxide deposited at low temperature (300°C) on top of the fluorine-rich layer prevents them from escaping from the fluorinated layer during the subsequent high temperature annealing process.

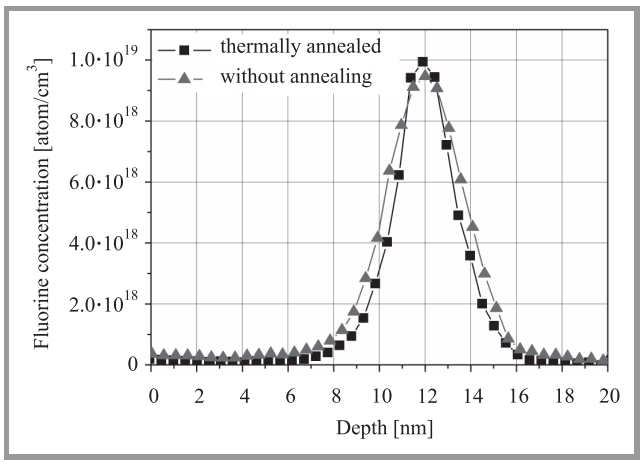

Fig. 1. The comparison of fluorine distribution profiles before and after high temperature annealing.

As presented in Fig. 1, the high temperature annealing performed in Ar at 1100°C, for 30 min had almost no effect on fluorine profile in the studied structures. The only change observed is marginal sharpening of the fluorine profile. This indicates that fluorine remains stable during high temperature annealing at its original location at the PECVD SiO_2/Si interface.

3.2. Electrical Characterization

The effect of fluorine incorporation into deposited silicon dioxide and of high temperature annealing was easily noticeable on both types of the electrical characteristics studied, i.e., capacitance-voltage ($C-V$) and current-voltage ($I-V$) characteristics of test metal-oxide-semiconductor capacitors.

3.2.1. Analysis of *C–V* Characteristics

As expected, the very high temperature annealing causes improvement of the *C–V* curves in both of the studied cases (Fig. 2). This improvement seems to be more spectacular for non-fluorinated sample in which apart from the decrease of the voltage shift (expressed, e.g., in terms $V_{fb} = 0$) also the frequency dispersion in the inversion region has been significantly reduced.

One may, however, notice also some consequences of high temperature annealing on the fluorinated samples.

The beneficial effects of high temperature annealing for attaining more robust oxides have been attributed to its possible ability to remove defects and damages existing in the bulk of the PECVD silicon dioxide layer. Application of high temperature annealing causes a reduction of both, D_{itmb} and Q_{eff} (see Table 2 and Fig. 3).

Similarly to the results presented in [8], within the course of this work it has been established that the fluorine atoms incorporated into the interface of SiO_2/Si improve the electrical parameters of silicon dioxide layer. However, the result of the high temperature annealing is still clearly noticeable on the measured $C-V$ curves as well as in the values of the evaluated electrical parameters, i.e., D_{itmb} and Q_{eff}. This means that the latter process is still capable of removing some defects existing in the bulk of PECVD silicon dioxide layer.

It has to be realized, however, that the degree of improvement due to high temperature annealing is by far smaller than that due to fluorination of the silicon substrate surface.

It is also worth mentioning that the degree of Q_{eff} changes is much higher than that of D_{itmb}, which means that fluorine presence in the structure is especially beneficial for curing

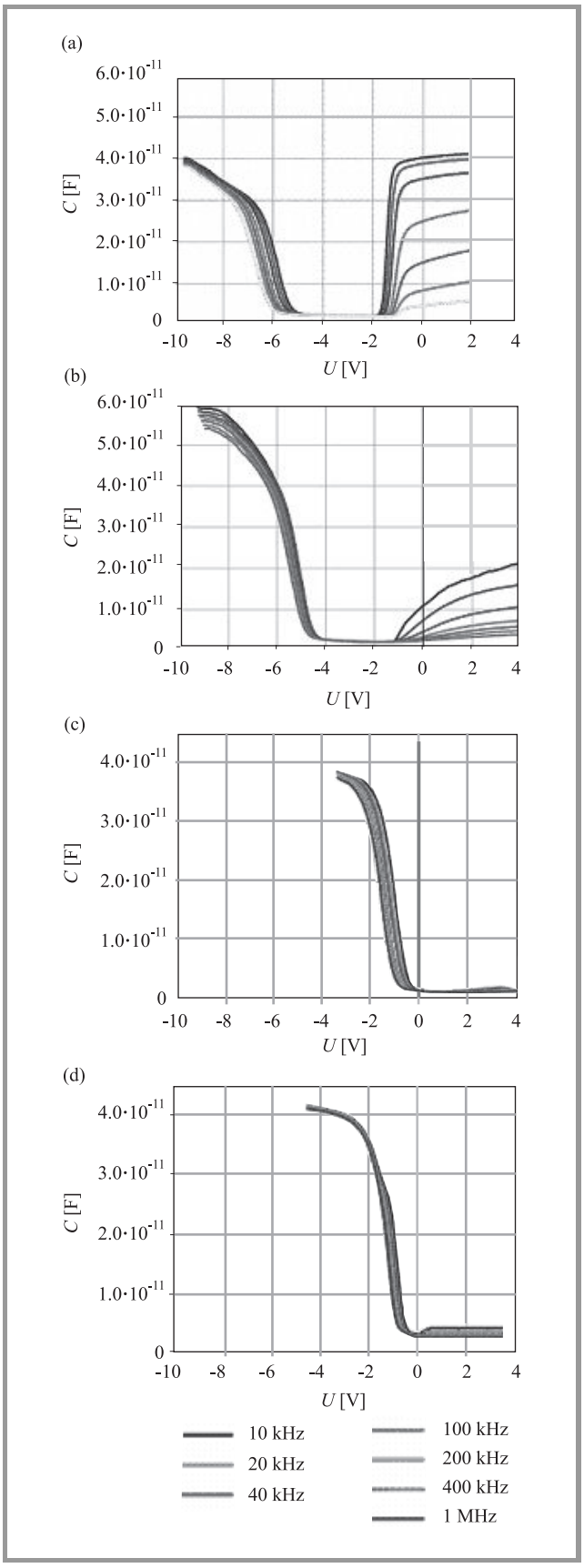

Fig. 2. The $C-V$ characteristics of samples fabricated in different ways: (a) control sample, (b) control sample annealed, (c) RIE fluorinated but not annealed, and (d) RIE fluorinated and annealed.

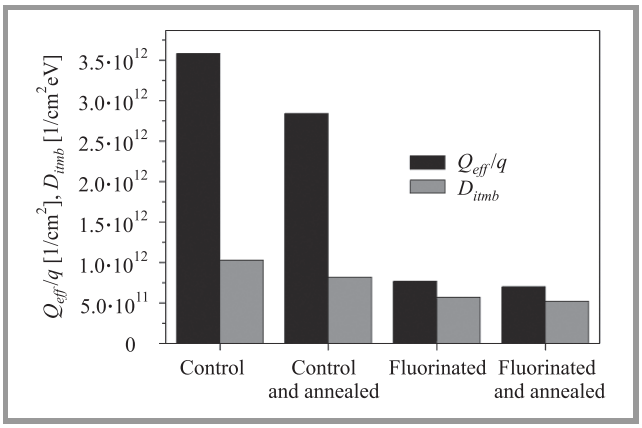

Fig. 3. Dependence of Q_{eff} and D_{itmb} on the method of fabrication the MOS test structure.

Table 2
Values of the most important electrical parameters of MOS structures evaluated from C–V characteristics of samples fabricated using different methods

Sample type	Control	Control annealed	RIE fluorinated	RIE fluorinated annealed
C–V curves analysis at $\varepsilon_{ox} = 3.9$				
N_A [cm^{-3}]	$1.73 \cdot 10^{15}$	$1.17 \cdot 10^{15}$	$0.43 \cdot 10^{15}$	$1.4 \cdot 10^{15}$
V_{fb} [V]	−4.15	−3.28	−1.42	−1.30
V_{mb} [V]	−3.4	−2.7	−0.95	−0.86
Q_{eff}/q [cm^{-2}]	$35.8 \cdot 10^{11}$	$28.4 \cdot 10^{11}$	$7.7 \cdot 10^{11}$	$7.0 \cdot 10^{11}$
D_{itmb} [1/eV cm^2]	$10.3 \cdot 10^{11}$	$8.17 \cdot 10^{11}$	$5.7 \cdot 10^{11}$	$5.18 \cdot 10^{11}$

the defects within the volume of the gate oxide, while high temperature annealing seems to be similarly effective in both areas (interface and volume of the oxide).

3.2.2. Analysis of *I–V* Characteristics

As shown in Fig. 4, application of high temperature annealing in control samples improves a little the statistics of breakdown events at the expense of higher leakage current, while having almost no effect on V_{bd} values.

Introduction of fluorine to the PECVD oxide improves both, V_{bd} values and their distribution. When high temperature annealing is additionally performed on fluorinated structures, we obtain even more narrow V_{bd} distribution, as well as higher V_{bd} values. Practically, no changes in the leakage currents values are observed.

Hence, also from the perspective of the electro-physical properties that are manifested on I–V characteristics, simultaneous application of both, fluorination and high temperature annealing is advantageous in comparison to the application of any of these methods individually.

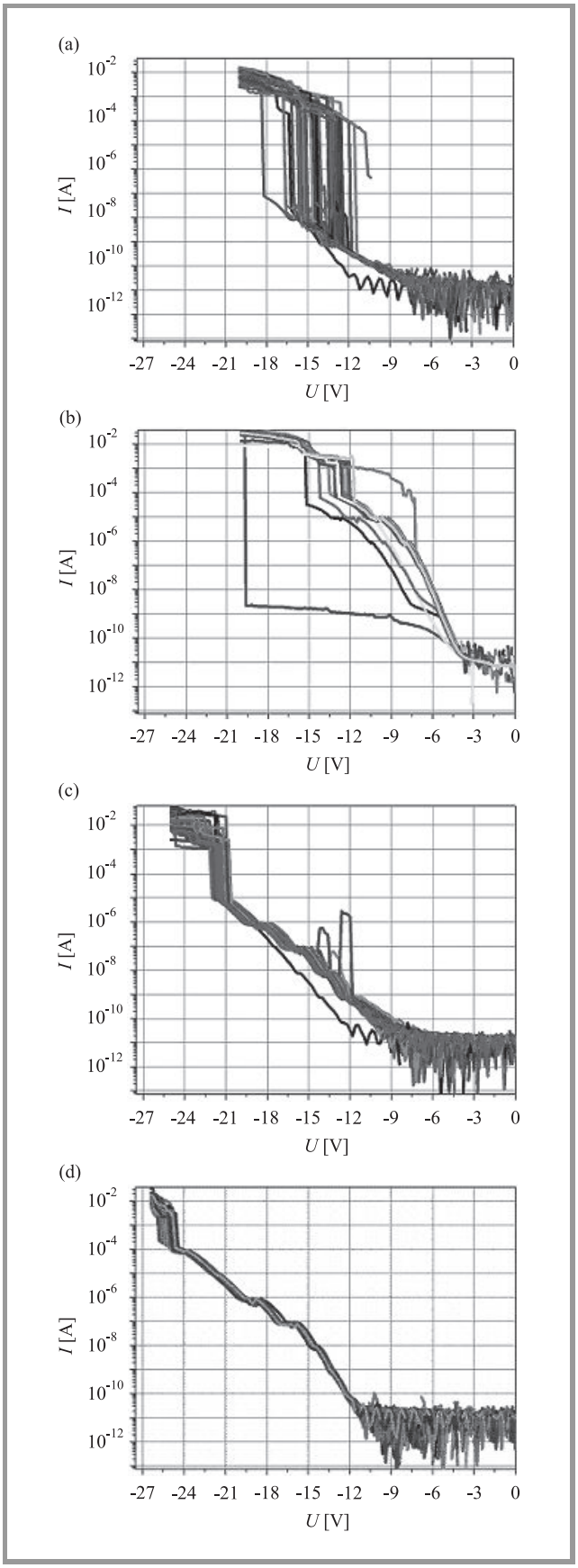

Fig. 4. The *I–V* characteristics of samples fabricated in different ways: (a) control sample, (b) control sample annealed, (c) RIE fluorinated but not annealed, and (d) RIE fluorinated and annealed.

4. Conclusions

The results obtained during this study show that fluorine incorporated at the PECVD oxide/Si interface by means of RIE is very stable even at high temperatures.
This effect allows combining the fluorination and high temperature annealing in order to improve the electro-physical properties of the low temperature oxide (e.g., PECVD oxide). We have also demonstrated that there are several advantages of the application of such combination. The properties of the SiO_2/Si interface (D_{itmb} decreased) and the bulk of the oxide layer (Q_{eff} decreased) are significantly improved. The integrity of the oxide (higher V_{bd}) and its uniformity (V_{bd} distribution) are also improved.

The improvement of the electro-physical properties of the SiO_2-Si systems obtained due to application of both studied steps (fluorination and high temperature annealing) is in all studied cases better than using one of these steps only.

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Grzegorz Głuszko and **Romuald B. Beck** – for biographies, see this issue, p. 24.