Paper

Large-Signal RF Modeling with the EKV3 MOSFET Model

Maria-Anna Chalkiadaki and Matthias Bucher

Abstract—This paper presents a validation of the EKV3 MOSFET model under load-pull conditions with high input power at 5.8 GHz, as well as S-parameter measurements with low input power up to 20 GHz. The EKV3 model is able to represent coherently the large- and small-signal RF characteristics in advanced 90 nm CMOS technology. Multifinger devices with nominal drawn gate length of 70 nm are used.

Keywords—compact model, EKV3 model, large-signal, load-pull, MOSFET model, radio frequency.

1. Introduction

The boost of wireless applications in combination with the downscaling of CMOS technologies, has posed a big challenge to the RF CMOS models, which have to be consistent with the increasing demands. Especially the design of integrated power amplifiers (PAs) in RF front-ends of wireless telecommunication circuits implemented in advanced CMOS technology requires that RF models are also validated under large-signal RF conditions where the device shows a nonlinear behavior. Such validation under more realistic operating conditions, e.g., with load-pull analysis, is however quite scarce in literature [1]–[3] for recent advanced CMOS technology.

The EKV3 is a scalable compact MOSFET model which has been designed to provide ease of parameter extraction and provide the designer insight into the device behavior. The scope of the present paper is to investigate the suitability of the EKV3 model to represent both large- and small-signal RF characteristics, from weak through moderate and strong inversion under variable bias conditions, for DC analysis, Y-parameters and load-pull analysis.

2. The EKV3 MOSFET Model

The EKV3 is an analytical compact MOSFET (metal oxide semiconductor field effect transistor) model that relies on MOSFET's physics – the charge sheet theory – to describe its behavior. EKV3 is a representant of the "charge-based" MOS transistor compact models [4], [5]. It first calculates the dependence of the mobile inversion charge density Q_i on the voltages applied to the transistor. Then, it relies on Q_i, and on its particular values Q_{iS} and Q_{iD} at the source and drain ends of the channel, to calculate the drain current and to model all aspects of the device behavior, such as transconductances, transcapacitances, noise, etc.

With the downscaling of the modern advanced CMOS technologies, the complexity of the MOSFET behavior has increased. The EKV3 model has been adapted to cover these new phenomena, such as: quantum effects; polydepletion; surface roughness, phonon- and Coulomb scattering; velocity saturation and channel length modulation; charge-sharing; drain induced barrier lowering; drain induced threshold voltage shift; reverse short- and narrow channel effect; shallow trench isolation effects; edge conductance effect; gate tunneling; layout dependent stress, induced gate noise, etc. Even though the complexity of technology has increased drastically, the EKV3 model maintains a comparatively small number of parameters and the extraction of their values can be a relatively easy procedure.

Furthermore, the RF application of a scalable, bias-dependent model [6], [7], requires that the phenomena such as transmission line effects occurring in the MOS channel (referred to as non-quasi static effects) are suitably described, which is the case in EKV3 [8]. Other high-frequency specific effects are induced gate and substrate noise, as well as increased short-channel thermal noise, which are covered in the model as well.

While at low frequencies the external resistances (except source and drain) and capacitances can be ignored, at radio frequencies they play a dominant role in the behavior of the devices, so they must be carefully modeled. Special relationships for the scaling of parasitics with the number of fingers exist [5]. EKV3 provides the possibility to choose among RF macromodels containing gate resistance, and a substrate network containing up to 5 resistances. Here, a single substrate resistance shown in the schematic representation in Fig. 1 is used, which is adequate except for a very low number of fingers.

Measurements were performed on-wafer at room temperature, and the EKV301.02 model was used for the simu-

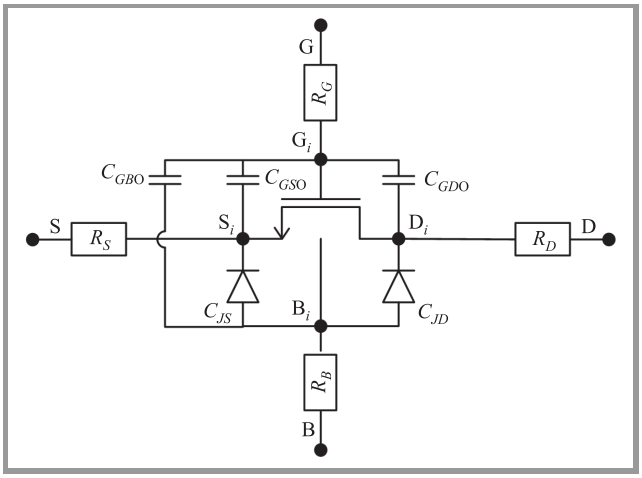

Fig. 1. EKV3 RF macromodel with a single substrate resistance.

lations. Devices with varying channel lengths, widths and number of fingers were measured to obtain a single scalable model, for NMOS and PMOS devices, similarly as shown in [7]. For the purpose of illustration, the device considered throughout the paper is an RF multifinger NMOS transistor with a minimum gate length of $L = 70$ nm, a gate width of $W = 2$ μm and number of fingers NF equal to 10. Parameter extraction was essentially performed from DC and small-signal RF measurement.

3. DC Analysis

Figure 2 shows the I_D versus V_G analysis in linear operation and saturation in linear and logarithmic scale. In addition the gate transconductance g_m versus V_G and the normalized transconductance to current ratio $g_m U_t / I_D$ versus I_D is depicted in both regions of operation. Finally, I_D versus V_D and output conductance g_{ds} versus V_D for six different values of V_G are also presented.

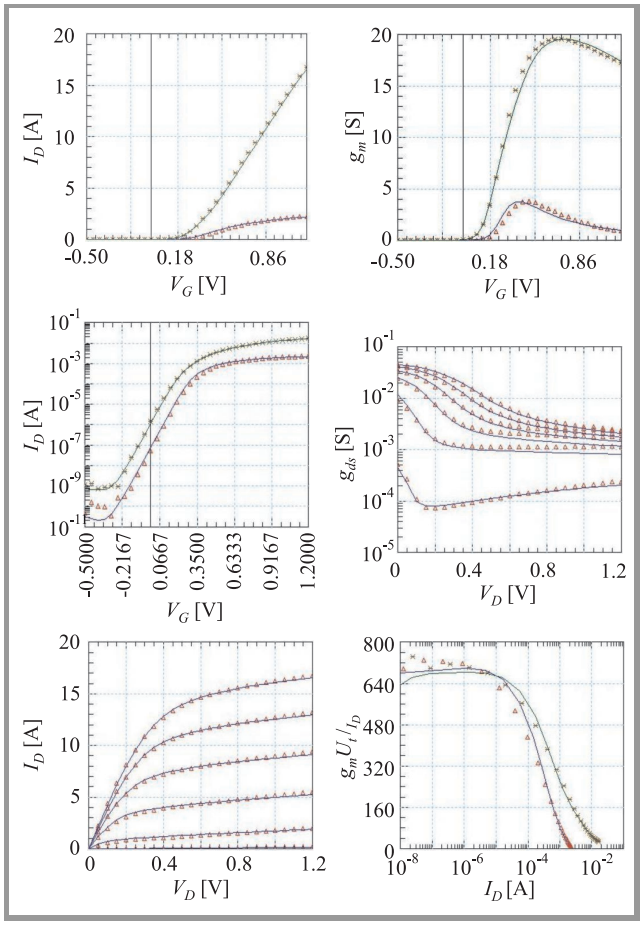

Fig. 2. Static characteristics of NMOS transistor; $L = 70$ nm; $W = 2$ μm; $NF = 10$; I_D versus V_G analysis; $V_D = 50$ mV, 1.2 V; $V_S = 0$ V; I_D versus V_D analysis; $V_G = \{0.2, 0.4, 0.6, 0.8, 1.0, 1.2\}$ V; $V_S = 0$ V. Markers: measurements, lines: EKV3 model.

The results of the DC analysis show that the EKV3 model is capable to represent with a very good accuracy the behavior of the MOSFET transistor with the incorporation of the majority of the phenomena that appear in modern CMOS ultra-deep submicron technologies.

4. Small-Signal Analysis

As the operating frequency increases to the gigahertz range, the role of the extrinsic components rivals that of the intrinsic ones. In order to have efficient circuit design and simulation, the MOS transistor models should be able to predict the behavior of the devices in a wide range of frequencies.

To evaluate the model's accuracy under small-signal conditions the transistor is considered as a two-port, where the gate is on port 1, drain on port 2, while the source is shorted to the substrate, which is the common reference terminal.

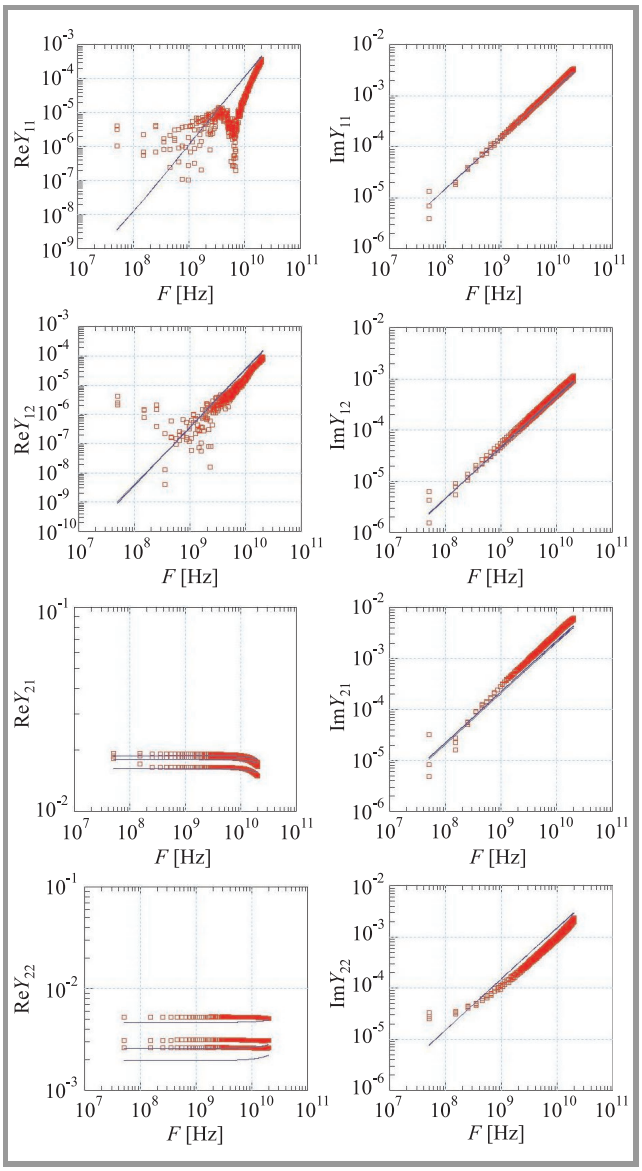

Fig. 3. Two-port small-signal Y-parameters of NMOS transistor; $L = 70$ nm; $W = 2$ μm; NF = 10; $F = 50$ MHz – 20.5 GHz; $V_G = 0.8$ V; $V_D = \{0.4, 0.6, 0.8\}$ V; $V_S = 0$ V. Markers: measurements, lines: EKV3 model.

A vector network analyzer (VNA) is then used to measure the small-signal S-parameters, which are de-embedded and then converted to Y-parameters.

In small-signal analysis, the response of the device is measured in a 50 Ω system, as a function of frequency and bias point. Then we can accurately predict the small-signal response if the device sees impedances other than 50 Ω, as the MOS transistor shows a linear behavior at low frequencies. The frequencies at which the device is tested range from 50 MHz up to 20.5 GHz.

Figure 3 shows the real and imaginary parts of the Y-parameters. These confirm that the device, under the given bias conditions, is not importantly affected by NQS (non-quasi static) effects [8], at least not below 10 GHz.

5. Large-Signal Analysis

Power amplifiers often constitute the bottleneck in using low-cost, high-density digital CMOS processes for integrating multi-gigahertz wireless application in single chips. The compact models should predict the distortion occurring in transistors operating under large-signal conditions, with acceptable accuracy. One way to check a model's capability in these conditions is to measure the load-pull characteristics.

Load-pull analysis consists of varying or "pulling" the load impedance seen by a device-under-test (DUT) while measuring the performance of the DUT. Load-pull is used to measure a DUT in actual operating conditions. This method is important since in large-signal conditions, MOS transistors show a nonlinear behavior and thus the operating point may change with power level or tuning. Load-pull analysis is usually performed at distinct frequencies, e.g., 2.4 or 5.8 GHz.

For the load-pull analysis two different measurements were carried out using two slightly different simulation setups. Firstly, output power P_{out} at operating frequency $F = 5.8$ GHz was studied when the load was varied in a specific range. Next, the gain versus input power P_{in} was examined when load (Z_L) was about 50 Ω. The difference between the two cases is that in the first one, P_{in} and terminal voltages are set but the load Z_L is varied, while in the second, Z_L is fixed at about 50 Ω and terminal voltages are set and P_{in} is varying from –20 dBm to +5 dBm. Here, for briefness, the setup that was used for the first case, using Agilent's ADS, is presented in Fig. 4.

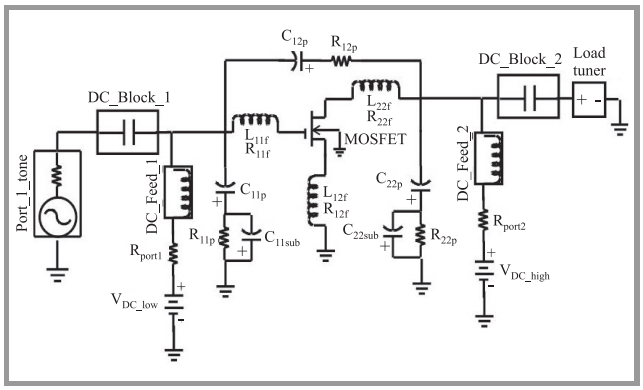

Fig. 4. Load-pull simulation setup; pulling Z_L.

The results that were obtained from the load-pull analysis when Z_L varies are displayed with the use of the Smith chart in Fig. 5. The contours represent all the different loads in the Smith chart area that result in the same transistor output power when P_{in} is constant. The node voltages that were applied to the transistor were $V_G = V_D = 0.8$ V and $V_S = 0$ V, while the input power was set at $P_{in} = 5$ dBm to ensure large-signal conditions.

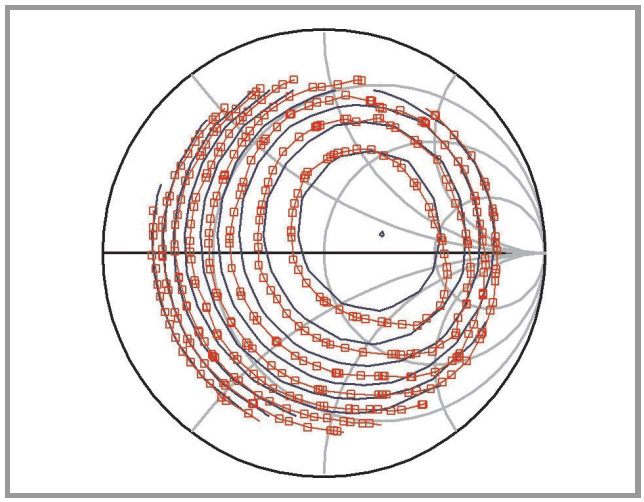

Fig. 5. P_{out} contours for an NMOS transistor pulling Z_L; $L =$ 70 nm; $W = 2$ μm; $NF = 10$; $F = 5.8$ GHz; $P_{in} = +5$ dBm; $V_G = V_D = 0.8$ V; $P_{out} = -4.65 - 3.5$ dBm (step = 0.815 dBm). Markers: measurements, lines: EKV3 model.

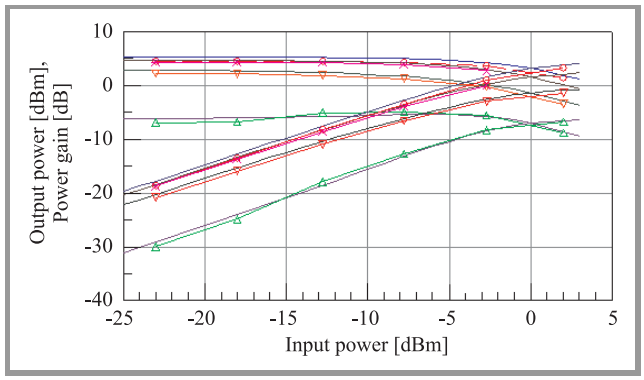

Fig. 6. Output power and power gain versus input power; NMOS transistor; $L = 70$ nm; $W = 2$ μm; $NF = 10$; $F = 5.8$ GHz; $Z_L = 50$ Ω; $P_{in} = -20 - +5$ dBm; $V_G = 0.8$ V; $V_S = 0$ V. Lines with markers: measurements, lines: EKV3 model. $V_D = 0.2$ V (triangle), 0.4 V (reverse triangle), 0.6 V (cross), 0.8 V (circle).

The EKV3 model is also consistent when considering the output power and output power gain in relation to the input

power from small- to large-signal conditions when Z_L is set to about 50 Ω as seen in Fig. 6. The gain compression is clearly apparent when input power is increased, revealing the nonlinear behavior of the transistor under large-signal conditions.

The EKV3 model depicts the output power qualitatively well, although the model tends to slightly overestimate the measured power gain at high drain voltage. Note that these results are not dependent on the number of channel segments [4], [8] used in EKV3 indicating that NQS effects are not prominent at the given conditions of analysis. When

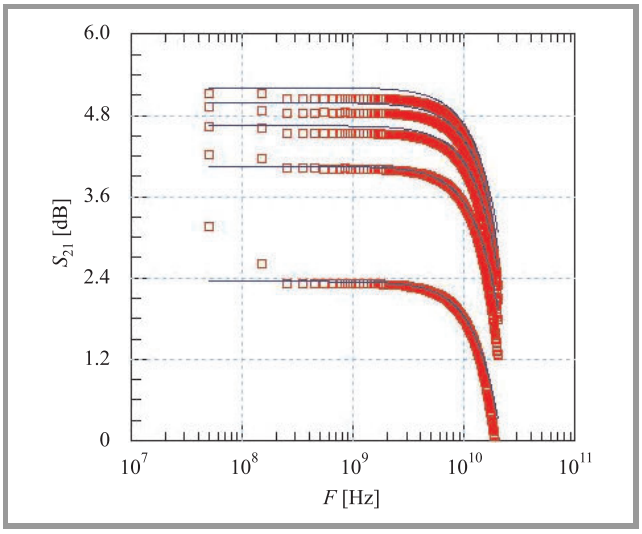

Fig. 7. Magnitude of S_{21} (small-signal) of an NMOS transistor; $L = 70$ nm; $W = 2$ μm; $NF = 10$; $V_G = 0.8$ V; $V_S = V_B = 0$ V; $V_D = \{0.4, 0.6, 0.8, 1.0, 1.2\}$ V. Markers: measurements, lines: EKV3 model.

examining the magnitude of S_{21} from small signal analysis (indicative of the RF gain), we observe that the model predicts the measurements relatively accurately, with a slight overestimation of gain by the model similarly as observed under large-signal conditions (Fig. 7).

6. Conclusion

This paper has shown the consistency of the EKV3 model in describing the MOSFET behavior covering DC analysis, small-signal S-parameter analysis up to 20 GHz, and load-pull analysis at 5.8 GHz. Extraction of RF parameters was done from the small-signal RF measurements. All results are obtained from a single RF NMOS device and the simulations are carried out with a single parameter set of the EKV3 MOSFET model, showing its capabilities in a wide range of different measurement conditions. This underlines the EKV3 model's capabilities as an RF model, including the nonlinear character of MOSFETs under high input power, which should be carefully taken into account, e.g., when designing for large-signal conditions occurring in RF power amplifiers.

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