Invited paper

SOI Technology: An Opportunity for RF Designers?

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Abstract— This last decade silicon-on-insulator (SOI) MOSFET technology has demonstrated its potentialities for high frequency (reaching cutoff frequencies close to 500 GHz for n-MOSFETs) and for harsh environments (high temperature, radiation) commercial applications. For RF and system-on-chip applications, SOI also presents the major advantage of providing high resistivity substrate capabilities, leading to substantially reduced substrate losses. Substrate resistivity values higher than 1 kΩ cm can easily be achieved and high resistivity silicon (HRS) is commonly foreseen as a promising substrate for radio frequency integrated circuits (RFIC) and mixed signal applications. In this paper, based on several experimental and simulation results the interest, limitations but also possible future improvements of the SOI MOS technology are presented.

Keywords— crosstalk, high resistivity silicon substrate, MOSFET, nonlinearities, silicon-on-insulator, wideband characterization.

1. Introduction

The semiconductor technology has been progressing enormously these last decades, such evolution has been driven by the continuous look for the increase of the operation speed and the integration density of complex digital circuits [1]. In the early 70's a scaling-down procedure of the transistor dimensions established by Dennard and coworkers [2] was proposed to pave the way to reaching both objectives. From those days to now, the keystone of the semiconductor industry has been the optimization of this scaling-down procedure.

The communication industry has always been a very challenging and profitable market for the semiconductor companies. The new communication systems are today very demanding; high frequency, high degree of integration, multi-standards, low power consumption, and they have to present good performance even under harsh environment such as high temperature, radiation, etc. The integration and power consumption reduction of the digital part will further improve with the continued downscaling of technologies. The bottleneck for further advancement is the analog front-end. Present-day transceivers often consist of three or four chipset solutions combined with several external components. A reduction of the external components is essential to obtain lower cost, power consumption and weight, but it will lead to a fundamental change in the design of analog front-end architectures. The analog front-end requires a high performance technology, like GaAs or silicon bipolar, with devices that can easily achieve operating frequencies in the GHz range. For the digital signal processor a small device feature size is essential for the implementation of complex algorithms. Therefore, it appears that only the best submicron CMOS technologies could provide a feasible and cost-effective integration of the communication systems.

This last decade metal oxide semiconductor (MOS) transistors have reached amazingly high operation speed and the semiconductor community has started to notice the radio frequency (RF) possibilities of such mainstream devices. Silicon-on-insulator (SOI) MOSFET technology has demonstrated its potentialities for high frequency (reaching cutoff frequencies close to 500 GHz for n-MOSFETs [3]) and for harsh environments (high temperature, radiations) commercial applications.

From its early development phase till recent years, SOI has grown from a mere scientific curiosity into a mature technology. Partially depleted (PD) SOI is now massively serving the 45-nm digital market where it is seen as a low cost – low power alternative to bulk silicon. Fully depleted (FD) devices are also widely spread as they outperform existing semiconductor technologies for extremely low power analog applications [4].

For RF and system-on-chip applications, SOI also presents the major advantage of providing high resistivity substrate capabilities, leading to substantially reduced substrate losses. Substrate resistivity values higher than 1 kΩcm can easily be achieved and high resistivity silicon (HRS) is commonly foreseen as a promising substrate for radio frequency integrated circuits (RFIC) and mixed signal applications [5].

In this paper, based on several experimental and simulation results the interest, limitations but also possible future improvements of the SOI MOSFET technology for microwaves and millimeter-waves applications are presented.

2. State of the Art RF Performance

Since the invention of the bipolar transistor in 1947, the operating frequencies of integrated transistors have been improved every year. In 1958, a cut-off frequency above 1 GHz is reached with a germanium bipolar transistor [6]. Since that date, several integrated technologies have been investigated and improved to further increase the operating frequency of transistors. In 1965, a GaAs metal semiconductor field effect transistor (MESFET) appears in the literature [7]. In 1973, a maximum oscillation frequency ($f_{\max}$) of 100 GHz is measured for a FET [8]. In 1980, a new architecture of field effect transistor with high electron mo-

bility (HEMT) is proposed and fabricated [9]. In 1995, a cutoff frequency $f_{\max}$ higher than 500 GHz is extrapolated for a HEMT [10]. In 2000, the limit of 1 THz is reached with III-V heterostructure bipolar transistor (HBT) [11] and even overpassed by HEMT in 2007 [12].

It is only in 1996, thanks to the successful downscaling of the silicon MOSFET gate, that cutoff frequencies higher than 200 GHz are presented [13]. Since that date, the interest in MOSFETs for low voltage, low power, high integration mixed-mode ICs (digital and analog parts on the same chip) in the field of microwaves and millimeter-waves applications has been constantly growing. MOSFET is a well-known, well-controlled and mature technology, as well as cost effective, which makes it the key technology for mass production.

Nowadays, thanks to the introduction of mobility booster such as strained silicon channel, cutoff frequencies close to 500 GHz and 350 GHz are achieved, respectively, for n- and p-MOSFETs [3] with the channel length of 30 nm.

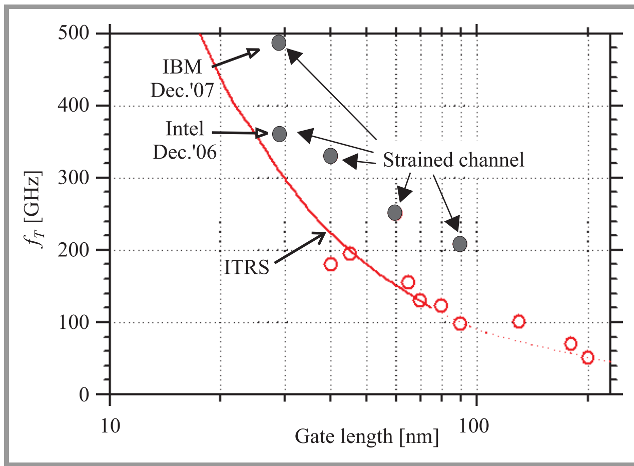

Fig. 1. State of the art current gain cutoff frequency as a function of gate length for unstrained and strained Si and SOI NMOSFETs.

Figure 1 presents the state of the art current gain cutoff frequency (f_T) for n-type MOSFETs as a function of gate length. In that graph, the continuous line represents the prediction from the International Technology Roadmap for Semiconductors (ITRS) published in 2006 [14]. Despite the poor carrier mobility of electrons in silicon compared to III-V materials, silicon MOSFET can be considered as a competitive technology for high frequency applications. It is worth to notice that strained channel silicon MOSFETs even overcome the ITRS roadmap values which gives quite good prospects for silicon technology still for certainly more than 15 years from now on.

3. Main Limiting Factors

Historically, device scaling remains the primary method by which the semiconductor industry has improved productivity and performance. From the 100-nm technology node, CMOS technologies have been facing many grand technological challenges. In this context, the most critical issue consists in the so-called short-channel effects (SCE).

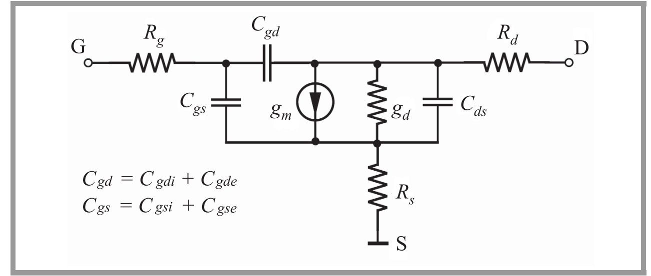

Fig. 2. Small-signal lumped equivalent circuit of MOSFET.

These parasitic effects tend to degrade the subthreshold characteristic, increase the leakage current and lead to a dependence of threshold voltage with respect to the channel length. Those static SCE have been reported theoretically and experimentally in the literature and solutions have been proposed. However, only a few publications have analyzed the limitation or degradation of high frequency characteristics versus the downscaling of the channel length. Considering a classical small-signal equivalent circuit for MOSFET as presented in Fig. 2, we can define the cutoff frequencies f_c, f_T and $f_{\max}$ representing the intrinsic (related to the useful MOSFET effect), the current gain and the available power gain cutoff frequencies, by expressions (1) to (3), respectively:

$$f_c = \frac{g_m}{2\pi C_{gs}}, \tag{1}$$

$$f_T \approx \frac{f_c}{\left(1+\frac{C_{gd}}{C_{gs}}\right)+\left(R_s+R_d\right)\left(\frac{C_{gd}}{C_{gs}}\left(g_m+g_d\right)+g_d\right)}, \tag{2}$$

$$f_{\max} \approx \frac{f_c}{2\left(1+\frac{C_{gd}}{C_{gs}}\right)\sqrt{g_d\left(R_g+R_s\right)+\frac{1}{2}\frac{C_{gd}}{C_{gs}}\left(R_s g_m+\frac{C_{gd}}{C_{gs}}\right)}}, \tag{3}$$

where: g_m – the gate transconductance, g_d – the ouput conductance, C_{gs}, C_{gd} and C_{ds} – the gate-to-source, gate-to-drain, and drain-to-source capacitances, respectively, R_g, R_d and R_s – the gate, drain and source access resistances, respectively.

Figure 3 represents a schematic cross-section of a classical silicon MOSFET where the different components of parasitic source and drain resistances and capacitances are illustrated.

The intrinsic cutoff frequency, f_c, measures the intrinsic ability of a field effect transistor (FET) to amplify high frequency signals. As reported in [15], the f_c values are a factor of 1.5 to 2 higher for HEMTs than for silicon MOSFETs with comparable gate length, and this is mainly explained by the respective dynamic properties of the two types of semiconductors (difference of g_m which is directly proportional to the carrier mobility). In order to enhance

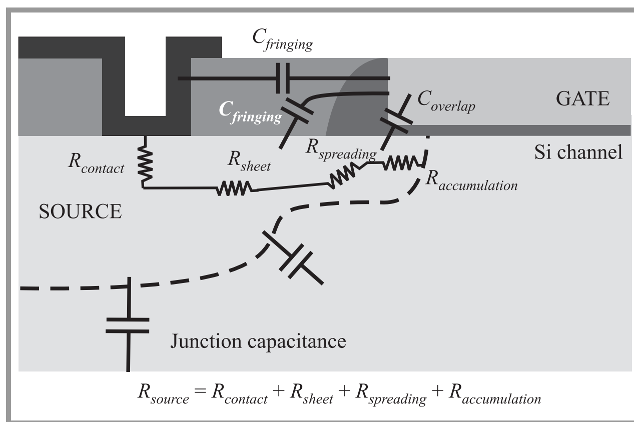

Fig. 3. Schematic cross-section of a Si MOSFET illustrating the different access resistances to the channel and the surrounding overlap and fringing capacitances.

the carrier mobility in silicon channel and then to improve the current drive and high frequency characteristics [3] of MOSFETs, strained n- and p-MOSFETs have been investigated these last years. Beside the carrier mobility difference between Si and III-V materials, it has been demonstrated that the $f_{\max}/f_T$ ratio is lower in the case of Si devices. As explained in [15], besides the well-know degradation of high frequency characteristics due to access resistances (R_g, R_d and R_s), the decrease of the ratios g_m/g_d and C_{gs}/C_{gd} in CMOS technology strongly contributes to the limiting improvement of f_T and $f_{\max}$ with the transistor channel length skrinkage. The increase of the output conductance, g_d, with the reduction of gate channel length is one of the well-known short channel effects of FET devices. The degradation of the ratio C_{gs}/C_{gd} means a loss of channel charge control by the gate and an increase of the direct coupling capacitance between gate (input) and drain (output) terminals. The self-aligned source and drain regions, one of the main advantages of MOSFET structure, are also a reason for the increase of parasitic capacitances between source and gate and more importantly drain and gate. As demonstrated in [15], from extraction results the C_{gs}/C_{gd} ratio is equal to 7.8 for the HEMT and only to 1.5–1.6 in the case of a MOSFET with 90 nm gate length.

It is therefore obvious that the optimization of these internal parameters will be crucial in order to further improve cutoff frequencies of ultra deep submicron MOSFETs. The impact of lightly doped drain (LDD) dose and energy implant as well as annealing temperature and time on C_{gs}/C_{gd} ratio, g_m and g_d and then on $f_{\max}$ has been investigated in [16]. The results demonstrate that LDD implant can indeed be considered as an optimization parameter for improving $f_{\max}$ and especially the ratio $G_{ass}/NF_{\min}$ (G_{ass} and $NF_{\min}$ being the associated power gain and the minimum RF noise figure, respectively), which is the most important figure of merit for low noise microwave applications. However, the optimization window is quite narrow and it seems difficult for a given technological node to get higher C_{gs}/C_{gd} and g_m/g_d ratios than 2 and 6, respectively, for a classical sub-100-nm gate length MOSFET structure. It is the main reason why $f_{\max}$ is almost equal to f_T in the case of MOSFETs and not 1.5 to 2 times higher as in the case of HEMTs with similar gate length and characterized by C_{gs}/C_{gd} and g_m/g_d ratios of 8 and 20, respectively.

In order to further improve the microwave performance of deep submicrometer MOSFETs, it seems crucial to keep the parasitic resistances and capacitances as low as possible, as predicted by ITRS and shown in Fig. 4 and to consider alternative MOS structures for which the C_{gs}/C_{gd} and g_m/g_d ratios (analog SCE) are improved.

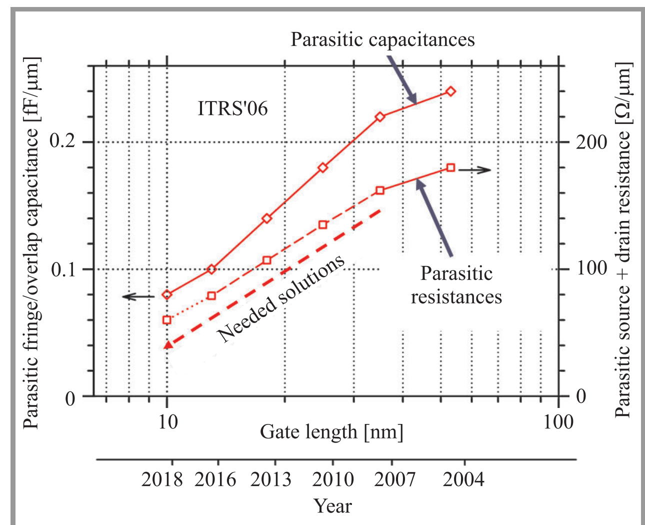

Fig. 4. Parasitic capacitances and source, and drain resistances as a function of the gate length published in ITRS'06 [12].

Several technological options have been presented in the litterature those last years to push further the digital and analog performance limits of single gate Si MOSFETs such as:

- Move from bulk Si MOSFETs to partially depleted [17] or fully depleted [18] SOI MOSFETs to enhance the gate electrostatic control on the channel carriers and thus minimize the SCE. Nowadays, ultra thin body (UTB) MOSFET in SOI technology with a silicon body thickness less that 10 nm has been proposed [19], [20]. Thanks to the buried oxide layer (BOX) underneath the SOI transistors, their junction capacitances (noted *Junction capacitance* in Fig. 3) to the Si substrate are drastically reduced.
- Strained MOSFETs have been largely investigated lately to improve the carrier mobility. The mechanical stress in the channel orginates from specific process steps [21] added into the classical CMOS process flow. Nowadays, strained SOI wafers are produced as well for which the top silicon layer is under a certain level of stress [22], [23].
- Low Schottky barrier contacts [24]–[28] are foreseen as a very interesting candidate to lower the source/drain contact resistances, to form abrupt junctions (no overlap), and drastically reduce the thermal budget for CMOS process.

- Metal gate allows to get rid of loss of electrostatic gate control related to the polysilicon gate depletion [29], [30], as well as to reduce the gate sheet resistance.
- Low-k and air gap [31], [32] should be introduced to reduce fringing capacitances between gate-to-source and gate-to-drain electrodes.
- SOI wafers with thin BOX have been proposed these last years to reduce SCE (for instance, DIBL) but also to lower self-heating issues [19], [20], [33], [34].
- High resistivity silicon substrate has demonstrated superior characteristics for the integration of high quality passive elements such as transmission lines [35], inductors [36], etc., as well as for reduction of the crosstalk between circuit blocks integrated on the same silicon chip [5].

This last point will be developed in detail in Section 5. Figure 5 schematically presents the cross-section of what we can call an ultimate single gate MOSFET basically including the technological options listed above. Unstrained p-type MOSFET including a metal gate and low Schottky barrier source and drain contacts has been built and characterized over a wide frequency band in [27]. The device architecture features a 20 nm thick SOI channel, a 2.4 nm SiO_2 gate oxide, a metallic tungsten gate and 15 nm-wide SiN spacers. The integration of a low Schottky barrier silicide (PtSi) coupled to boron segregation demonstrates a 50% improvement on the current drive accompanied by reinforced immunity against SCE when compared to the dopant-free approach. This constitutes the first implementation of a dopant segregated band-edge silicide obtained by implant-to-silicide (ITS) and activated at low temperature (500°C). The RF characterization unveils a unity current gain cut-off frequency f_T of 180 GHz for a 30 nm gate long device as shown in Fig. 6. This constitutes the best result reported in literature [37] for unstrained channel fully depleted SOI p-MOSFETs.

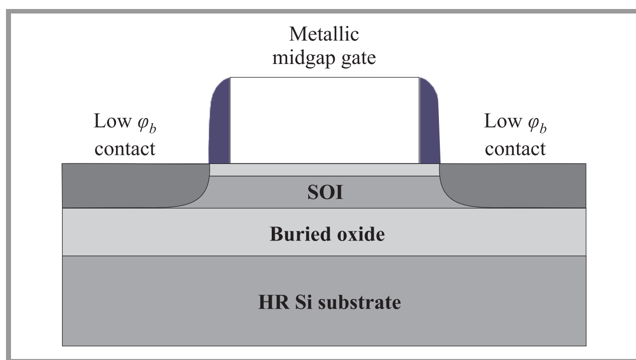

Fig. 5. Schematic cross-section view of an optimized single fully depleted SOI MOSFET.

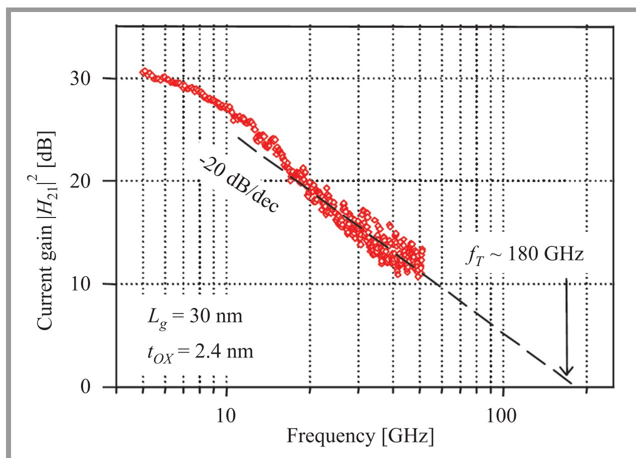

Fig. 6. Current gain as a function of frequency for a 30 nm p-type segregated PtSi Schottky barrier MOSFET.

Multiple gate MOSFETs are often cited as the ultimate MOS devices to reduce the SCE. The analog and RF performances of FinFETs are presented in the following section.

4. RF Performance of a Multigate MOSFET: FinFET

To reduce the SCE in nanometer scale MOSFETs, multiple-gate architectures emerge as one of the most promising novel device structures, thanks to the simultaneous control of the channel by more than one gate. The idea of the double-gate (DG) MOSFET was first introduced by J.-P. Colinge [38]. Starting by the FinFET [39], other multiple-gate SOI MOSFETs have been introduced since [40] such as triple-gate (TG), FinFET, pi-gate (PG), quadruple-gate (QG), omega-gate (Ω-G), etc. Many works have investigated and demonstrated the great potential of multiple-gate devices to comply with the I_{on}/I_{off} requirements of the ITRS for logic operation [40], [41].

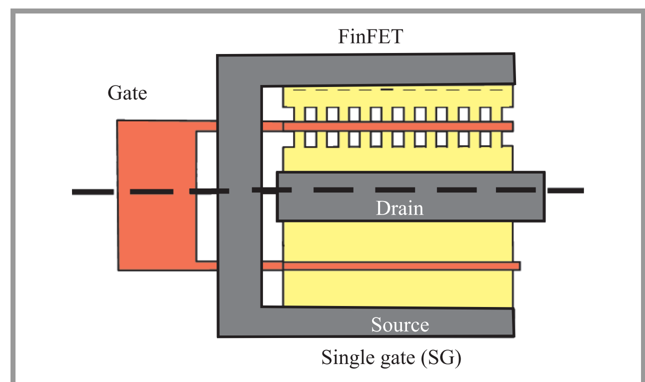

Fig. 7. Schematic top view of a FinFET composed of 10 fins (upper) and SG MOSFET (lower) occupying the same active silicon foot print.

Indeed, FinFETs are known to be promising devices for high density digital applications in the sub-65 nm nodes due to their high immunity to short channel effects and their excellent compatibility with planar CMOS process. Most

Fig. 8. DC and RF characteristics of 60 nm gate length FinFET for various fin widths (W_{fin}): (a) transfer characteristic in log scale; (b) extracted access resistances; (c) transfer characteristic in linear scale and gate transconductance; (d) current gain and maximum available power gain versus frequency.

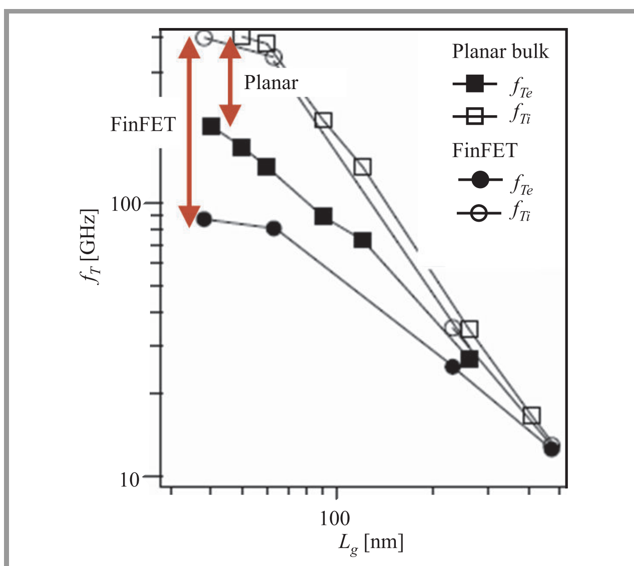

Fig. 9. Extracted intrinsic (f_{Ti}) and extrinsic (f_{Te}) current gain cutoff frequencies for a SG MOSFET and FinFET as a function of the channel length.

of the investigations performed on FinFETs have focused on their technological aspects and perspectives for digital applications [42], [43], while only a few have assessed their analog figures of merit [44], [45]. In this section, the RF performance of FinFETs with various geometries is presented.

FinFETs are fabricated on a SOI wafer with 60 nm Si film on 145 nm of buried oxide, with $< 100 >$ and $< 110 >$ Si planes for top and lateral channels, respectively. The silicon active area is patterned using 193 nm lithography with aggressive resist and oxide hard mask trimming to define narrow silicon fins. A hydrogen anneal and a sidewall oxidation are used for surface smoothening and corner rounding. The fin patterning resulted in a fin height (H_{fin}) of 60 nm, fin width (W_{fin}) of 22, 32 and 42 nm, and fin spacing (S_{fin}) of 328 nm. The gate stack consisting of a plasma nitrided oxide with equivalent oxide thickness equal to 1.8 nm, as measured on planar devices, and 100 nm polysilicon is deposited. Gate lengths (L_g) of 40, 60 and 120 nm are fabricated. High angle As/BF_2 extensions are then implanted and a 40 nm-thick selective epitaxial growth (SEG) is per-

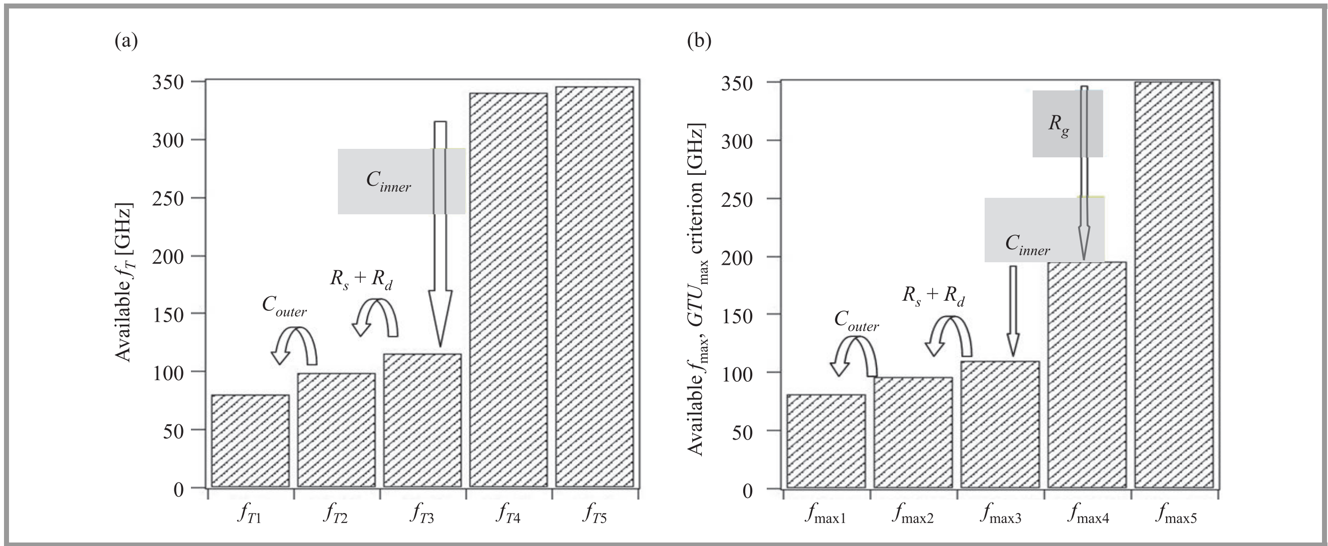

Fig. 10. Analysis of the relative impact of each lumped extrinsic parameters on (a) the current gain cutoff frequency (f_T) and on (b) the maximum available gain cutoff frequency (f_{max}) for a 60 nm long FinFET.

formed on the source and drain regions. After the heavily doped drain (HDD) implantations and rapid thermal annealing (RTA), NiSi is used as silicide and only one metal level is deposited.

The DC and RF analyses are performed on RF FinFETs (Fig. 7) composed of 50 gate fingers (N_{finger}) controling 6 fins (N_{fin}) each. As shown in Fig. 8(a) the 60 nm technology investigated here outlines a good control over SCE, with a subthreshold slope (S) close to 73.5 mV/dec. This value is even closer to ideal for $L_g = 120$ nm ($S =$ 62.9 mV/dec). Data in Fig. 8 are normalized by considering the total gate width $W_{tot} = N_{finger} N_{fin} (W_{fin} + 2H_{fin})$. No threshold voltage ($V_T$) roll off was observed with respect to $L_g (V_T \sim 260$ mV) and only small V_T variations (within 30 mV) are recorded as a function of W_{fin}. As expected, the devices also exhibit reduced SCE as the fin width is reduced. This is shown in Fig. 8(a), which indicates lower S values for narrower fins. However, reducing W_{fin} is also expected to increase the source (R_s) and drain (R_d) resistance [46], as shown in Fig. 8(b), which leads to a reduction of the normalized drain current as well as the effective gate transconductance (Fig. 8(c)).

The S-parameters of the devices are measured with a 110 GHz VNA from Agilent. An open-short deembedding step is performed to remove the parasitics associated with the access pads. The current gain ($|H_{21}|$) as a function of frequency which yields the device transition frequency (f_T) is presented in Fig. 8(d) for FinFETs with different fin widths. Unfortunately, we can observe a reduction of the cutoff frequency with the shrinkage of W_{fin}. This degradation is mainly related to the increase of the source and drain resistances with the thinning down of the fin width (Fig. 8(b)).

The DC and RF performances of planar MOSFETs with similar dimensions (Fig. 7) have been measured for comparison purposes. Figure 9 presents the extracted RF cutoff frequencies of planar and FinFET devices as a function of channel length. The so-called intrinsic (f_{Ti}) and extrinsic (f_{Te}) cutoff frequencies stand, respectively, for the current gain cutoff frequency related to only the intrinsic lumped parameter elements (g_m, g_d, C_{gsi} and C_{gdi}) and the complete small-signal equivalent circuit presented in Fig. 2 (including the parasitic capacitances, C_{gse} and C_{gde}, as well as the accesss resistances R_s, R_d, and R_g). It is quite interesting to see that both devices present similar intrinsic cutoff frequencies (around 400 GHz for a channel length of 60 nm) but the extrinsic cutoff frequency, f_{Te}, of FinFET (90 GHz) is nearly twice lower than that of the planar MOSFET (180 GHz). A possible explanation for the latter effect might be the more relevant impact of extrinsic capacitances and resistances in the case of short gate length FinFETs.

Based on a wideband analysis, the lumped small-signal equivalent circuit parameters (Fig. 2) are extracted from the measured S-parameters according to the methods described in [47] and [48]. Figure 10 shows the relative impact of each parasitic parameter on the current gain (f_T in Fig. 10(a)) and maximum available power gain (f_{max}, Fig. 10(b)) cutoff frequencies of a 60 nm long FinFET. As expected from the expressions (1)–(3) and the published results for SG MOSFETs [49] the gate resistance has an important impact on f_{max} whereas f_T is unchanged. The sum of fringing capacitances C_{inner} directly linked to the FinFET three-dimensional (3D) architecture has a huge impact on both cutoff frequencies. In fact, f_T and f_{max} drop down, respectively, by a factor of 3 and 2. Finally, the source and drain resistances as well as the parasitic capacitances related to the feed connexions outside the active area of the transistor slightly decrease both cutoff frequencies. Based on that analysis, it is quite clear that the fringing capacitances inside the active area of the FinFET are the most important limiting factor for this type of non-planar multiple gate transistors.

In [50], Wu and Chan analyze the geometry-dependent parasitic components in multifin FinFETs. Parasitic fringing capacitance and overlap capacitance are physically modeled as functions of gate geometry parameters using the conformal mapping method. The relative contribution from each part of the 3D geometry of the FinFET is calculated. They subdivide the fringing capacitances in 3 distinct components noted C_1, C_2 and C_3 in Fig. 11(a). They demonstrate the importance of the fringing capacitance C_3 (Fig. 11(b)) which orginates from the capacitive coupling between the source and drain regions of the fins (side walls) and the gate electrode located between fins assuring the electrical connection between the gates wrapping the different fins connected in parallel through the source and drain contacts.

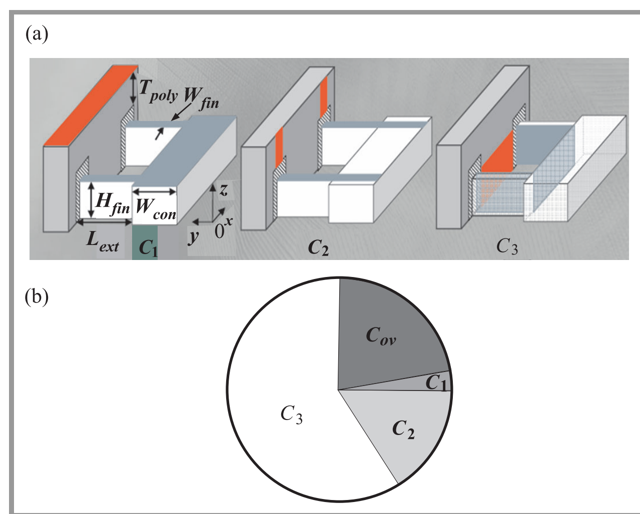

Fig. 11. (a) Three-dimensional schematic presentation of the various contributions of the fringing capacitances for a FinFET (C_1, C_2, C_3); (b) relative importance of each fringing capacitance (C_1, C_2, C_3) and overlap capacitance (C_{ov}).

In [51] and [52], the authors have demonstrated based on finite element numerical simulations the possibility to reduce C_{inner} and thus its impact on the FinFET cutoff frequencies by reducing the fin spacing (Fig. 12(a)) or by increasing the aspect ratio of the fin (higher H_{fin}/W_{fin} – see, Fig. 12(b)), respectively.

Figure 13 shows the extracted input capacitance ($C_{gg} = C_{gs} + C_{gd}$) in strong inversion ($V_g = 1.7$ V and $V_d = 0$ V) as a function of the active gate width (W_{tot}) for a FinFET and a SG MOSFET with 60 nm gate length. Both devices are built simultanuously on the same SOI wafer. A first order extrapolation of the measured data yields C_{gg} values of 1.33 fF/μm for the FinFET devices and only 1.09 fF/μm of active gate width for the SG, indicating a 20% increase of input capacitance in the case of FinFETs. Assuming that the normalized oxide capacitance is equal in both SG and FinFET devices, this increase is solely due to additional fringing in FinFETs. Using additional capacitance data measured in deep depletion, the extrinsic gate capacitance is actually found to be 40% higher for FinFETs. As explained above, this higher normalized input capacitance for FinFET can be explained by the fact that the gate fingers must run over non active area between each pair

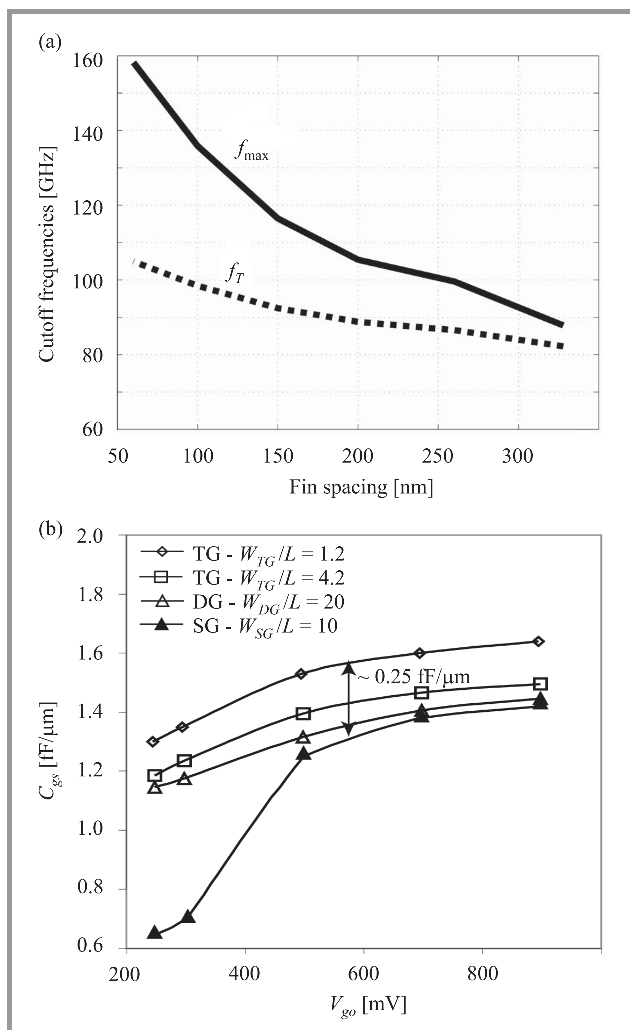

Fig. 12. (a) Cutoff frequencies of FinFETs versus fin spacing; (b) effect of W/L ratio on the normalized C_{gs} extracted at $V_d = 1$ V at various V_{go} and $L = 100$ nm.

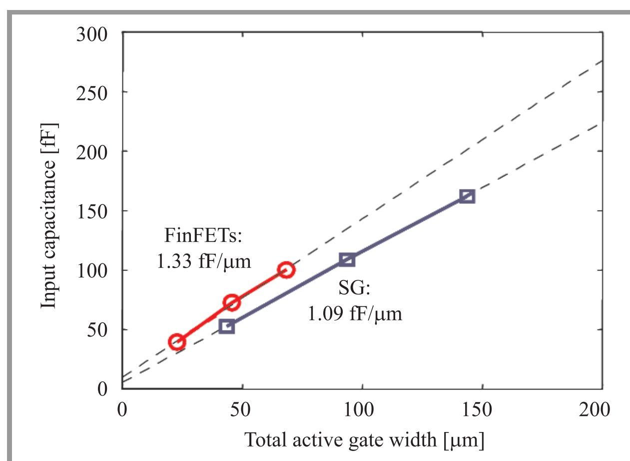

Fig. 13. Extracted input capacitance in strong inversion ($V_g = 1.7$ V and $V_d = 0$ V) as a function of W_{tot} for 60 nm SG MOSFET and 60 nm FinFET.

of parallel fins, a situation that is not encountered in SG MOSFETs.

To summarize, the simulation and experimental results indicate that FinFET is a multiple gate structure of interest to reduce digital short channel effects and then assure a lower threshold voltage roll-off, a better subthreshold slope and then higher I_{on}/I_{off} ratio, but the high frequency performance such as the cutoff frequencies as well as RF noise figure as presented in [53] are degraded compared to its SG MOSFET counterpart because of the increased fringing capacitance linked to its complex 3D non-planar architecture. Consequently, a trade-off exists regarding W_{fin} between high f_T and $f_{\max}$ (large W_{fin}) and good control of SCE (small W_{fin}).

5. High Resistivity SOI Substrate

5.1. Coplanar Waveguides Transmission Lines

The use of high resistivity silicon substrate is mandatory to reduce as much as possible the high frequency losses associated with the substrate conductivity. High resistivity silicon substrate cannot be introduced in the case of bulk Si MOSFETs due to the problem related to latch-up between devices. In SOI technology, thanks to the buried oxide the thin top silicon layer in which the transistors are implemented is electrically isolated from the Si substrate which can have high resistivity without impacting the good behavior of the MOS integrated circuits (ICs). Recently, high quality coplanar waveguides (CPW) presenting insertion loss of less than 2 dB/mm at 200 GHz as well as low- and high-pass filters at millimeter waves have been succefully built in an industrial SOI CMOS process environment [54].

The insertion loss of a CPW line lying on a lossy silicon substrate depends on the conductor loss (α_{cond}) and the substrate loss (α_{sub}) which is inversely proportional to the effective resistivity of the substrate. The effective resistivity represents the value of the substrate resistivity that is actually seen by the coplanar devices. This parameter accounts for the wafer inhomogeneities (i.e., oxide covering and space charge effects) and corresponds to the resistivity that a uniform (without oxide nor space charge effects) silicon wafer should have in order to sustain identical RF substrate losses. The effective resistivity is extracted from the measured S-parameters of the CPW line with a method depicted in [55].

Simulation results displayed in Fig. 14 outline how this parameter affects substrate and total losses for a 50 Ω CPW with 1 μm-thick Al line, the central conductor width of 40 μm and spacing between conductors of 24 μm. These data are obtained with analytical formulas presented in [56] and assuming metal conductivity of $3 \cdot 10^7$ S/m. It is seen that substrate losses (α_{sub}) are small (~ 0.1 dB/cm) when ρ_{eff} is close to 3 kΩcm and become clearly meaningless compared to conductor losses (α_{cond}) when ρ_{eff} reaches 10 kΩcm.

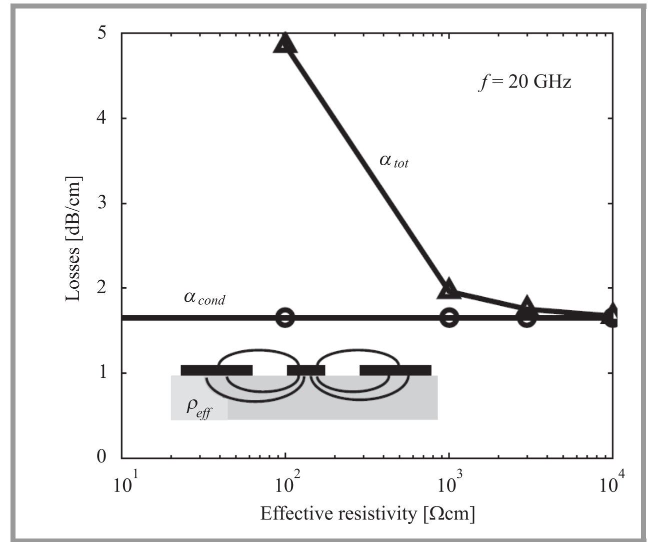

Fig. 14. Total (α_{tot}) and conductor (α_{cond}) losses as a function of ρ_{eff} at 20 GHz for a CPW line geometry according to [56].

Keeping substrate losses at low levels is a priority target when designing high performance integrated silicon systems. In this field, high resistivity (> 3 kΩcm) silicon wafers are foreseen as promising candidates for radio frequency integrated circuits [57] and mixed signal applications [58]. However, oxide passivated high resistivity (HR) wafers are known to suffer from parasitic surface conduction due to fixed charges (Q_{ox}) in the oxide [59]. Indeed, charges within the oxide attract free carriers near the substrate surface, reducing the effective resistivity (ρ_{eff}) seen by coplanar devices and increasing substrate losses. It has been recently shown in [60] that values as low as $Q_{ox} = 10^{10}/\text{cm}^2$ could lower the value of resistivity by more than one order of magnitude in the case of 50 Ω CPW transmission line. The parasitic surface conduction can also be formed underneath metallic lines with the application of a DC bias (V_a) [61].

The extracted line loss and effective substrate resistivity as a function of the DC bias applied to the central conductor of a CPW line are, respectively, presented in Figs. 15(a) and 15(b) for different substrates, oxide layers and metallic lines as summarized in Table 1. Techno A and B are wafers coming from the industry while the three other wafers named C, D and E are home processes with one metal layer. In all cases, the metallic structures are patterned on either oxidized p-type HR unibond SOI (techno A, B, C) or oxidized p-type HR bulk Si (techno D and E) substrates.

The total RF losses (α_{tot}) of the CPW lines are extracted from the measured S-parameters with a thru-line-reflect method [62]. They are reported at 10 GHz in Fig. 15(a) as a function of V_a, where it is seen that α_{tot} may be significantly affected by V_a when the oxide thickness (t_{ox}) is in the several hundreds of nanometers (techno C). Indeed, in that case highly positive or negative biases have a large impact on the free carrier concentration below the oxide, thereby strongly affecting substrate losses. This effect is attenu-

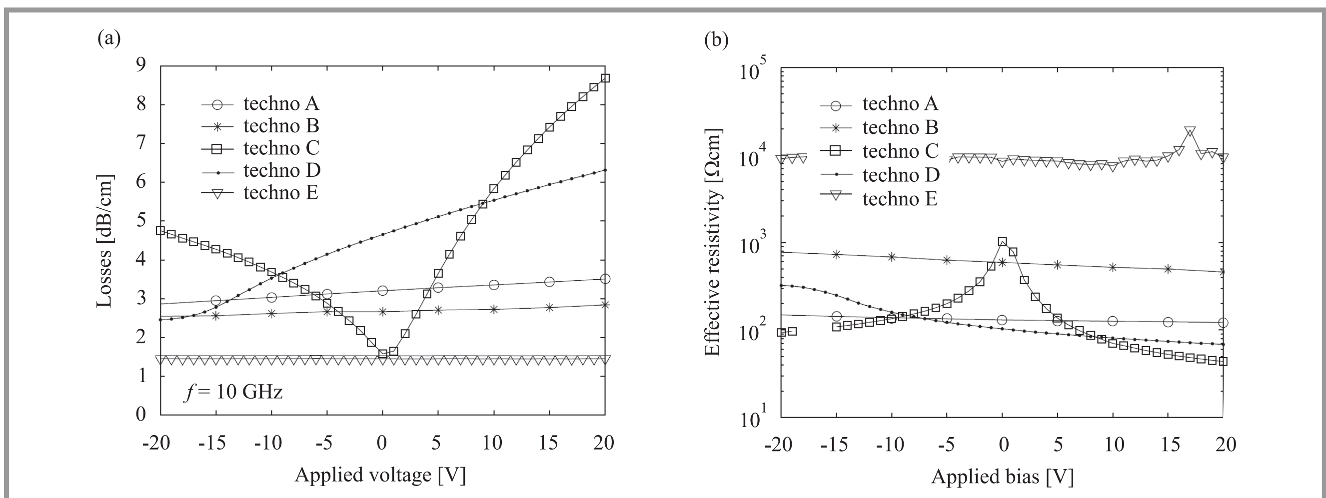

Fig. 15. (a) CPW losses and (b) effective substrate resistivity measured for different technologies described in Table 1 as a function of DC bias applied to the CPW central conductor.

Table 1
Additional information on the different technologies investigated in Fig. 15.

Techno	Starting wafer	Metal layers	Oxide thickness [μm]	Si passivation	Oxide type
A	HR SOI	M3	3	No	BOX + oxidized SOI + interlayer dielectrics
B	HR SOI	M5–M6	4.1	No	BOX + oxidized SOI + interlayer dielectrics
C	HR SOI	M1	0.3	No	BOX + oxidized SOI
D	HR Si bulk	M1	1	No	PECVD
E	HR Si bulk	M1	1	Polysilicon	PECVD
The data in columns 3 and 4, respectively, indicate the metal levels that were used and the total equivalent oxide thickness for CPW lines.					

ated for thicker oxides (techno A, B and D). The V_a value for which losses are minimum ($V_{a,\min}$) corresponds to the state of deep depletion underneath the oxide. As shown in Fig. 15, the V_a depends on the flatband voltage (V_{FB}) of the structure and is therefore dependent on t_{ox} as well as the oxide charge density (Q_{ox}).

The parasitic surface conduction can be reduced or even suppressed if the silicon substrate is passivated before oxidation with a trap-rich, highly resistive layer.

Figure 16 illustrates the impact of trap density (D_{it}) at the HR Si substrate/SiO_2 interface on the value of ρ_{eff} at 0 V for several Q_{ox} densities. It is seen with no surprise that the minimum D_{it} level that is required to obtain lossless substrates (i.e., $\rho_{eff} = 10$ kΩcm) is an increasing function of the fixed charge density in the oxide. This is because for higher positive densities, a higher concentration of electrons is attracted near the substrate surface and a higher density of traps is required to absorb those charges.

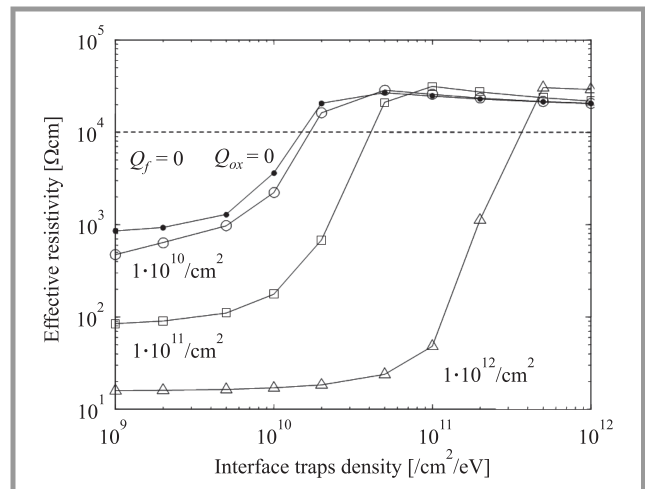

Fig. 16. Simulated effective resistivity values ρ_{eff} as a function of the trap density D_{it} for several fixed charges densities Q_{ox} and an applied bias value of 0 V.

The introduction of a high density of traps at the Si/SiO_2 interface has been successfully achieved using low-pressure chemical vapor-deposited (LPCVD) polysilicon (polySi) and amorphous silicon (α-Si) in [63] and [64], respectively. In the context of SOI technology, substrate passivation could also be an efficient technique to reduce substrate losses. To be compatible with a HR SOI wafer fabrication

process, the passivation layer should be included within the SOI structure by bonding an oxidized silicon wafer with a passivated HR substrate.

In [65], the proposed method consists in the LPCVD-deposition of amorphous silicon followed by Si-crystallization at 900°C with RTA. This method was compared with previously published techniques (passivation with amorphous silicon in [64] or LPCVD-polysilicon in [63] and was demonstrated to perform better in terms of substrate loss reduction: effective resistivity values higher than 10 kΩcm were reported, compared to 3 and 6 kΩcm in the case of amorphous Si and LPCVD polySi passivation, respectively. The new passivation method was also shown to present better rms surface roughness ($\sigma = 0.37$ nm) and to remain effective after long thermal anneals (4 hours at 900°C). A successful bonding of this layer with an oxidized substrate was achieved, showing that this new passivation technique could be introduced at reduced cost inside a smartcut or BESOI process in order to fabricate SOI wafers with enhanced resistivity, i.e., higher than 10 kΩcm.

Figure 15(a) indicates that substrate passivation with polysilicon (techno E) significantly reduces RF losses while getting rid of the V_a influence. This is because traps present inside the polySi layer can absorb free carriers and pin the surface potential to a value independent on V_a [63]. Figure 15(b) presents the effective resistivity (ρ_{eff}) extracted according to a method depicted in [55]. Not surprisingly, the highest ρ_{eff} value is observed for the passivated substrate, while at 0 V, the lowest value is obtained for the low quality (Q_{ox}-rich) PECVD oxide. It should also be noticed that due to the inverted layer underneath the BOX in techno A and B, the extracted values of ρ_{eff} do not exceed 130 and 580 Ωcm, respectively. These values are both more than one order of magnitude lower than the nominal substrate resistivity.

5.2. Crosstalk

In recent years, rapid progress of integrated circuit technology has enabled the co-integration of analog front-end and digital baseband processing circuits of communication systems onto the same chip. Such mixed-signal systems-on-chip (SoCs) allow more functionality, higher performance, lower power and higher reliability than non-integrated solutions, where at least two chips are needed, one for digital and one for the analog applications. Moreover, thanks to CMOS technology scaling and its associated increasing integration level, SoCs have become the way to achieve cost effectiveness for demanding applications such as home entertainment and graphics, mobile consumer devices, networking and storage equipment.

Such a rising integration level of mixed-signal ICs raises new issues for circuit designers. One of these issues is the substrate noise (Fig. 19(a)) generated by switching digital circuits, called digital substrate noise (DSN), which may degrade the behavior of adjacent analog circuits [66]. DSN issues become more and more important with IC evolution as

- digital parts get more noisy due to increasing complexity and clock frequencies;
- digital and analog parts get closer;
- analog parts get more sensitive because of V_{dd} scaling for power concern issues.

In general, substrate noise can be decomposed in three different mechanisms: noise generation, injection/propagation into the substrate and reception by the analog part [67]. Improvement in the reduction of any of these three mechanisms, or in all of them, will lead to a reduction of the DSN and in a relaxation of the design requirements. Typically, guard rings and overdesigned structures are adopted to limit the effect of substrate noise, thereby reducing the advantages of the introduction of new technologies. It is thus a major issue for the semiconductor industry to find area-efficient design/technology solutions to reduce the impact of substrate noise in mixed-signal ICs.

This last decade several publications have demonstrated theoretically and experimentally the interest of high resistivity SOI substrate to greatly reduce the crosstalk level between integrated circuits [5]. Figure 17 shows how the crosstalk between two 50 μm spaced metallic pads is affected by ρ_{eff} and indicates that ρ_{eff} must be at least in the several kΩcm range to get rid of conductive coupling inside the substrate for frequencies around 100 MHz and lower.

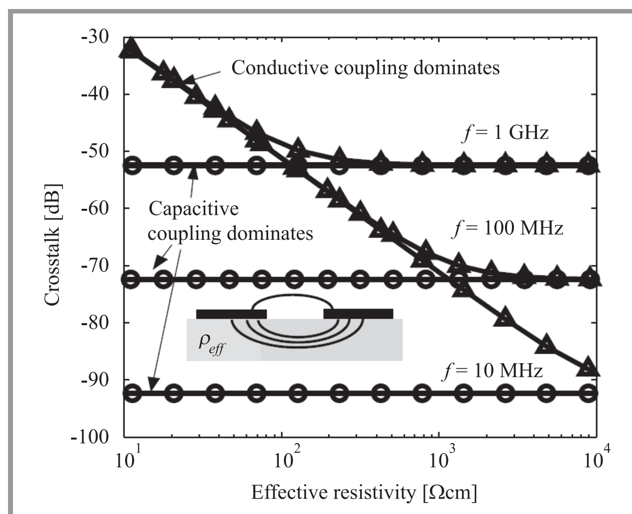

Fig. 17. Simulated crosstalk level at 10 MHz, 100 MHz and 1 GHz as a function of ρ_{eff} according to model presented in [5].

The result of the substrate crosstalk measurements using a classical double-pad structure in which both pads are connected to separate RF probing pads [5] is shown in Fig. 18 in the form of $|S_{21}|$ versus frequency curves. The measurements are performed by using the low-frequency VNA up to 4 GHz and by applying various bias conditions on the coupling pads. The figure shows significantly

higher (∼ 13 dB at 0 V) crosstalk level below 1 GHz for the standard HR SOI wafer, due to conductive effects in the substrate associated with parasitic surface conduction [68]. It also highlights a significant dependence with respect to the applied bias. The crosstalk level is strongly reduced for negative bias and when deep depletion is formed below the BOX, whereas it is enhanced and exhibits higher cutoff frequencies for positive bias and increased inversion below the oxide. On the other hand, the passivated wafer exhibits:

– no effect of the applied bias due to the presence of the trap-rich polysilicon layer below the BOX [55];

– a perfect 20 dB/dec slope which shows that purely capacitive coupling occurs in the measurable frequency range (i.e., above the noise floor of the VNA).

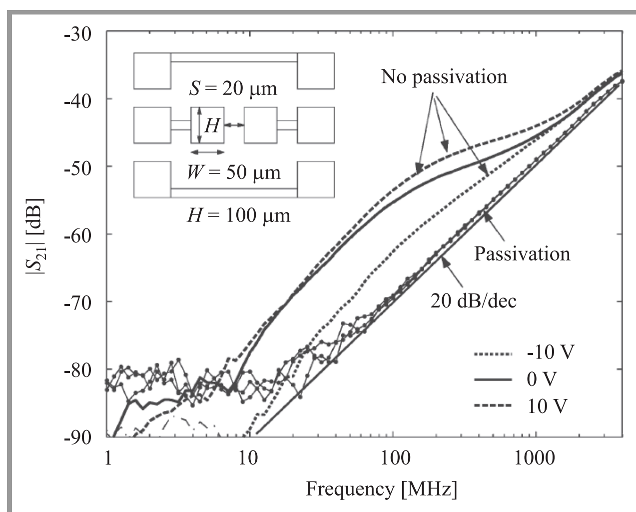

Fig. 18. Crosstalk measured as a function of frequency and under distinct bias conditions on the unpassivated and passivated HR Si wafers.

A reduction of crosstalk below 1 GHz is of particular interest for mixed signal applications, since it is known from previous studies that the frequency spectrum of the noise generated by digital logic typically expands to several hundreds of megahertz, corresponding to multiples of the clock signal [69], [70] or circuit internal resonance frequencies [71]. The generation of noise in that frequency range has also been shown to strongly increase the jitter in phase-locked loops (PLLs), which seem to be particularly sensitive to substrate noise injected at the PLL reference frequency, i.e., in the few hundreds of megahertz range [72]. It is further believed that in terms of crosstalk, the benefits gained by substrate passivation will even increase in the future. Indeed, a reduction of the BOX thickness for the next generations of active SOI devices will be required to reduce short channel effects and self-heating [73].

In [74], we compare experimental DSN characterizations of CMOS circuits lying on SOI and bulk Si substrates. Current injected into the substrate creates substrate voltage fluctuations (substrate noise). It is mainly created by two mechanisms [66]: coupling from the noisy digital power supply circuit and from switching drains.

The DSN for 8 switching inverter trees biased at either 0.8 or 1.2 V and for an input clock frequency of 225 MHz has been measured in the case SOI and Si bulk substrates. DSN for SOI circuit presents a quite different frequency response (Fig. 19(b)). At low frequency, SOI and Si bulk present the same kind of response, with the SOI DSN level decreasing faster with increasing frequency. At higher frequency, the SOI DSN presents a kind of "pass-band filter" shape, which is not visible in the case of the bulk circuit.

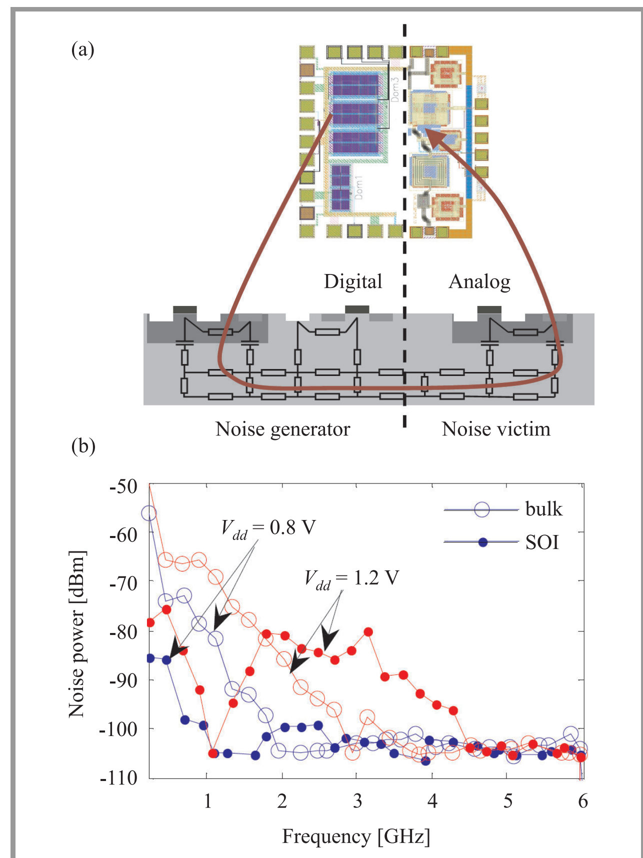

Fig. 19. (a) Schematic representation of the substrate crosstalk between digital and analog parts of a SoC; (b) comparison of the frequency envelope of the measured DSN (clock frequency = 225 MHz, 8 inverter trees).

We have shown in our previous work that this second part of the frequency response is due to ringing on supply rail, due to parasitic capacitances and inductances [75]. For the 1.2 V supply voltage, the SOI technology allows an important reduction of DSN up to 1 GHz. At higher frequency, the noise due to ringing on supply rail becomes dominant, and the bulk circuit shows a lower DSN level. This conclusion is in agreement with the results of studies on the supply noise showing that special attention should be paid to supply rail for SOI technology, due to lower intrinsic decoupling capacitances [76]. At lower power supply (0.8 V), as for the bulk, high frequency noise generation decreases. The ringing supply noise tends thus to be negli-

gible. The SOI technology presents then better DSN results than bulk for frequency up to 2 GHz, and similar DSN level for upper frequency.

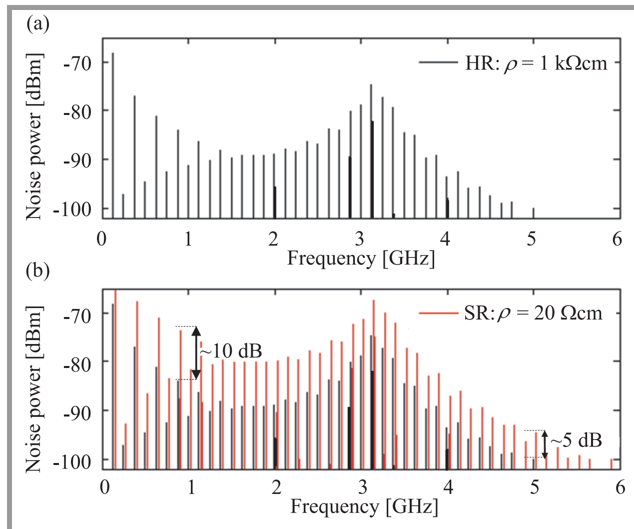

Fig. 20. Frequency spectrum of the measured DSN in (a) standard and (b) high resistivity SOI substrate (clock frequency = 225 MHz, V_{dd} = 1.2 V, 8 inverter trees).

Figure 20 shows the reduction of the DSN thanks to the use of HR SOI substrate compared to standard resistivity SOI. The decrease of the DSN should be even more pronounced if a passivation layer (trap-rich layer) is introduced underneatch the BOX.

5.3. Nonlinearities Along CPW Lines

High-resistivity silicon substrates are promising for RF applications due to their reduced substrate loss and coupling, as presented in the two previous subsections, which helps to enable RF cellular transmit switches on SOI using HRS handle wafers [77], [78]. RF switches have high linearity requirements: for instance, a recent III-V RF switch product specifies less than −45 and −40 dBm for 2nd and 3rd harmonic power (H2 and H3), respectively, at +35 dBm input power [79]. As requirements become even more stringent for advanced multimode phones and 3G standards, it is important to investigate even small contributions to harmonic distortion (HD).

As explained above, when the CPW line is biased the distribution of potential and free carriers inside the Si substrate changes like in the case of a classical MOS capacitor. The variation of carriers distribution in the Si substrate with the applied bias or large RF signal will thus lead to the existence of nonlinear capacitance (C) and conductance (G) associated with the Si substrate. Those variable C and G are at the origin of the harmonics formation inside the Si substrate.

Figure 21 shows the harmonic distortion of Al metal lines on thermally oxidized HRS p-type substrates of different resistivities. The 1 kΩcm substrate presents lower HD than the 20 Ωcm substrate over most of the power sweep.

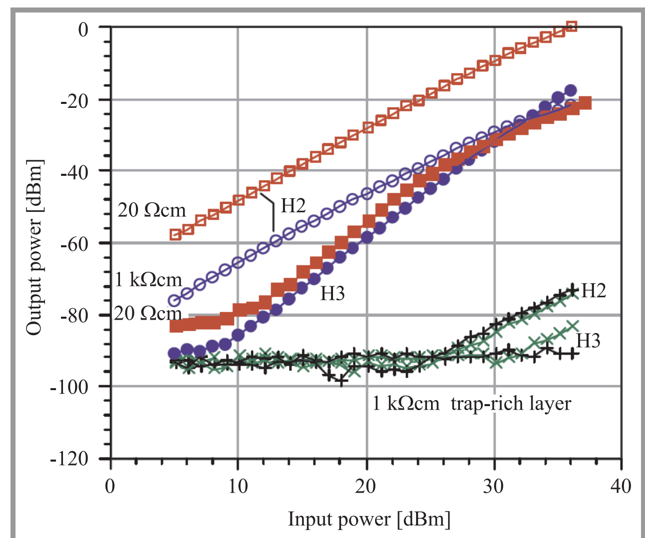

Fig. 21. Measured harmonic distortion for low- and high-resistivity silicon substrates, and high-resistivity silicon substrates with trap-rich layers. CPW metal is aluminum on 60 nm of oxide with length of 2.1 mm. The trap-rich layer significantly reduces HD.

A drastic drop of the HD is observed when the HR Si substrate is passivated with a trap-rich layer (as-deposited amorphous silicon), that is, by at least 50 and 65 dB in H2 and H3, respectively, or to the noise floor. As explained above, thanks to the high density of traps in the polycrystalline silicon or as-deposited amorphous silicon layer located at the Si-SiO_2 interface, the surface potential at this interface is nearly fixed, and the external DC bias or large amplitude RF signal applied to the line does not impact the distribution of carriers inside the Si substrate.

6. Conclusions

The performance of SOI MOSFET technology in microwaves and millimeter waves has been presented. Nowadays, strained SOI N-MOSFET which exhibits a cutoff frequency close to 500 GHz is really competing with the III-V technologies. Thanks to the introduction of high resistivity SOI substrate, the integration of high quality passives is a reality and the reduction of the substrate crosstalk is a real advantage compared to Si bulk for the development of high integration low voltage mixed-mode applications. Major semiconductor companies such as IBM, RFMD, Honeywell, OKI, etc., have already produced several products for the telecommunication market based on SOI RF technologies.

As demonstrated in the present paper, by the introduction of a trap-rich layer underneath the BOX, HR SOI substrate can still be improved. Having a polysilicon-based layer with the thickness of approximately 300 nm sandwiched between the BOX and the HT Si substrate, CPW insertion loss, crosstalk, DSN, as well as harmonic distortion are greatly reduced.

To summarize, present and future HR SOI MOSFET technologies are very good candidatea for mixed-mode low voltage low power RF and even millimeter waves applications.

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